ABSTRACT

Recent research and development efforts in the area of CMOS and IC’s are oriented towards reducing the power and increasing the gain of single chip systems. While focusing the attention on low power and gain in the device, the material used has to be taken into consideration.

In semiconductor industry emerging devices with low power and high gain are mainly used in VLSI applications. The primary driving factor being the increase in scale of integration, the chip has to accommodate smaller and faster transistors than their predecessors. During the last decade conventional scaling in devices has been a challenge for the semiconductor technology. Scaling has been aimed to achieve high speed, low power and high density. However, as scaling approaches its physical limit, it becomes more difficult in real time implementations. Researches carried out to investigate an alternative have led to the introduction of new materials and concepts to overcome the variations. High-k dielectric materials are explored to reduce Off current and parasitic capacitance in devices. Among the different high-k materials available the nano size Zirconium dioxide is suggested as the alternate gate oxide material for devices due to its thermal stability and small grain boundary size based on the experiment carried out.

The double gate (DG) devices are considered to be one of the most promising technologies to meet the requirements of ITRS roadmap, due to its excellent immunity to short channel effects and high On current. Different high-k materials are used in DG MOSFET devices and their performances are compared. Dual Material Gate and Single Halo Channel Engineering devices in Double Gate architecture have also been investigated. Integrated Systems Engineering (ISE) - Technology Computer-Aided Design (TCAD) used for the realization, comparison and analysis of all the devices are analyzed.

DG MOSFET: Double Gate Metal Oxide Field Effect Transistor is designed and simulated in the sub threshold region, linear region, saturation region and various device parameters are computed. Then the impact of high-k dielectric is
analysed by replacing the conventional gate dielectric, Silicon dioxide with various high-k dielectric materials and Nano size ZrO₂ (Zirconium di oxide) is found out to be the best alternative for SiO₂(Silicon di oxide). The device shows improved transconductance and higher drive current. The suitability of nanoscale DG MOSFETS for circuit applications is analyzed with the help of the CMOS inverter circuit and their gains are also measured for circuit applications.

DMDG MOSFET: Gate Engineering Techniques are applied and the conventional DG MOSFETs are used and the simulations are carried out using Sentaurus simulator. The parameters such as On current, Off current, I_on/I_off ratio, DIBL (Drain Induced Barrier Lowering), normalized transconductance, transconductance generation factor, output resistance, intrinsic gain and intrinsic gate capacitances are analyzed for various high-k material for DMDG MOSFET. The suitability of nanoscale DMDG MOSFET for circuit applications is also explored by comparing the performance with the help of CMOS inverter for different high-k dielectrics and the circuit with high-k dielectrics shows a significant improvement in gain.

SHDG MOSFET: Single Halo Double Gate Metal Oxide Field Effect Transistor is developed using Sentaurus simulator and its analog performances are investigated. It is observed that the integration of high-k dielectrics in the devices significantly reduce the short channel effects and Off current in SHDG MOSFETs. The suitability of nano scale SHDG MOSFET for circuit applications is also studied with the help of the CMOS inverter circuit and their gain values are calculated. It is found that ZrO₂ based devices perform considerably better.