CHAPTER 7

CONCLUSION

7.1. SUMMARY OF THE THESIS

The growth of the personal devices has led to the increased need for the design of the devices with low power. Also, in order to meet the real time performance in many of the recent applications, it is necessary to increase the gain of the circuit. Combining these objectives, it becomes customary in the modern day electronic devices to reduce Off current and increase the circuit gain. Hence in this thesis, three different DG MOSFET devices are explored with different gate oxide dielectric materials for VLSI applications are discussed below.

The work proposed in this thesis combines high-k material and device simulation based on different types of DG MOSFET structures. The main drawback of the CMOS technology is high Off current and short channel effect. Double gate transistor as a substitute for bulk CMOS from a single gate device with different high-k material in sub threshold region is proposed in this thesis. Here the ZrO$_2$ dielectric material is synthesized using chemical methods at different room temperatures and optimized for a high-k dielectric constant value. The synthesized ZrO$_2$ material is subjected for impedance analysis and it is found to have high dielectric constant value. Due to high-k value it has a smaller Off current in the CMOS devices than SiO$_2$ as a gate oxide material.

The device parameters for analog applications in sub threshold region of operation with high-k dielectric material gate oxide for DG MOSFET device and their optimization have studied. Improvements in the drain current, transconductance, output resistance and voltage gain for ZrO$_2$ dielectric material are observed over conventional dielectrics in DG MOSFET. The CMOS amplifiers implemented with these DG MOSFET with different high-k dielectric materials have larger voltage gain than conventional CMOS. DIBL is decreased by 88% for ZrO$_2$ as agate oxide material in DG MOSFET as compared with the conventional


SiO$_2$ in the same device. The Off current is also decreased by 61% for ZrO$_2$ compared to SiO$_2$ in DG MOSFET device. The gain of the amplifier increases for the inverting amplifier designed using various high-k dielectric materials for DG MOSFET.

This thesis also analyses the influence of Gate Engineering on the performance of DG MOSFET. With the CMOS processing technology already into the 100-nm regime, fabricating DMDG MOSFET devices should not be complex in the near future. Gate engineered devices show an increase of gain by 66%, increase of gate capacitance by 33%, increase of drive current by 82% and decrease of DIBL by 52% respectively, for ZrO$_2$ as a gate oxide dielectric material were compared with the conventional dielectric material. Thus, the gate work function engineering such as the DMDG MOSFET technology is the most favourable technique for low-power sub threshold analog applications in future.

In this thesis the performance of a SHDG MOSFET is also analyzed. The Off current of the SiO$_2$ gate oxide material based device shows a decrease of about 52% when compared with conventional dielectric material in SHDG MOSFET. This decrease is due to the screening of the drain bias by the step function in the surface potential profile. So any increase in Off current is suppressed in the device. The Drain Induced Barrier Lowering of the device also reduced by around 40% for ZrO$_2$ based device compared with conventional dielectric material. So the Single Halo DG MOSFET can be used for low-power subthreshold analog applications because of its capability to suppress leakage and Short Channel Effects. The SHDG MOSFET exhibits substantial increase in the gain for various high-k materials which makes the device more suitable for subthreshold analog applications. Thus the SHDG MOSFET with ZrO$_2$ shows superior performance when compared to SiO$_2$ based devices.

Hence, three different DG MOSFET devices were proposed and their various parameters are analyzed for various high-k dielectric gate oxide materials for different VLSI applications. The simulation results prove that the circuit
employed with the high-k material perform considerably better for all the devices considered in this thesis.

7.2. SUGGESTIONS FOR FUTURE WORK

The effects of high-k dielectrics with advanced MOSFETs play a vital role in Scaling.

More studies on the effect of high-k dielectric material on stress and strain engineering techniques have to be explored. Because that may give more performance improvement in the nano electronics area in future. Scaling of gate oxide in future will depend on the other various high-k dielectric materials. Group III and V devices with high-k dielectrics are still a concern or research area. The interesting material like HfO$_2$ based oxide material also to be explored.