CHAPTER 3

PERFORMANCE ANALYSIS OF FSTPI FED INDUCTION MOTOR WITH BOOST PFC CONVERTER

3.1 INTRODUCTION

This chapter presents performance of a FSTPI fed induction motor with boost PFC converter. In most electronic power supplies, the AC input is rectified and a bulk capacitor is connected directly after the diode rectifier bridge. This type of utility interface draws excessive peak input currents and hence it produces a high level of harmonics and low input power factor. Due to low power factor the load efficiency is reduced. In order to meet the harmonics limits, new AC-DC converter designs must employ active power factor correction at the input. Therefore boost PFC converter is designed and it is implemented with FSTPI fed induction motor. By digital simulation the characteristics of the induction motor system are investigated and simulation results are presented using Matlab 7.3 platform.

Adly Girgis et al (1992) described the performance of capacitors for power factor correction, which tends to increase the total harmonic distortion. The second concern is the switching of the power factor correction capacitors. During a capacitor switching, transient over voltages are produced which contain a high frequency component. These transient over voltages, if large enough, can damage sensitive power electronic devices. Krishnan et al (1995) analyzed the impact of the power factor correction circuit on induction motor drive system, in which the power factor correction circuit has a single
power device with a forward diode in the boost configuration. The above approach increases the losses in diode and bridge rectifier and consequently decreases the system efficiency. Jung Cho et al (1997) proposed zero voltage transition isolated PWM boost converter for single stage power factor correction. The above approach has one disadvantage like low frequency ripple which exists in the output. Yamamoto et al (2002) designed and analyzed canonical switching cell converter performance. Yuen-Haw Chang (2004) designed CMOS gate based switched capacitor boost DC-AC inverter. The designed topology produces heat problem due to power loss and hence system performance is affected by poor efficiency. Paul Nosike Ekemezie (2007) designed boost PFC converter and performance analyzed in the case of input voltage and current. The above converters are not suitable to relatively small size power supply due to its lower efficiency.

With relevant to these observations, in the proposed research work the boost converter is implemented with FSTPI fed induction motor and performances are analyzed in view of power factor, THD and efficiency.

3.2 BOOST CONVERTER: PRINCIPLE OF OPERATION

Figure 3.1 shows the basic circuit of boost converter for power factor correction. An uncontrolled diode rectifier with a boost converter is used to convert the single phase AC voltage into a constant DC link voltage, which is fed to the PWM inverter supplying an induction motor. The boost converter is the widely used topology for achieving power factor correction. This converter draws unity power factor current from the AC mains and eliminates a harmonic current which regulates the DC link voltage even under fluctuating voltage conditions of AC mains. This circuit uses a snubber inductor which is connected in series with main switch and rectifier to control the di/dt rate of the rectifier.
The bulk energy storage capacitor sits on the output side of the converter rather than just after the diode rectifier bridge. The average inductor current which charges the bulk capacitor is proportional to the utility line voltage. For proper operation, the output voltage must be higher than the peak line voltage and current drawn from the line must be proportional to the line voltage. In circuit operation, it is assumed that the inductance of boost inductor is large so that it can be represented by constant current source and that the output ripple voltage is negligible so that the voltage across the output filter capacitor can be represented by constant voltage source.

SIMULATION RESULTS

3.2.1 Design procedure of simulation parameters

Induction Motor

Consider the loop voltage equations of the induction motor

\[ V_{as} = (R_s + j\omega L_{ls})I_s + Z_o I_o \quad \text{(3.1)} \]

\[ 0 = \left(\frac{R_f}{s} + j\omega L_{lr}\right)I_r + Z_o I_o \quad \text{(3.2)} \]
where

\[ I_s = I_r + I_o \] (3.3)

\[ Z_o = \frac{j\omega_s L_m R_e}{f R_e + j\omega_s L_m} \] (3.4)

\[ I_s, I_r \text{ and } I_o \] are the stator, rotor and magnetizing branch currents respectively. \( V_{as} \) is the stator phase voltage, \( f_s \) is the supply stator frequency, \( R_s \) and \( R_r \) are stator and stator referred rotor phase resistances, respectively. \( L_m, L_{ls} \text{ and } L_{lr} \) are the magnetizing, stator leakage and stator referred rotor leakage inductances per phase, respectively. \( s \) is the slip which is given by

\[ s = \frac{\omega_m - \omega_r}{\omega_s} = 1 - \frac{\omega_r}{\omega_s} = 1 - \frac{P}{2} \frac{\omega_r}{\omega_s} = 1 - \frac{nP}{120f_s} \] (3.5)

where \( \omega_m \) and \( \omega_s \) are rotor mechanical and electrical angular speed, respectively. \( n \) is the rotor speed in rpm, and \( P \) is the number of poles. The mechanical power developed (\( P_m \)) in the rotor for a \( m \)-phase machine is given by

\[ P_m = m I_r^2 R_r \frac{(1-s)}{s} \] (3.6)

where \( m \) is three in the present study.

**Inverter**

The inverter output phase voltage is programmed as a function of stator frequency command of the induction motor and given as

\[ V_i = V_{as} = V_{of} + k_{vf} f_s \] (3.7)

where \( V_{of} \) is the offset voltage and it is given by

\[ V_{of} = I_b R_s \] (3.8)
and the constant $k_{vf}$ is given by

$$k_{vf} = \left( \frac{V_b - V_{rf}}{f_b} \right)$$  \hspace{1cm} (3.9)

where $I_b$ is the base (rated) stator phase current, $V_b$ is the base (rated) stator phase voltage and $f_b$ is the base (rated) stator frequency.

The inverter switching and conduction losses are given approximately by

$$P_{ins} = m\frac{1}{2} V_{dc} I_s f_{sw}(t_{ri} + t_{fi} + t_{rr})$$  \hspace{1cm} (3.10)

$$P_{inc} = m[I_s V_{CE}]$$  \hspace{1cm} (3.11)

where $t_{ri}$ and $t_{fi}$ are the rise and fall times of the power devices, $t_{rr}$ is the reverse recovery time of the freewheeling diodes, $f_{sw}$ is the inverter switching frequency, $V_{CE}$ is the on state voltage drop across the power device, $V_{dc}$ is the dc link voltage input to the inverter and $P_{ins}$ and $P_{inc}$ are the inverter switching and conduction losses, respectively.

**Bridge Rectifier**

The conduction losses are considered in this study and they are derived as

$$P_{br} = 2V_d I_{in} = 2 \times 0.7 \times \frac{P_{in}}{V_{in}} = (1.4) \frac{P_{in}}{V_{in}}$$

where $V_d$ is the diode conduction voltage drop, $P_{in}$ is the ac input power from the main supply, $V_{in}$ is the ac input voltage and $I_{in}$ is the ac input current and $P_{br}$ is the conduction losses in a single phase rectifier bridge.
Boost PFC Circuit

AC input voltage (rms)  90V-270V

Input frequency 47-53 Hz

Target efficiency ($\eta$) is 72% (min) at 90V AC/1000W

The selection of boost converter components is based on the following standard procedure:

Maximum input power, $P_{in}\,(max) = \frac{P_o\,(max)}{\eta_{min}} = \frac{1000\,W}{0.72} = 1338\,W$

Maximum rms input current, $I_{in\,(rms)}\,max = \frac{P_{in}\,(max)}{V_{in\,(rms)\,min}} = \frac{1338}{90} = 15.4\,A$

Maximum peak input current, $I_{in\,(pk)\,max} = I_{in\,(rms)\,max} = 15.4 \times \sqrt{2} = 21.7\,A$

Average input current, $I_{in\,(avg)\,max} = \frac{2 \times I_{in\,(pk)\,max}}{\pi} = \frac{2 \times 21.7}{\pi} = 13.87\,A$

Boost Capacitor

Boost capacitor, $C_{in} = K_{\Delta I\,L} \cdot \frac{l_{in\,(rms)\,max}}{2\pi f_{sw} \times r \times V_{in\,(rms)\,min}}$

$K_{\Delta I\,L} = \text{Inductor current ripple factor (20% in this design)}$

$r = \text{high frequency voltage ripple factor typically from 3\% to 9\% (5\% used in this design)}.$

Switching frequency, $f_{sw} = 100000\,Hz$

Boost capacitance, $C_{in} = 0.2 \times \frac{15.4}{2\pi \times 100000 \times 0.05 \times 90}$

$C_{in} = 1\,\mu F.$
**Boost Inductor**

Minimum input peak voltage, \( V_{in(pk)\text{min}} = \sqrt{2} V_{in(pk)\text{min}} \)

\[ = 90\sqrt{2} = 127V \]

Peak boost transistor duty cycle

\[ D_{pk} = 1 - \frac{V_{in(pk)}}{V_o} = 1 - \frac{127}{400} = 0.6825 \]

**Inductor ripple current**

\[ \Delta I_L = 0.2 I_{in(pk)\text{max}} = 0.2 \times 21.7 \]

\[ = 4.34 \text{ A} \]

\( \Delta I_L \) is based on the assumption of 20% ripple current

**Peak inductor current**

Maximum load current, \( I_L(pk)\text{max} = I_{in(pk)\text{max}} + \frac{\Delta I_L}{2} \)

\[ = 21.7 + \frac{4.34}{2} = 23.87 \text{ A} \]

Inductance, \( L = \frac{V_{in(pk)\text{min}} \times D_{pk}}{f_{sw} \times \Delta I_L} = \frac{127 \times 0.6825}{100000 \times 4.34} = \frac{86.6775}{434000} = 2 \times 10^{-4} \)

\[ = 2\text{mH is selected} \]

**Output Capacitor**

The value of the output capacitor impacts hold up time and ripple voltage. In this design, the criterion for selection of this capacitor is the amount of tolerable ripple in the output voltage.

\[ C_{out} = \frac{P_o}{2\pi f_r \times \Delta V} \]
where $f_r$ is a frequency of the rectified sine wave and $\Delta V$ is desired peak to peak output voltage ripple

$$\text{Output capacitor, } C_{\text{out}} = \frac{1000}{2\pi \times 100 \times 0.03 \times 400} = \frac{2.5}{7536} = 330 \ \mu F$$

The parameters of the induction motor are given below.

Stator resistance, $r_s = 1.11 \Omega$, Rotor resistance, $r_r = 1.08 \Omega$

Stator inductance, $l_s = 0.006 H$, Rotor inductance, $l_r = 0.006 H$

Mutual inductance, $M = 0.20 H$

Poles, $P = 2$

Moment of inertia, $J = 0.02 Kg \ m^2$

Co-efficient of viscous friction, $F = 0.00575 \ Nm/(rad/sec)$

The parameters used in the simulation are

- Nominal line voltage ($V_{ac}$) : 200V
- Output Voltage ($V_o$) : 200V DC
- Output power ($P_o$) : 1KW
- Boost inductor : 2mH
- Boost capacitor : 1µF
- Output capacitor : 330µF
- Switching frequency : 100 KHz
The complete simulink block diagram of system is shown in Figure 3.1. This block diagram consists of two blocks. The block which consists switching pulses generates PWM pulses for four switches of FSTPI at the terminals Out 1 to Out 4. The other block consists FSTPI, induction motor and diode bridge rectifier. Voltage block is used to display the three phase voltage waveforms. Figure 3.2 shows the circuit of FSTPI fed induction motor with boost PFC converter. This circuit contains three phase input AC power supply, diode bridge rectifier, boost power factor correction circuit with an inductor and capacitor, split capacitor, four MOSFET switches and three phase induction motor. Figure 3.3 shows the power factor measurement circuit of boost PFC converter. It can be seen that a better power factor of 0.998 is achieved in the designed converter than the existing power CMOS-gate based switched capacitor boost DC-AC inverter (CMOS-TG QSC boost DC-AC inverter). The inductor size and the amount of inductor current ripple will affect circuit efficiency and power factor. The designed converter increases the inductor size and hence reduces switching loss. Therefore proposed converter provides improved power factor and efficiency. The input voltage and current waveform of existing converter are shown in Figure 3.4. The waveform clearly indicates that the power factor of existing converter is 0.94.

Figure 3.5 presents the switching pulses applied to switches M1 and M2. Figure 3.6 illustrates the phase voltage applied to the three phase induction motor. Figure 3.7 shows the efficiency of three phase induction motor in which boost converter FSTPI is used. It can be seen that the efficiency has improved to 75% due to minimized conduction losses. The efficiency of designed converter is high when compared to existing CMOS-TG QSC boost DC-AC inverter which has only 70% of efficiency. The efficiency curve of CMOS-TG QSC boost DC-AC inverter is shown in Figure 3.8. The simulation results show that the designed converter provides better performance than existing CMOS-TG QSC boost DC-AC inverter designed
The performance comparison of designed boost converter and an existing converter is revealed in Table 3.1.

Table 3.1  Performance comparison between existing converter and proposed boost converter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Performance of existing converter</th>
<th>Performance of proposed boost converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>70</td>
<td>75</td>
</tr>
<tr>
<td>Power Factor</td>
<td>0.94</td>
<td>0.998</td>
</tr>
</tbody>
</table>


Figure 3.2  Simulation Block Diagram of FSTPI Fed Induction Motor Drive System with Boost Converter
Figure 3.3 Four Switch Three Phase Inverter Fed Induction Motor System with Boost Converter
Figure 3.4 Power Factor Measurement of Boost PFC Converter

Figure 3.5 Power Factor Measurement of CMOS-TG QSC boost DC-AC inverter
Figure 3.6 Driving Pulses for M1 and M2

Figure 3.7  Phase Voltage

Figure 3.8  Output Power Vs Efficiency of FSTPI Fed Induction Motor with Boost Converter
Figure 3.9 Output Power Vs Efficiency of CMOS-TG QSC boost DC-AC inverter

3.4 CONCLUSION

This chapter illustrated the simulation study of implementation of boost PFC converter with FSTPI fed induction motor. Implementation of boost PFC converter reduces the losses produced by system components and increases the system efficiency and input power factor. From the simulation study, it is established that the FSTPI fed induction motor with boost PFC converter provides a power factor of 0.998 compared to a value of 0.94 for the existing CMOS-TG QSC boost DC-AC inverter. The efficiency of FSTPI fed induction motor is 75% compared to 70% in case of the existing converter. The simulation result exhibits better performance of boost converter than existing converter.