CHAPTER 1

INTRODUCTION

1.1 GENERAL

The induction motors are most widely used in industrial control and automation. They are robust, reliable, cheap and available in all power ratings. The squirrel cage types of induction motors are very popular in variable speed drives. With the invent of high speed power semiconductor devices three phase inverters are widely used device for variable speed AC motor drives. A conventional six switch three phase voltage source inverters have been utilized for variable speed drives. The SSTPI consists three legs, with a pair of complementary power switches per phase. Due to the nonlinear behavior of power switched circuits, distorted currents are normally drawn from the line which results low power factor and high total harmonic distortion in conventional inverter fed induction machine. Hence power switch reduction from six to four reduces the total harmonic distortion as well as the cost. The FSTPI uses only two legs with four switches. The main features of FSTPI are:

- Reduced switch and freewheeling diode current
- Reduced price because of the reduction in number of switches
- Number of drive circuits are only two as only two branches are controlled
- Reduction of conduction loss is dependent on the power semiconductor devices
In induction motor drive applications, drawing sinusoidal current from the utility and less harmonics injection into the utility are providing high efficiency operation and low cost. Hence this research work mainly focuses on the impact of the power factor correction circuit on inverter fed induction motor drive systems. To improve the input power factor of FSTPI fed induction motor the boost converter, boost converter with compound active clamping and half bridge doubler boost converter are implemented in the proposed method. Most of the past research on variable speed drives mainly concentrated on the development of the efficient control algorithms. However, the cost, simplicity and flexibility of the drive system are not considered. Thus, the main issue of this research work is to develop a cost effective, simple and efficient high performance FSTPI fed induction motor drive systems. The proposed work mainly focuses on performance of FSTPI fed induction motor with respect to system efficiency, power factor and THD. The proposed method can be applied in the large power and automotive industrial applications since it reduces additional heating and minimizes over voltages due to reduced THD and improved power factor.

1.2 BACKGROUND OF FSTPI FED INDUCTION MOTOR

The main objectives of FSTPI fed induction motor are reduction of both the cost of the inverter and the computation for real time implementation. The FSTPI fed induction motor has a problem of low power factor due to the harmonic current injected into the power supply. Therefore, implementation of power factor correction schemes in the above method is essential. In this thesis simulation study of FSTPI fed induction motor is developed with power factor correction converters to reduce total harmonic distortion and to improve the input power factor. The simulation work is done by matlab/simulink.

Based on the conceptual frame of reference, the performance of FSTPI system is not analyzed when induction motor is used as a load. In this thesis, the performances of FSTPI fed induction motor have been analyzed in terms of system efficiency, power factor and THD. Adly Girgis et al (1992) described the performance of capacitors for power factor correction, which tend to increase the total harmonic distortion. The second concern is the switching of the power factor correction capacitors. During a capacitor
switching, transient over voltages are produced which contain a high frequency component. These transient over voltages, if large enough, can damage sensitive power electronic devices. Krishnan et al (1995) analyzed the impact of the power factor correction circuit on induction motor drive system, in which the power factor correction circuit has a single power device with a forward diode in the boost configuration. Hui et al (1997) implemented soft switched boost type power factor correction circuit. The above approaches increase the losses in the diode and bridge rectifier. Jung Cho et al (1997) proposed zero voltage transition isolated PWM boost converter for single stage power factor correction. Liaw et al (2000) implemented soft switching mode rectifier consisting of a power factor correction converter. The above technique provides larger conduction losses and suits for low power applications. Yaan-Haw Chang (2004) designed power CMOS gate based switched capacitor boost DC-AC inverter and integrated with boost converter. The performance of the above technique is affected by conduction and switching losses. The proposed work utilizes power factor correction circuit with boost converter and it is implemented with four switch inverter. The designed circuit is implemented with three phase induction motor and the performances have been analyzed.

Jovanovic (1998) introduced inductor in the series path of the boost switch rectifier to reduce the reverse recovery losses. Carlos Alberto Canesin et al (1999) described ZCS-PWM boost rectifier with IGBT as switching device. The above method provides high turn off losses. Yamamoto et al (2002) designed power factor correction circuit by buck boost converter. The designed converter is suitable to apply to small size power supply due to large storage circuit energy. Chen et al (2002) designed compound active- clamping DC-DC converter. In the above method, the auxiliary switch of the converter needs an additional diode and an inductor to reduce the resonance between
snubber inductor and the parasitic capacitance of the auxiliary switch. Luiz Henrique et al (2005) analyzed analog and digital control types applied to the boost converter. The above technique has a disadvantage of control circuit complexity and the increased number of components implying larger cost and weight. Paul Nosike Ekemezie (2007) implemented AC-DC converter for power factor correction towards digital control. Rui Li et al (2007) designed ZVS-SVM controlled three phase boost converter. The above methods increase turnoff loss of switching devices and resonance between junction capacitance and inductance. In the proposed technique, the boost converter employing compound active clamping is designed and implemented with four switch inverter. The three phase induction motor is fed by the four switch inverter and performances has been analyzed and compared with an existing converter in terms of power factor, efficiency and THD. Maksimovic et al (1995) designed power factor correction circuit with boost doubler rectifier. This technique is suitable for high power operations with the maximum voltage range of 260V. Ramesh Srinivasan et al (1998) designed converter using half bridge topology. The designed converter is suitable for low input voltage system and it is not suitable for universal input voltage operation. Shmilovitz et al (2000) implemented controller for a half bridge boost rectifier. Roberto Mendes Finzi et al (2005) designed half bridge topology. The above techniques produce minimum efficiency and low power factor due to voltage stresses and commutation losses of switching device. Bo Feng et al (2005) designed power factor correction circuit with boost converter employing compound active clamping. In the above technique the performance of the converter has suffered due to parasitic resonance between the resonant inductor and the junction capacitance of the boost diode. In the proposed method the half bridge topology with boost converter is designed
and implemented with FSTPI fed three phase induction motor. Three phase induction motor performances have been analyzed and compared with an existing converter which utilizes compound active clamping. The proposed technique utilizes lower input voltage, having lower power losses than the conventional boost rectifier. Due to reduced number of power switches in the proposed method the voltage stresses and commutation losses are minimized and consequently provide improved efficiency and reduced THD. In this thesis, the simulation studies of various converters employed with FSTPI fed induction motor drive have been analyzed. The simulation result shows better performance of the designed converter.

1.3 OBJECTIVES OF THE THESIS

The objective of this thesis can be listed as follows:

(i) Comparing the performance characteristics of FSTPI fed induction motor with conventional SSTPI fed induction motor.

(ii) Simulating and studying the performance of FSTPI fed induction motor with boost PFC converter.

(iii) Simulating and analyzing the performance of FSTPI fed induction motor with boost converter employing compound active clamping.

(iv) Simulating and studying the performance of FSTPI fed induction motor with half bridge doubler boost converter.
1.4 ORGANIZATION OF THE THESIS

The remaining chapters of the thesis are organized as follows.

Chapter 2 discusses the simulation study and experimental implementation of FSTPI fed induction motor. The total harmonic distortion is compared with conventional inverter fed induction motor. The experimental results are presented to demonstrate the validity of the simulated results.

Chapter 3 deals with the performance of FSTPI fed induction motor with boost converter. Power factor correction converter is implemented at the input to improve the power factor.

Chapter 4 provides the performance of FSTPI fed induction motor with boost converter employing compound active clamping. It can effectively reduce the loss caused by diode reverse recovery.

Chapter 5 depicts the performance of FSTPI fed induction motor with half bridge doubler boost converter. It can effectively reduce the loss caused by commutation.

Chapter 6 summarizes the work presented in the thesis. The main contributions of the thesis are highlighted and a list of potential research directions, to study further issues of the FSTPI fed induction motor are presented.