APPENDIX 1

ATMEL 89C2051 MICROCONTROLLER DESCRIPTION

A 1.1 Features

- 2K Bytes of reprogrammable Flash Memory
- 2.7 V to 6V operating range
- Fully static operating : 0 Hz to 24 MHz
- Two level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 15 Programmable I/O Lines
- Two 16-Bit Timer / Counters
- Six Interrupt Sources
- Programmable Serial UART Channel.
- Direct LED Drive outputs
- On-Chip Analog Comparator
- Low Power Idle and power down Modes

A 1.2 Description

The AT89C2051 is a low-voltage, high-performance CMOS 8-bit microcomputer with 2K bytes of Flash programmable and erasable read-only memory (PEROM). The device is manufactured using ATMEL high-density nonvolatile memory technology and is compatible with the industry-standard
MCS-51 instruction set. ATMEL AT89C2051 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89C2051 provides the following standard features: 2K bytes of Flash, 128 bytes of RAM, 15 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the AT89C2051 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware resets.

A 1.3 Pin Configuration of ATMEL 89C2051

![Pin Configuration of ATMEL 89C2051 Microcontroller](image)
A 1.4 Block Diagram

Figure A 1.2 Block Diagram of Atmel 89C2051 Microcontroller

A 1.5 Pin Description

VCC-Supply voltage.

GND-Ground.
Port 1

Port 1 is a 8-bit bi-directional I/O port. Port pins P1.2 to P1.7 provide internal pull-ups. P1.0 and P1.1 require external pull-ups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. Port 1 output buffers can sink 20 mA and can drive LED displays directly. When 1 is written to Port 1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs. Port 1 also receives code data during Flash programming and verification.

Port 3

Pins P3.0 to P3.5 and P3.7 are seven bi-directional I/O pins with internal pull-ups. P3.6 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general purpose I/O pin. The Port 3 output buffers can sink 20 mA. When 1 is written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs.

Port 3 also serves the functions of various special features of the AT89C2051 as listed below:

Table A 1.1 Special Features of ATMEL 89C2051 Microcontroller

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3.0</td>
<td>RXD (serial input port)</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD (serial output port)</td>
</tr>
<tr>
<td>P3.2</td>
<td>INT0 (external interrupt 0)</td>
</tr>
<tr>
<td>P3.3</td>
<td>INT1 (external interrupt 1)</td>
</tr>
<tr>
<td>P3.4</td>
<td>T0 (timer 0 external input)</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1 (timer 1 external input)</td>
</tr>
</tbody>
</table>
Port 3 also receives some control signals for Flash programming and verification.

**RST**

Reset input. All I/O pins are reset to 1’s as soon as RST goes high. Holding the RST pin high for two machine cycles while the oscillator is running, resets the device. Each machine cycle takes 12 oscillator or clock cycles.

**XTAL1**

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

**XTAL2**

Output from the inverting oscillator amplifier.

**A 1.6 Oscillator Characteristics**

The XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop; but minimum and maximum voltage high and low time specifications must be observed.
A 1.7  Oscillator Connections

![Oscillator Connections Diagram]

Note: C1, C2 = 30 pF ± 10 pF for Crystals
      = 40 pF ± 10 pF for Ceramic Resonators

A 1.8  IR2110 HIGH AND LOW SIDE DRIVER

Features:

- Floating channel designed for bootstrap operation, fully operational to +500 V or +600 V tolerant to negative transient voltage, dv/dt immune.
- Gate drive supply range from 10 to 20 V.
- Under voltage lockout for both channels.
- 3.3 V logic compatible, separate logic supply range from 3.3 V to 20 V.
- Logic and power ground ± 5V offset.
- CMOS Schmitt – triggered inputs with pull-down.
- Cycle by cycle edge triggered shut down logic.
- Matched propagation delay for both channels.
- Output is in phase with input.

Figure A 1.4 Driver Circuit