CHAPTER 5
FOUR SWITCH THREE PHASE INVERTER FED
INDUCTION MOTOR WITH HALF BRIDGE
DOUBLER BOOST CONVERTER

5.1 INTRODUCTION

This chapter depicts the performance of FSTPI fed induction motor with half bridge doubler boost converter. In this proposed topology the given input voltage is converted into doubled output voltage. The half bridge boost converter is an adequate topology to obtain high DC voltages in AC-DC converters. Maksimovic et al (1995) introduced boost doubler rectifiers and performance analyzed in terms of power factor, THD and efficiency. The above method utilizes power factor controller to minimize the harmonics, thus harmonics are not minimized to desired level. Ramesh Srinivasan et al (1998) designed converter using half bridge topology and analyzed the performance with respect to power factor and efficiency with single phase load. In the above method the converter performances are affected due to minimum commutation losses. Shmilovitz et al (2000) implemented controller for a half bridge boost rectifier. In the above method the large size capacitors produce high surge currents during the initial charge up. Hence a small displacement factor exists between voltage and current which decreases the input power factor and consequently increases THD. Roberto Mendis Finzi Neto (2005) designed half bridge doubler boost converter and analyzed the performance in view of power factor and THD. Due to voltage stress across the semiconductor devices the power factor of the circuit is affected.
This proposed research work simulates the half bridge doubler boost converter with FSTPI fed induction motor drive. The simulation result shows that the designed converter improves the system performance than existing system. The simulation work is carried out using matlab/simulink.

5.2 HALF-BRIDGE DOUBLER BOOST CONVERTER

In the half bridge circuit the output voltage will be twice the value of the input voltage. Thus, for a nominal 230V input voltage range, the output voltage will be greater than 760V. Thus a high voltage rated semiconductor components are required to meet the desired design. For a nominal 110V input voltage range, the output voltage range will be greater than 370V. This voltage level is acceptable and adopted in boost PFC circuits. Thus, the half bridge topology is proposed in this chapter as a good choice for the 110 V input voltage system.

![Basic Circuit of Half Bridge Doubler Boost Converter](image)

**Figure 5.1 Basic Circuit of Half Bridge Doubler Boost Converter**

The half bridge doubler boost topology is shown in Figure 5.1. The voltage across each semiconductor device is equal to $V_o$ and the voltage ripple across capacitors $C_2$ and $C_3$ is reduced. The control circuit employed in this topology is rather simple, since the same gate signal can be applied to main
switches $S_1$ and $S_2$. By considering boost PFC circuit and assuming sinusoidal input current at unity power factor

$$P_{in} = \text{input power} = V_s I_s$$

$$P_{loss} = \text{Conduction loss in bridge rectifier} = 2V_F \frac{I_s}{K_f}$$

where $V_s$ is rms input voltage, $I_s$ is rms input current and $V_F$ is diode forward voltage drop.

When only conduction losses considered

Bridge efficiency

$$= \left( \frac{P_{in} - P_{loss}}{P_{in}} \right)$$

$$= \left( 1 - 1.82 \frac{V_F}{V_S} \right)$$

From the above equation, the reduction in efficiency at higher $V_F$ values suggests that by reducing number of devices in series the total conduction voltage drop in the semiconductor devices and significantly improves the overall efficiency of the PFC circuit. The main advantage of this topology is that at any time there is only one semiconductor on stage voltage drop which may be expected to result in high operating efficiencies.

5.2.1 Circuit Operation

For the control action to be effective throughout the line cycle, it is essential that the voltage across each of the capacitors $C_1$ and $C_2$ be maintained to be greater than the instantaneous value of the line voltage.
Mode 1 and 2 correspond to the two modes of circuit operation. When the inductor current strikes the lower bound, $S_1$ is turned on. $S_1$ conducts if $I_L$ is greater than zero, otherwise $D_1$ conducts. In either case, as the voltage across $C_1$ is greater than the line voltage peak. When the inductor strikes the upper bound, $S_2$ is turned on. $S_2$ and $D_2$ conduct depending on $i_L$ polarity. The overall output voltage is the sum of the individual capacitor voltages and hence must be greater than twice the input voltage peak.
Steady state analysis

The aim of the analysis is to study and predict the performance of the circuit.

The following assumptions are made in the analysis

(i) The line voltage varies sinusoidally and is given by the expression
\[ V_S = V_P \sin \theta \]
where \( V_P \) is the peak line voltage and \( \theta = \omega t \) (\( \omega \) is the angular line frequency)

(ii) As the switching frequency is much higher than the line frequency, the line voltage is assumed to be constant during each inductor current switching cycle.

(iii) The output capacitors are large enough so that their voltage ripples (both the switching frequency and line frequency) can be neglected. Each of the two capacitors has the same value equal to \( C \).

(iv) For unity PF operation, neglecting switching components \( i_L = I_P \sin \theta \), where \( I_P \) is the peak line current.

(v) Converter losses are neglected. Therefore, applying input-output power balance
\[ P_o = V_o I_o = \frac{V_P I_P}{2} \]
where \( P_o \) is an output power and \( I_o \) is load current.

(vi) Voltage across capacitors \( C_1 \) and \( C_2 \) are both greater than the peak value of the line voltage \( V_P \).

(vii)
5.3 SIMULATION RESULTS

5.3.1 Design Procedure of Simulation parameters

The simulation model of the half bridge voltage doubler boost converter rated 50Hz, 1KW, 100V DC. The maximum input current slope during the zero crossing provided by this converter is approximately given by

\[ \Delta i_s = \frac{V_{d/2}}{\Delta t_{on} L} \]

When \( \Delta t_{on} \) is assumed as half of the switching cycle, considering 100KHz as switching frequency and 1A as change in input current, \( \Delta i_s \), then inductance of 10mH is obtained for L.

Power balance equation can be used to define voltage, current and output load ratings,

\[ V_s I_s = V_d I_d \]

where \( V_s, I_s \) are source voltage and current and \( V_d, I_d \) are destination voltage and current.

The specification of the capacitors start with the derivation of the DC bus current, \( i_{bus} \). The expression of \( i_{bus} \) is

\[ i_C = \frac{\sqrt{2} I_S}{2} \sin \omega_s t - \frac{\sqrt{2} I_S}{4} \cos 2\omega_s t \]

Only AC component of \( i_{bus} \) will flow through the capacitors. Therefore by neglecting the high frequency harmonics, the current in each capacitor results in

\[ i_C = \frac{\sqrt{2} I_S}{2} \sin \omega_s t - \frac{\sqrt{2} I_S}{4} \cos 2\omega_s t \]
It can be seen that the fundamental frequency flows through the capacitors. By assuming specified ripple factor with the capacitor rms current the capacitor value can be obtained by

\[ C = \frac{2I_{\text{rms}}}{\omega_s (RF) V_d} \]

By considering \( f_s = 100\text{KHz} \), \( RF = 3\text{mA} \), \( V_d = 100\text{V} \) the value of capacitance obtained is 500 \( \mu \text{F} \) each.

Simulation test is performed on the proposed half bridge doubler boost converter FSTPI fed induction motor using matlab/simulink as shown in Figure 5.4. The parameters of the induction motor are given below.

Stator resistance, \( r_s = 1.11\Omega \), Rotor resistance, \( r_r = 1.08\Omega \)

Stator inductance, \( l_s = 0.006\text{H} \), Rotor inductance, \( l_r = 0.006\text{H} \)

Mutual inductance, \( M = 0.20\text{H} \)

Poles, \( P = 2 \)

Moment of inertia, \( J = 0.02\text{Kg m}^2 \)

Co. Efficient of viscous friction, \( F = 0.00575\text{Nm} / (\text{rad/sec}) \)

The parameters used in the simulation are

Nominal line voltage (\( V_{ac} \)) : 100V
Output Voltage (\( V_o \)) : 200V DC
Output power (\( P_o \)) : 1KW
Boost inductor : 10mH
Output capacitor : 500\( \mu \text{F} \)
Switching frequency : 100 KHz
Figure 5.5 shows the power factor measurement of boost converter with half bridge double boost converter. It can be seen that the designed topology has improved power factor to the value of 0.9998. From the result the power factor of designed converter is high as existing converter which has a value of 0.996.

Figure 5.6 presents the switching pulses applied to switches M1 and M2. Figure 5.7 illustrates the phase voltage applied to the three phase induction motor which is operated with half bridge doubler boost converter. It can be seen that the output voltage exceeds more than twice the input voltage.

Figure 5.8 depicts the efficiency of three phase induction motor in which efficiency is improved to 98%. It can be seen that the designed topology has improved efficiency than boost converter with compound active clamping which has only 97.7% of efficiency as seen in Figure 5.9.

Figure 5.10 demonstrates the THD waveforms. It can be seen that the THD is reduced to 1.84% compared to the existing converter which has a value of 3.1%. The results of improved efficiency and reduced THD indicate that the voltage stresses and commutation losses of proposed method are reduced due to reduced number of switches. The THD waveform of existing converter with compound active clamping is shown in Figure 5.11. The simulation result exhibits the proposed converter has better performance over boost converter with compound active clamping converter designed by Bo Feng (2005) with respect to power factor, efficiency and THD.
Figure 5.4  Four Switch Three Phase Inverter Fed Induction Motor System with Half Bridge Doubler Boost Converter
Figure 5.5  Power Factor Measurement of Boost Converter with Half Bridge Doubler Boost Converter

Figure 5.6 Driving Pulses for Switches M1 and M2
Figure 5.7 Phase Voltage

Figure 5.8 Input Voltage Vs Efficiency of Half Bridge Doubler Boost Converter FSTPI Fed Induction Motor
Figure 5.9  Input Voltage Vs Efficiency of boost converter with compound active clamping converter

Figure 5.10  FFT Analysis for Half Bridge Doubler Boost Converter
FSTPI Fed Induction Motor
According to the results presented above, the following advantages can be attributed to the proposed converter.

- The voltage across the semiconductor devices is reduced and approximately equal to the output voltage.
- Doubled output voltages can be achieved.
- There are no switching losses.
- Efficiency is considerably high.
- Improved power factor.
- Significantly low THD.

The performance comparison of designed converter and an existing half bridge doubler boost converter is revealed in Table 5.1.
Table 5.1 Performance comparison between existing converter and proposed Half bridge doubler boost converter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Performance of existing converter</th>
<th>Performance of proposed Half bridge doubler boost converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>97.7%</td>
<td>98%</td>
</tr>
<tr>
<td>Power Factor</td>
<td>0.996</td>
<td>0.9998</td>
</tr>
<tr>
<td>THD</td>
<td>3.1%</td>
<td>1.84%</td>
</tr>
</tbody>
</table>


5.3 CONCLUSION

The proposed half bridge doubler boost converter with FSTPI fed induction motor drive has been simulated using matlab/simulink in this chapter. The designed half bridge doubler boost converter requires minimum number of switches in input side and hence commutation loss in minimized. The half bridge doubler boost converter is implemented with the FSTPI fed induction motor and performances have been observed. From the simulation results, the input power factor has been observed to be 0.9998 compared to a value of 0.996 in the case of the existing PFC converter with compound active clamping. The result shows that the efficiency of induction motor has improved to 98% compared to the existing converter which has only 97.7% of efficiency. From the result the THD is observed to be 1.84%. The THD is reduced much lower than the existing converter which has a value of 3.1%. The performance comparison shows that the designed converter provides better performance than the existing PFC converter with compound active clamping converter.