CHAPTER 3

ANALYSIS AND VALIDATION OF LCC TOPOLOGIES

3.1 INTRODUCTION

In this chapter, various methods of analysing a resonant converter are presented and their pros and cons are compared. Based on the results of comparison of all available methods, fundamental harmonic approximation (FHA) technique is selected to analyse all the candidate LCC topologies. Mathematical expression for voltage gain that can be obtained from each topology is derived. The derived expressions are validated using simulation results.

3.2 METHODS OF ANALYSIS

There are several methods to model and analyse the performance of resonant converters of all nature and type. All these methods have been successfully applied to analyse resonant converters and are well documented in the literature. Some of the methods reported are

a) Fundamental Harmonic Approximation (FHA) or Fundamental Frequency Approximation (FFA) or AC analysis (Steigerwald 1988)

b) State-Plane analysis (Bhat et al 1991)

c) Discrete Time Domain analysis (Agarwal et al 1995)
d) Cyclic Averaging method (Foster et al 2003)

e) Extended Fundamental Frequency Analysis (EFFA) (Forsyth et al 2003).

Generally, the preferred attributes of a particular method are its mathematical simplicity, ability to provide insight into required details, ease of practical implementation, less time consuming or faster to solve and accuracy. All the methods mentioned above possess some attributes and lack some other attributes. Based on the application requirement, a choice is made in favour of one particular method of analysis (Alexander Bucher et al 2008). Table 3.1 gives a detailed account on the advantages and disadvantages of all the available methods.

**Table 3.1 Details of various methods of analysis**

<table>
<thead>
<tr>
<th>Name of the method</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Analysis</td>
<td>Simple, less computation time</td>
<td>Slightly inaccurate beyond resonant frequency</td>
</tr>
<tr>
<td>State plane analysis</td>
<td>Gives geometrical state-plane trajectories, easier to design</td>
<td>Complicated analysis</td>
</tr>
<tr>
<td>Discrete time domain analysis</td>
<td>Easily used for discrete control</td>
<td>Sampling is required, complicated analysis</td>
</tr>
<tr>
<td>Cyclic averaging method</td>
<td>Extension of state space analysis</td>
<td>State space model for each cycle has to be obtained</td>
</tr>
<tr>
<td>EFFA</td>
<td>Extension of AC analysis, accurate</td>
<td>Accurate only after resonant frequency, more computation time</td>
</tr>
</tbody>
</table>

Recently, EFFA has been applied to obtain more accurate results compared to FHA. However, when the converter is operated below the
resonant frequency, both EFFA and conventional FHA methods produce almost similar results. The difference is significant only at resonant frequency and region beyond the resonant frequency. Because of this reason, researchers continue to use conventional FHA method to analyse and design resonant converters (Xiaodong Li and Bhat 2008). Hence, in this thesis, FHA method is used to obtain the required performance parameters.

3.3 AC ANALYSIS METHOD

In AC analysis method, the power flow from input to output is assumed to be contributed only due to the fundamental component. The harmonic components will be filtered by the resonant tank elements and hence do not contribute to power flow. However, the load resistance connected at the output terminals will not be the actual resistance seen by the resonant tank network. Depending upon the nature of voltage and current (square or sine wave), the equivalent AC resistance seen by the resonant tank can be computed. The concept of AC analysis method is explained for a SPRC because it resembles closely with the candidate topologies.

Figure 3.1 illustrates the derivation of equivalent AC resistance to be used in loading the resonant circuit by using AC analysis method. The PRCs and SPRCs use an inductive output filter and drive the rectifier with an equivalent voltage source (i.e. low impedance source provided by the resonant capacitor). A square wave of current is drawn by the rectifier and its fundamental component must be used in arriving at an equivalent AC resistance.
The output voltage $V_o$ is given by

$$V_o = \frac{1}{\pi} \int_0^\pi V_p \sin \omega t \, d(\omega t) = \frac{2V_p}{\pi} = \frac{2\sqrt{2}}{\pi} V_{ac\,(RMS)}$$

(3.1)

Rearranging Equation (3.1), we get

$$V_{ac\,(RMS)} = \frac{\pi}{2\sqrt{2}} V_o$$

(3.2)

From Fourier’s series, the RMS value of fundamental component of current is given by

$$I_1 = I_{ac\,(RMS)} = \frac{\sqrt{2}}{\sqrt{2}\pi} I_o = \frac{2\sqrt{2}}{\pi} I_o$$

(3.3)

From Equations (3.2) and (3.3), the AC equivalent resistance $R_{ac}$ is given by

$$R_{ac} = \frac{V_{ac\,(RMS)}}{I_{ac\,(RMS)}} = \frac{\sqrt{2}V_o}{2\sqrt{2}I_o} = \frac{\pi^2}{8} R_L$$

(3.4)

Thus, classical AC analysis technique can be used to investigate the characteristics of the resonant converters by taking the fundamental
components of all waveforms and by loading the resonant circuits with an equivalent resistance which takes into account the nonlinear behaviour of the output rectifiers.

### 3.4 MATHEMATICAL ANALYSIS AND VALIDATION OF LCC TOPOLOGIES

The shortlisted candidate LCC topologies have to be analysed if they can provide the required voltage gain of 2 and possess good load regulation. Voltage gain expressions for all the topologies have to be derived and validated by using simulation.

The voltage gain of the resonant tank is defined as

\[ M = \frac{V_o}{V_d} \]  

(3.5)

The resonant frequency and the normalized switching frequency are given by

\[ \omega_o = \frac{1}{\sqrt{LC}} \quad \text{and} \quad \omega_n = \frac{\omega}{\omega_o} \]  

(3.6)

Equation (3.7) gives the characteristic impedance \( Z_n \) and quality factor \( Q \) of the resonant network.

\[ Z_n = \sqrt{\frac{L}{C}} \quad \text{and} \quad Q = \frac{\omega_o L}{R} = \frac{Z_n}{R_L} \]  

(3.7)

Figure 3.2 shows the circuit that is used to derive the voltage gain of topology 1.
Figure 3.2 Circuit to derive voltage gain of topology 1

Voltage gain $M$ is given by

$$M = \frac{V_o}{V_d} = \frac{I_o R_{ac}}{V_d} \quad (3.8)$$

Output current $I_o$ is obtained from basic circuit theory and is given by

$$I_o = I_{in} \left( \frac{1}{sC_1} + \frac{1}{sC_2} + R_{ac} \right) \frac{\left( \frac{V_d}{Z_{in}} \right) \times \frac{1}{sC_1}}{\left( \frac{1}{sC_1} + \frac{1}{sC_2} + R_{ac} \right)} \frac{V_d \times sC_2}{Z_{in} \times \left( sC_1 + sC_2 + s^2C_1C_2R_{ac} \right)} \right) \quad (3.9)$$

Input impedance as seen by the source $Z_{in}$ can be found as

$$Z_{in} = \left( \frac{R_{ac} + \frac{1}{sC_2}}{sC_2} \right) + sL \quad (3.10)$$

Simplifying Equation (3.10), input impedance becomes

$$Z_{in} = \frac{1 + sC_2 R_{ac} + s^2L C_1 + s^2L C_2 + s^3L C_1 C_2 R_{ac}}{sC_1 + sC_2 + s^2C_1 C_2 R_{ac}} \quad (3.10a)$$
Substituting Equation (3.10a) in Equation (3.9),

\[
I_o = \frac{V_o \times sC_2}{1 + sC_2R_{ac} + s^2LC_1 + s^2LC_2 + s^3LC_1C_2R_{ac}} \tag{3.11}
\]

Substituting Equation (3.11) in Equation (3.8), voltage gain is computed and is given as

\[
M = \frac{sC_2R_{ac}}{1 + sC_2R_{ac} + s^2LC_1 + s^2LC_2 + s^3LC_1C_2R_{ac}} \tag{3.12}
\]

Substituting \( s = j\omega \) and by using Equations (3.4)-(3.7), voltage gain \( M \) can be simplified and is given by

\[
M = \frac{j\pi^2\omega_n x}{8Q} \frac{1}{1 - \omega_n^2(1 + x) + j\frac{\pi^2\omega_n x}{8Q}(1 - \omega_n^2)} \tag{3.13}
\]

The ratio of resonant capacitances \( C_1 \) to \( C_2 \) is defined as \( x \).

The voltage gain is plotted with the normalised frequency \( \omega_n \) as the variable parameter and taking \( x = 1 \). Figure 3.3 shows the voltage gain plot obtained from Equation (3.13). It is observed that at the normalised frequency of \( \omega_n = 0.7 \), the voltage gain is 2. Further, the voltage gain remains constant at 2 for all values of loaded quality factor \( Q \). Thus, it can be concluded that topology 1 provides the required load voltage regulation also and meets the load requirements.

The validation plot obtained by simulating the LCC circuit using PSpice is shown in Figure 3.4. It is observed that the theoretical voltage gain plot matches with the PSpice simulation plot very closely. This proves the
validity and correctness of the method used in deriving the voltage gain expression. Voltage gain expressions for the remaining topologies are derived and validated similarly.

Figure 3.3 Voltage gain plot of topology 1

Figure 3.4 Voltage gain plot of topology 1 obtained from simulation
Figure 3.5 shows the circuit of topology 2 from which voltage gain expression is derived.

**Figure 3.5 Circuit to derive voltage gain of topology 2**

Voltage gain $M$ is given by Equation (3.8). Output current is given by

$$I_o = I_{in} \frac{sL}{sL + \frac{1}{sC_2} + R_{ac}} \times \frac{\left( \frac{V_d}{Z_{in}} \right) \times sL}{sL + \frac{1}{sC_2} + R_{ac}} \times \frac{V_d \times sL \times sC_2}{Z_{in} \times \left( 1 + sC_2 R_{ac} + s^2 L C_2 \right)}$$  \hspace{1cm} (3.14)

Substituting Equation (3.14) in Equation (3.8),

$$M = \frac{I_o R_{ac} V_d}{V_d} \times \frac{V_d \times sL \times sC_2}{1 + sC_2 R_{ac} + s^2 L C_2} \times \frac{1}{Z_{in}} \times \frac{R_{ac}}{V_d}$$  \hspace{1cm} (3.15)

Simplifying Equation (3.15), voltage gain is given by

$$M = \frac{R_{ac} \times sL \times sC_2}{1 + sC_2 R_{ac} + s^2 L C_2} \times \frac{1}{Z_{in}}$$  \hspace{1cm} (3.16)

Input impedance as seen by the source $Z_{in}$ can be found as

$$Z_{in} = \left[ \left( R_{ac} + \frac{1}{sC_2} \right) sL \right] + \frac{1}{sC_1}$$  \hspace{1cm} (3.17)
Simplifying Equation (3.17),

\[ Z_{in} = \frac{1 + sC_2 R_{ac} + s^2 L C_1 + s^2 L C_2 + s^3 L C_1 C_2 R_{ac}}{sC_1 + s^2 C_1 C_2 R_{ac} + s^3 L C_1 C_2} \]  

(3.18)

Substituting Equation (3.18) in Equation (3.16), voltage gain becomes

\[ M = \frac{sL \times sC_2 \times R_{ac}}{1 + sC_2 R_{ac} + s^2 L C_2} \times \frac{sC_1 + s^2 C_1 C_2 R_{ac} + s^3 L C_1 C_2}{1 + sC_2 R_{ac} + s^2 L C_1 + s^2 L C_2 + s^3 L C_1 C_2 R_{ac}} \]  

(3.19)

Simplifying Equation (3.19), voltage gain is given by

\[ M = \frac{s^3 L C_1 C_2 R_{ac}}{1 + sC_2 R_{ac} + s^2 L C_1 + s^2 L C_2 + s^3 L C_1 C_2 R_{ac}} \]  

(3.20)

Substituting \( s = j \omega \) and \( R_{ac} \) in Equation (3.20),

\[ M = \frac{-j \omega^3 L C_1 C_2 \frac{\pi^2}{8} R_L}{1 + j \omega C_2 \frac{\pi^2}{8} R_L - \omega^2 L C_1 - \omega^2 L C_2 - j \omega^3 L C_1 C_2 \frac{\pi^2}{8} R_L} \]  

(3.21)

Simplifying Equation (3.21) by using Equations (3.4)-(3.7),

\[ M = \frac{-j \frac{\pi^2}{8} \omega^3 x}{1 + j \frac{\pi^2}{8} \frac{\omega^2 x}{Q} - \omega^2 x - j \frac{\pi^2}{8} \frac{\omega^3 x}{Q}} \]  

(3.22)

Rearranging and simplifying Equation (3.22), voltage gain is given by

\[ M = \frac{1}{1 - \frac{1}{\omega_n} + \frac{8}{\pi^2} \frac{Q}{\omega_n x} \left[ \frac{1}{\omega_n^2} - (1 + x) \right]} \]  

(3.23)
Figures 3.6 and 3.7 show the voltage gain plots obtained from theoretical analysis and simulation respectively. Since settling time is involved in simulation, the initial portions in the simulated plot seem to be slightly deviated. However, in both these plots, the value of voltage gain remains constant around 1.2 near a normalised frequency of 0.8 and the peak value occurs at a normalised frequency of 1.0. Since the voltage gain is not sufficient, topology 2 is not suitable for the chosen application.

![Figure 3.6 Voltage gain plot of topology 2](image-url)
Figure 3.7 Voltage gain plot of topology 2 obtained from simulation

Figure 3.8 shows the circuit of topology 3. The voltage gain $M$ is obtained from basic circuit theory as shown below.

\[
\begin{align*}
I_o &= I_{in} \left( \frac{1}{sC_2} + \frac{1}{sC_2} + R_{ac} \right) = \left( \frac{V_d}{Z_{in}} \right) \times \frac{1}{sC_2} = \frac{V_d}{1 + sC_2 R_{ac} + s^2LC_2} \times \frac{1}{Z_{in}} \\
Z_{in} &= \left[ (R_{ac} + sL) \left( \frac{1}{sC_2} \right) + \frac{1}{sC_1} \right]
\end{align*}
\]
Simplifying Equation (3.25),

\[ Z_{in} = \frac{1 + sC_1R_{ac} + sC_2R_{ac} + s^2LC_1 + s^2LC_2}{sC_1 + s^2C_1C_2R_{ac} + s^3LC_1C_2} \]  \( (3.26) \)

Substituting Equation (3.26) in Equation (3.24),

\[ I_o = \frac{V_d}{1 + sC_2R_{ac} + s^2LC_2} \times \frac{sC_1 + s^2C_1C_2R_{ac} + s^3LC_1C_2}{1 + sC_1R_{ac} + sC_2R_{ac} + s^2LC_1 + s^2LC_2} \]  \( (3.27) \)

Simplifying Equation (3.27), output current is given by

\[ I_o = \frac{V_dsC_1}{1 + sC_1R_{ac} + sC_2R_{ac} + s^2LC_1 + s^2LC_2} \]  \( (3.28) \)

Substituting Equation (3.28) in Equation (3.8), voltage gain becomes

\[ M = \frac{I_oR_{ac}}{V_d} = \frac{sC_1R_{ac}}{1 + sC_1R_{ac} + sC_2R_{ac} + s^2LC_1 + s^2LC_2} \]  \( (3.29) \)

Substituting \( s = j\omega \) and \( R_{ac} \) in Equation (3.29), the voltage gain \( M \) becomes

\[ M = \frac{j\omega C_1\frac{\pi^2}{8}R_L}{1 + j\omega C_1\frac{\pi^2}{8}R_L + j\omega C_2\frac{\pi^2}{8}R_L - \omega^2LC_1 - \omega^2LC_2} \]  \( (3.30) \)

Simplifying Equation (3.30), voltage gain is given by

\[ M = \frac{j\frac{\pi^2}{8}\frac{\omega_n}{Q}}{1 + j\frac{\pi^2}{8}\frac{\omega_n}{Q}(1 + x) - \omega_n^2(1 + x)} \]  \( (3.31) \)
Figures 3.9 and 3.10 show the voltage gain plots obtained from theoretical analysis and simulation respectively. It is observed that the voltage gain is only 0.5 which is not sufficient for the chosen application.
Figure 3.11 shows the circuit diagram for topology 4 and will be used to derive the voltage gain of topology 4.

![Figure 3.11 Circuit to derive voltage gain of topology 4](image)

Voltage gain $M$ is given by

$$M = \frac{V_o}{V_d} = \frac{I_o R_{ac}}{V_d} = \frac{I_{in} R_{ac}}{V_d} = \frac{V_d}{Z_{in}} \times \frac{R_{ac}}{V_d} = \frac{R_{ac}}{Z_{in}}$$  \hspace{1cm} (3.32)

Input impedance as seen by the source $Z_{in}$ can be found as

$$Z_{in} = \left[ \left( \frac{1}{sC_1} + \frac{1}{sC_2} \right) \right] + R_{ac}$$  \hspace{1cm} (3.33)

Simplifying Equation (3.33), input impedance is given by

$$Z_{in} = \frac{1 + sC_1 R_{ac} + sC_2 R_{ac} + s^2 L C_1 + s^3 L C_1 C_2 R_{ac}}{sC_1 + sC_2 + s^2 L C_1 C_2}$$  \hspace{1cm} (3.34)

Substituting Equation (3.34) in Equation (3.32),

$$M = \frac{R_{ac}}{Z_{in}} = \frac{(sC_1 + sC_2 + s^3 L C_1 C_2) \times R_{ac}}{1 + sC_1 R_{ac} + sC_2 R_{ac} + s^2 L C_1 + s^3 L C_1 C_2 R_{ac}}$$  \hspace{1cm} (3.35)
Substituting \( s = j\omega \) and \( R_{ac} \) in Equation (3.35),

\[
M = \frac{j\omega C_1 \frac{\pi^2}{8} R_L + j\omega C_2 \frac{\pi^2}{8} R_L - j\omega^3 L C_1 C_2 \frac{\pi^2}{8} R_L}{1 + j\omega C_1 \frac{\pi^2}{8} R_L + j\omega C_2 \frac{\pi^2}{8} R_L - \omega^2 L C_1 - j\omega^3 \frac{\pi^2}{8} L C_1 C_2 R_L}
\]  

(3.36)

Simplifying Equation (3.36), voltage gain is given by

\[
M = \frac{j \frac{\pi^2}{8} \frac{\omega_n}{Q} (1 + x - \omega_n^2 x)}{1 - \omega_n^2 + j \frac{\pi^2}{8} \frac{\omega_n}{Q} (1 + x - \omega_n^2 x)}
\]  

(3.37)

Equation (3.37) can further be simplified and rewritten as

\[
M = \frac{1 + x - \omega_n^2 x}{1 + x - \omega_n^2 x - j \frac{8Q}{\pi^2 \omega_n} (1 - \omega_n^2)}
\]  

(3.38)

The voltage gain plots of topology 4 obtained using theoretical analyses and validated using simulation are shown in Figures 3.12 and 3.13 respectively. It is observed that the voltage gain is 1 at a normalised frequency of 1. This voltage gain is not sufficient to meet the load requirement. Further, the voltage gain reduces closer to zero at a normalised frequency of around 1.4.

The voltage gain \( M \) of topology 5 can be obtained from the circuit shown in Figure 3.14. Voltage gain \( M \) is given by

\[
M = \frac{V_e}{V_d} = \frac{I_e R_{ac}}{V_d} = \frac{I_{ie} R_{ac}}{V_d} = \frac{V_d}{Z_{in}} \times \frac{R_{ac}}{V_d} = \frac{R_{ac}}{Z_{in}}
\]  

(3.39)
Figure 3.12 Voltage gain plot of topology 4

Figure 3.13 Voltage gain plot of topology 4 obtained from simulation
Figure 3.14 Circuit to derive voltage gain of topology 5

Input impedance as seen by the source $Z_{in}$ can be found as

$$Z_{in} = \frac{1}{sC_1} + \left( \frac{1}{sC_2} || sL \right) + R_{ac}$$  \hspace{1cm} (3.40)

Simplifying Equation (3.40), input impedance is given by

$$Z_{in} = \frac{1 + sC_1 R_{ac} + s^2 L C_1 + s^2 L C_2 + s^3 L C_1 C_2 R_{ac}}{sC_1 + s^3 L C_1 C_2}$$  \hspace{1cm} (3.41)

Substituting Equation (3.41) in Equation (3.39), voltage gain becomes

$$M = \frac{R_{ac}}{Z_{in}} = \frac{(sC_1 + s^3 L C_1 C_2) \times R_{ac}}{1 + sC_1 R_{ac} + s^2 L C_1 + s^2 L C_2 + s^3 L C_1 C_2 R_{ac}}$$  \hspace{1cm} (3.42)

Substituting $s = j\omega$ and $R_{ac}$ in Equation (3.42), voltage gain will be

$$M = \frac{j\omega C_1\pi^2}{8 R_L} - j\omega^3 L C_1 C_2 \frac{\pi^2}{8 R_L}$$

$$M = \frac{1 + j\omega C_1\pi^2}{8 R_L} - \omega^2 L C_1 - \omega^2 L C_2 - j\omega^3 \frac{\pi^2}{8 L C_1 C_2 R_L}$$  \hspace{1cm} (3.43)

Simplifying Equation (3.43), voltage gain becomes

$$M = \frac{j\pi^2 \omega_n (1 - \omega_n^2 x)}{1 - \omega_n^2 (1 + x) + j\frac{\pi^2}{8} \omega_n (1 + x - \omega_n^2 x)}$$  \hspace{1cm} (3.44)

The theoretical and simulated voltage gain plots are shown in Figures 3.15 and 3.16 respectively. It is observed that topology 5 also does not provide the load voltage gain requirement. Further, the effect of transients
in simulation can be easily seen in Figure 3.16 though the key points of interest match exactly with the theoretical analysis. Thus, the validity of the theoretical analysis is once again proved.

Figure 3.15 Voltage gain plot of topology 5

Figure 3.16 Voltage gain plot of topology 5 obtained from simulation

For topology 6, the circuit shown in Figure 3.17 is used to derive the expression for voltage gain $M$ which is given by Equation (3.8).
Output current is given by

\[
I_o = I_{in} \left( \frac{sL + \frac{1}{sC_2}}{sL + \frac{1}{sC_2} + R_{ac}} \right) \frac{V_d}{Z_{in}} \times \frac{1 + s^2LC_2}{1 + sC_2R_{ac} + s^2LC_2} \quad (3.45)
\]

Input impedance as seen by the source \(Z_{in}\) can be found as

\[
Z_{in} = \frac{1}{sC_1} + \left( R_{ac} \right) \left( sL + \frac{1}{sC_2} \right) \quad (3.46)
\]

Simplifying Equation (3.46),

\[
Z_{in} = \frac{1 + sC_1R_{ac} + sC_2R_{ac} + s^2LC_2 + s^3LC_1C_2R_{ac}}{sC_1 + s^2C_1C_2R_{ac} + s^3LC_1C_2} \quad (3.47)
\]

Substituting Equation (3.47) in Equation (3.45),

\[
I_o = \frac{V_d \left( 1 + s^2LC_2 \right)}{1 + sC_2R_{ac} + s^2LC_2} \times \frac{sC_1 + s^2C_1C_2R_{ac} + s^3LC_1C_2}{1 + sC_1R_{ac} + sC_2R_{ac} + s^2LC_2 + s^3LC_1C_2R_{ac}} \quad (3.48)
\]
Simplifying Equation (3.48), output current is given by

\[ I_o = \frac{V_d \times \left(1 + s^2LC_2\right)sC_1}{1 + sC_1R_{ac} + sC_2R_{ac} + s^2LC_2 + s^3LC_1C_2R_{ac}} \] (3.49)

Substituting Equation (3.49) in Equation (3.8), voltage gain will be

\[ M = \frac{I_o \cdot R_{ac}}{V_d} = \frac{sC_1R_{ac} \times \left(1 + s^2LC_2\right)}{1 + sC_1R_{ac} + sC_2R_{ac} + s^2LC_2 + s^3LC_1C_2R_{ac}} \] (3.50)

Substituting \( s = j\omega \) and \( R_{ac} \) in Equation (3.50),

\[ M = \frac{j\omega C_1 \frac{\pi^2}{8} R_L - j\omega^3 L C_1 C_2 \frac{\pi^2}{8} R_L}{1 + j\omega C_1 \frac{\pi^2}{8} R_L + j\omega C_2 \frac{\pi^2}{8} R_L - \omega^3 L C_2 - j\omega^3 \frac{\pi^2}{8} L C_1 C_2 R_L} \] (3.51)

Simplifying Equation (3.51), voltage gain is given by

\[ M = \frac{j \frac{\pi^2}{8} \omega_n \left(1 - \omega_n^2 x\right)}{1 - \omega_n^2 x + j \frac{\pi^2}{8} \omega_n \left(1 + x - \omega_n^2 x\right)} \] (3.52)

Figures 3.18 and 3.19 show the theoretical and simulated voltage gain plots respectively. It is observed that topology 6 also does not provide the load voltage gain requirement and cannot be used for the proposed application.
Figure 3.18 Voltage gain plot of topology 6

Figure 3.19 Voltage gain plot of topology 6 obtained from simulation

From the circuit shown in Figure 3.20 for topology 7, the voltage gain is derived as shown below.
Output current is given by

\[
I_o = I_{in} \frac{1}{sC_1} + \left( \frac{sL}{sC_2} \right) + \frac{1}{sC_1} + \left( \frac{sL}{sC_2} \right) + R_{ac} \tag{3.53}
\]

Simplifying Equation (3.53), output current will become

\[
I_o = \frac{V_{in} \times (1 + s^2LC_1 + s^3LC_2)}{Z_{in} \times 1 + sC_1R_{ac} + s^2LC_1 + s^2LC_2 + s^3LC_1C_2R_{ac}} \tag{3.54}
\]

Input impedance as seen by the source \( Z_{in} \) can be found as

\[
Z_{in} = R_{ac} \left[ \frac{1}{sC_1} + \frac{sL}{1 + s^3LC_2} \right] \tag{3.55}
\]

Simplifying Equation (3.55), input impedance is given by

\[
Z_{in} = \frac{R_{ac} \times (1 + s^2LC_1 + s^2LC_2)}{1 + sC_1R_{ac} + s^2LC_1 + s^2LC_2 + s^3LC_1C_2R_{ac}} \tag{3.56}
\]
Substituting Equation (3.56) in Equation (3.54) and simplifying,

\[ I_o = \frac{V_d}{R_{ac}} \]  

(3.57)

Substituting Equation (3.57) in Equation (3.8), voltage gain becomes

\[ M = \frac{I_o R_{ac}}{V_d} = 1 \]  

(3.58)

Since the entire resonant network and AC equivalent resistance \( R_{ac} \) is in parallel with the input, the total available input potential is dropped across this network. Hence, voltage gain is 1 irrespective of change in frequency and load conditions. In other words, as the resonant network exists in parallel with the input and load, the voltage gain is always 1. Figure 3.21 shows the simulated voltage gain plot which justifies the hypothesis. Since a voltage gain of 2 is required, topology 7 cannot be used.

![Figure 3.21 Voltage gain plot of topology 7 obtained from simulation](image)

The circuit for topology 8 is shown in Figure 3.22 which is used to derive the expression for voltage gain.
Figure 3.22 Circuit to derive voltage gain of topology 8

Output current is given by

\[ I_o = I_{in} \frac{sL + \frac{1}{sC_1}}{sL + \frac{1}{sC_1} + \frac{1}{sC_2} + R_{ac}} \frac{V_d}{Z_{in}} \times \frac{1 + s^2LC_1}{1 + sC_1R_{ac} + s^2LC_1 + \frac{C_1}{C_2}} \]  

(3.59)

Input impedance as seen by the source \( Z_{in} \) can be found as

\[ Z_{in} = \left( R_{ac} + \frac{1}{sC_2} \right) \left( \frac{1}{sC_1} + sL \right) = \frac{(1 + sC_2R_{ac}) \times (1 + s^2LC_1)}{sC_1 + sC_2 + s^2C_1C_2R_{ac} + s^3LC_1C_2} \]  

(3.60)

Substituting Equation (3.60) in Equation (3.59) and simplifying,

\[ I_o = \frac{V_d \times (sC_2 + s^3LC_1C_2)}{(1 + sC_2R_{ac}) \times (1 + s^2LC_1)} \]  

(3.61)

Substituting Equation (3.61) in Equation (3.8), voltage gain is given as

\[ M = \frac{I_o R_{ac}}{V_d} = \frac{sC_2R_{ac} + s^3LC_1C_2R_{ac}}{1 + sC_2R_{ac} + s^2LC_1 + s^3LC_1C_2R_{ac}} \]  

(3.62)

Substituting \( s = j\omega \) and \( R_{ac} \) in Equation (3.62),

\[ M = \frac{j\omega C_2 \frac{\pi^2}{8} R_L - j\omega^3LC_1C_2 \frac{\pi^2}{8} R_L}{1 + j\omega C_2 \frac{\pi^2}{8} R_L - \omega^2LC_1 - j\omega^3 \frac{\pi^2}{8} LC_1C_2R_L} \]  

(3.63)
Simplifying Equation (3.63), voltage gain becomes

\[ M = \frac{1}{1 - j \frac{8Q}{\pi \omega_n x}} \]  

(3.64)

Figure 3.23 Voltage gain plot of topology 8

Figure 3.24 Voltage gain plot of topology 8 obtained from simulation
Table 3.2 Voltage gain expressions for all topologies

<table>
<thead>
<tr>
<th>Topology</th>
<th>Circuit Diagram</th>
<th>Voltage Gain Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td><img src="image" alt="Circuit Diagram 1" /></td>
<td>[ \frac{j \frac{\pi^2 \omega_n x}{8Q}}{1 - \omega_n^2 (1 + x) + j \frac{\pi \omega_n x}{8Q} (1 - \omega_n^2)} ]</td>
</tr>
<tr>
<td>2</td>
<td><img src="image" alt="Circuit Diagram 2" /></td>
<td>[ \frac{1}{1 - \frac{1}{\omega_n^2} + j \frac{8Q}{\pi \omega_n} \left( \frac{1}{\omega_n^2} - (1 + x) \right)} ]</td>
</tr>
<tr>
<td>3</td>
<td><img src="image" alt="Circuit Diagram 3" /></td>
<td>[ \frac{j \frac{\pi^2 \omega_n}{8Q}}{1 + j \frac{\pi^2 \omega_n}{8Q} (1 + x) - \omega_n^2 (1 + x)} ]</td>
</tr>
<tr>
<td>4</td>
<td><img src="image" alt="Circuit Diagram 4" /></td>
<td>[ \frac{1 + x - \omega_n^2 x}{1 + x - \omega_n^2 x - j \frac{8Q}{\pi \omega_n} (1 - \omega_n^2)} ]</td>
</tr>
<tr>
<td>5</td>
<td><img src="image" alt="Circuit Diagram 5" /></td>
<td>[ \frac{j \frac{\pi^2 \omega_n}{8Q} (1 - \omega_n^2 x)}{1 - \omega_n^2 (1 + x) + j \frac{\pi^2 \omega_n}{8Q} (1 + x - \omega_n^2 x)} ]</td>
</tr>
<tr>
<td>6</td>
<td><img src="image" alt="Circuit Diagram 6" /></td>
<td>[ \frac{j \frac{\pi^2 \omega_n}{8Q} (1 - \omega_n^2 x)}{1 - \omega_n^2 x + j \frac{\pi^2 \omega_n}{8Q} (1 + x - \omega_n^2 x)} ]</td>
</tr>
<tr>
<td>7</td>
<td><img src="image" alt="Circuit Diagram 7" /></td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td><img src="image" alt="Circuit Diagram 8" /></td>
<td>[ \frac{1}{1 - j \frac{8Q}{\pi \omega_n x}} ]</td>
</tr>
</tbody>
</table>
Figures 3.23 and 3.24 show the voltage gain plots of topology 8 that were obtained theoretically and using simulation respectively. It is observed that topology 8 does not provide the required voltage gain of 2 and load voltage regulation. Hence, this topology cannot be used for the chosen application. Table 3.2 shows the voltage gain expressions of all the candidate topologies.

3.5 CONCLUSION

From the voltage gain plots of all the topologies, it is observed that only topology 1 provides the required voltage gain and load voltage regulation. In topology 1, at the normalised frequency of 0.7, voltage gain remains constant at 2 for all load conditions. The remaining topologies do not provide the required voltage gain and hence cannot be used for the chosen automotive application.

The resonant tank elements present in topology 1 have to be designed such that the size of the inductor is minimal. Further, the voltage and current stress of the resonant tank needs to be determined. The design details of the resonant tank elements used in topology 1 are described in Chapter 4.