APPENDIX 1

1N4007

DISCRETE SEMICONDUCTORS

DATA SHEET

1N4001G to 1N4007G
Rectifiers
FEATURES

- Glass passivated
- High maximum operating temperature
- Low leakage current
- Excellent stability
- Available in ammo-pack.

DESCRIPTION

Rugged glass package, using a high temperature alloyed construction. This package is hermetically sealed and fatigue free as coefficients of expansion of all used parts are matched.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VRRM</td>
<td>repetitive peak reverse voltage 1N4001G</td>
<td>-</td>
<td>50</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1N4002G</td>
<td>-</td>
<td>100</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1N4003G</td>
<td>-</td>
<td>200</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1N4004G</td>
<td>-</td>
<td>400</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1N4005G</td>
<td>-</td>
<td>600</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1N4006G</td>
<td>-</td>
<td>800</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1N4007G</td>
<td>-</td>
<td>1000</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VR</td>
<td>continuous reverse voltage 1N4001G</td>
<td>-</td>
<td>50</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1N4002G</td>
<td>-</td>
<td>100</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1N4003G</td>
<td>-</td>
<td>200</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1N4004G</td>
<td>-</td>
<td>400</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS

\[ T_j = 25 \, ^\circ C; \text{ unless otherwise specified.} \]

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_F</td>
<td>forward voltage</td>
<td>( I_F = 1 , A ); see Fig.3</td>
<td>-</td>
<td>1.1</td>
<td>V</td>
</tr>
<tr>
<td>V_F(AV)</td>
<td>full-cycle average forward voltage</td>
<td>( I_F(AV) = 1 , A )</td>
<td>-</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>I_R</td>
<td>reverse current</td>
<td>( V_R = V_{Rmax} )</td>
<td>10</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_R = V_{Rmax}; T_{amb} = 100 , ^\circ C )</td>
<td>50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_R(AV)</td>
<td>full-cycle average reverse current</td>
<td>( V_R = V_{RRMmax}; T_{amb} = 75C )</td>
<td>30</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

### THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{thj-tp}</td>
<td>thermal resistance from junction to tie-point</td>
<td>lead length = 10 mm</td>
<td>46</td>
<td>K/W</td>
</tr>
<tr>
<td>R_{th j-a}</td>
<td>thermal resistance from junction to ambient</td>
<td>note 1</td>
<td>100</td>
<td>K/W</td>
</tr>
</tbody>
</table>

**Note**

1. Device mounted on epoxy-glass printed-circuit board, 1.5 mm thick; thickness of copper ³40 mm, see Fig.4. For more information please refer to the “General Part of associated Handbook”. 
Graphical Data

Package Outline
DEFINITIONS

Data sheet status

- Objective specification: This data sheet contains target or goal specifications for product development.

- Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

- Product specification: This data sheet contains final product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.
APPENDIX 2

ATMEL 8 – BIT MICROCONTROLLER AT89C2051

Features

- Compatible with MCS-51™ Products
- 2K Bytes of Reprogrammable Flash Memory – Endurance: 1,000 Write/Erase Cycles
- 2.7V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Two-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 15 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial UART Channel
- Direct LED Drive Outputs
- On-Chip Analog Comparator
- Low Power Idle and Power Down Modes
Description

The AT89C2051 is a low-voltage, high-performance CMOS 8-bit microcomputer with 2K Bytes of Flash programmable and erasable read only memory (PEROM). The block diagram of Atmel 89C2051 is shown in Figure A.2.1. The Pin Configuration of Atmel 89C2051 is shown in Figure A2.2. The device is manufactured using Atmel’s high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C2051 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

The AT89C2051 provides the following standard features: 2K Bytes of Flash, 128 bytes of RAM, 15 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the AT89C2051 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.
Figure A2.1 Block diagram of Atmel 89C2051
Figure A2.2 Pin Configuration

Pin Description

V CC : Supply voltage

GND : Ground.

Port 1

Port 1 is an 8-bit bidirectional I/O port. Port pins P1.2 to P1.7 provide internal pullups. P1.0 and P1.1 require external pullups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 20 mA and can drive LED displays directly. When 1s are written to Port 1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current (I\text{IL}) because of the internal pullups. Port 1 also receives code data during Flash programming and verification.

Port 3

Port 3 pins P3.0 to P3.5, P3.7 are seven bidirectional I/O pins with internal pullups. P3.6 is hard-wired as an input to the output of the on-chip
comparator and is not accessible as a general purpose I/O pin. The Port 3 output buffers can sink 20 mA. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ($I_{IL}$) because of the pullups. Port 3 also receives some control signals for Flash programming and verification. Port 3 also serves the functions of various special features of the AT89C2051 as listed below:

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3.0</td>
<td>RXD (serial input port)</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD (serial output port)</td>
</tr>
<tr>
<td>P3.2</td>
<td>INT0 (external interrupt 0)</td>
</tr>
<tr>
<td>P3.3</td>
<td>INT1 (external interrupt 1)</td>
</tr>
<tr>
<td>P3.4</td>
<td>T0 (timer 0 external input)</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1 (timer 1 external input)</td>
</tr>
</tbody>
</table>

**RST**

Reset input. All I/O pins are reset to 1s as soon as RST goes high. Holding the RST pin high for two machine cycles while the oscillator is running resets the device. Each machine cycle takes 12 oscillator or clock cycles.

**XTAL1**

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

**XTAL2**

Output from the inverting oscillator amplifier.
APPENDIX 3

PIC16F84A

High Performance RISC CPU Features

- Only 35 single word instructions to learn
- All instructions single cycle except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- 1024 words of program memory
- 68 bytes of data RAM
- 64 bytes of data EEPROM
- 14-bit wide instruction words
- 8-bit wide data bytes
- 15 special function hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
  - External RB0/INT pin
  - TMR0 timer overflow
  - PORTB<7:4> interrupt on change
  - Data EEPROM write complete
Peripheral Features

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25 mA sink max. per pin
  - 25 mA source max. per pin
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler

Special Microcontroller Features:

- 1000 erase/write cycles Enhanced Flash program memory
- 1,000,000 typical erase/write cycles EEPROM data memory
- EEPROM Data Retention > 40 years
- In-Circuit Serial Programming (ICSP™) - via two pins
- Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Code-protection
- Power saving SLEEP mode
- Selectable oscillator options
DEVICE OVERVIEW

This document contains device-specific information for the operation of the PIC16F84A device. The Pin diagram of PIC16F84A is shown in Figure A3.1. The PIC16F84A Pinout description is shown in Table A3.1. Additional information may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023), which may be downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC16F84A belongs to the mid-range family of the PICmicro™ microcontroller devices. A block diagram of the device is shown in Figure 3.2.
The program memory contains 1K words, which translates to 1024 instructions, since each 14-bit program memory word is the same width as each device instruction. The data memory (RAM) contains 68 bytes. Data EEPROM is 64 bytes.

There are also 13 I/O pins that are user-configured on a pin-to-pin basis. Some pins are multiplexed with other device functions. These functions include:

- External interrupt
- Change on PORTB interrupt
- Timer0 clock input

Figure A3.2 Block diagram of PIC16F84A
<table>
<thead>
<tr>
<th>Pin Name</th>
<th>DIP No.</th>
<th>SOIC No.</th>
<th>SSOP No.</th>
<th>I/O/P Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSC1/CLKIN</td>
<td>16</td>
<td>16</td>
<td>18</td>
<td>I</td>
<td>ST/CMOS (3)</td>
<td>Oscillator crystal input/external clock source input.</td>
</tr>
<tr>
<td>OSC2/CLKOUT</td>
<td>15</td>
<td>15</td>
<td>19</td>
<td>O</td>
<td>—</td>
<td>Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.</td>
</tr>
<tr>
<td>MCLR</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>I/P</td>
<td>ST</td>
<td>Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.</td>
</tr>
<tr>
<td>RA0 RA1 RA2</td>
<td>17</td>
<td>17 18</td>
<td>19 20</td>
<td>I/O</td>
<td>TTL TTL TTL ST</td>
<td>PORTA is a bi-directional I/O port. Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.</td>
</tr>
<tr>
<td>RA3 RA4/T0CKI</td>
<td>18 1 23</td>
<td>18 1 23</td>
<td>19 20</td>
<td>I/O</td>
<td>TTL TTL TTL ST</td>
<td>PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. RB0/INT can also be selected as an external interrupt pin. Interrupt on change pin. Interrupt on change pin. Serial programming clock. Interrupt on change pin. Serial programming data.</td>
</tr>
<tr>
<td>RB0/INT RB1 RB2 RB3 RB4 RB5 RB6 RB7</td>
<td>6 7 8 9 10 11 12 13</td>
<td>6 7 8 9 10 11 12 13</td>
<td>7 9 10 11 12 13 14</td>
<td>I/O I/O I/O I/O I/O I/O I/O</td>
<td>TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL/TTL</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>5</td>
<td>5</td>
<td>5,6</td>
<td>P</td>
<td>—</td>
<td>Ground reference for logic and I/O pins.</td>
</tr>
<tr>
<td>VDD</td>
<td>14</td>
<td>14</td>
<td>15,16</td>
<td>P</td>
<td>—</td>
<td>Positive supply for logic and I/O pins.</td>
</tr>
</tbody>
</table>

Legend:  I= input      O = output      I/O = Input/Output      P = power
— = Not used   TTL = TTL input   ST = Schmitt Trigger input
APPENDIX 4

INTERNATIONAL RECTIFIER IR2110

FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +500V or +600V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
- Separate logic supply range from 3.3V to 20V
- Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

\[ V_{\text{OFFSET}} \text{ (IR2110)} \quad 500\text{V max. (IR2113)} \quad 600\text{V max.} \]
\[ I_{\text{O}+/-} \quad 2\text{A / 2A} \]
\[ V_{\text{OUT}} \quad 10 \text{ - } 20\text{V} \]
\[ t_{\text{ON/Off (typ.)}} \quad 120 \& 94 \text{ ns} \]
Delay Matching (IR2110) \quad 10 \text{ ns max. (IR2113)} \quad 20\text{ns max.} \]
Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts. The Functional block diagram of IR2110/IR2113 is shown in Figure A4.1.

Figure A4.1 Functional block diagram
# Lead Definitions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VQD</td>
<td>Logic supply</td>
</tr>
<tr>
<td>HIN</td>
<td>Logic input for high side gate driver output (HO), in phase</td>
</tr>
<tr>
<td>SD</td>
<td>Logic input for shutdown</td>
</tr>
<tr>
<td>LIN</td>
<td>Logic input for low side gate driver output (LO), in phase</td>
</tr>
<tr>
<td>»ss</td>
<td>Logic ground</td>
</tr>
<tr>
<td>VB</td>
<td>High side floating supply</td>
</tr>
<tr>
<td>HO</td>
<td>High side gate drive output</td>
</tr>
<tr>
<td>Vs</td>
<td>High side floating supply return</td>
</tr>
<tr>
<td>»cc</td>
<td>Low side supply</td>
</tr>
<tr>
<td>LO</td>
<td>Low side gate drive output</td>
</tr>
<tr>
<td>COM</td>
<td>Low side return</td>
</tr>
</tbody>
</table>
APPENDIX 5

DESIGN CALCULATIONS OF CONTROL CIRCUIT

DESIGN OF CURRENT LIMITING RESISTANCE

The current limiting resistance is calculated as follows:

\[ I_1 = 4 \text{ mA} \]
\[ I_1 = (V-V_D)/R_1 \]
\[ R_1 = (V-V_D)/I_1 \]
\[ = (5-0.7)/4 \times 10^{-3} \]
\[ = 1 \text{ k}\Omega \]

DESIGN OF CRYSTAL OSCILLATOR

The capacitance of crystal circuit is calculated as follows:

\[ f = 11.05 \text{ MHz} \]
\[ C = 16.5 \text{ pF} \]
\[ f = 1/[2\pi\sqrt{(LC)}] \]
\[ 10 \times 10^6 = 1/(2\pi\sqrt{L \times 16.5 \times 10^{-12}}) \]
\[ L = 15 \mu\text{H} \]

\[ C = C_1C_2/(C_1+C_2) \]
\[ C = C'C'/(C'+C') \]
\[ C = C'/2 \]
\[ C' = 2C \]
\[ = 2 \times 16.5 \text{ pF} \]
\[ = 33 \text{ pF} \]
DESIGN OF DRIVER CIRCUIT

The parameters of driver circuit are given as follows:

\[ T = 3 \text{ ms} \]
\[ R = 100 \Omega \]
\[ T = 2 \pi RC \]
\[ 3 \times 10^{-3} = 2 \pi 100 \text{ C} \]
\[ C = 47 \mu \text{F} \]

\[ R_2 = \frac{(V - V_{gs})}{I_g} \]
\[ = \frac{(10 - 1)}{0.4} \]
\[ = 22.5 \Omega \]

DESIGN OF FILTER

The filter is designed for fifth order harmonics, since the third harmonic is harmless.

\[ f_5 = 5f \]
\[ = 5 \times 50 = 250 \text{ Hz} \]

Let \( C = 2 \mu \text{F} \)

\[ f_5 = \frac{1}{2\pi\sqrt{(LC)}} \]
\[ 250 = \frac{1}{2\pi\sqrt{(L \times 2 \times 10^{-6})}} \]
\[ L = 200 \text{ mH} \]
APPENDIX 6

VOLTAGE TO BE INJECTED

The voltage to be compensated by the DVR is calculated as follows

Resistance of the transmission line $r$/km $= 0.09 \ \Omega$

Inductance of the line $l$/km $= 0.6 \ \text{mH}$

Length of the line $l'$ $= 200 \ \text{km}$

Power rating of the line $P$ $= 900 \ \text{kW}$

Rated voltage $= 11 \ \text{kV}$

Power factor $= 0.8$

Total resistance $R = r \times l \ \Omega$

$= 0.09 \times 200$

$= 18 \ \Omega$

Total Inductance $L = l' \times l \ \text{mH}$

$= 0.6 \times 200$

$= 120 \ \text{mH}$

Inductive Reactance $X_L = 2 \pi f L \ \Omega$

$= 314 \times 0.12$

$= 37.6 \ \Omega$
Total Impedance $Z = \sqrt{R^2 + X^2} \ \Omega$

$= \sqrt{18^2 + 37.6^2}$

$= 41 \ \Omega$

Total current $I = \frac{P}{\sqrt{3} V_1 \cos \varphi} \ \text{A}$

$= \frac{900 \times 10^3}{\sqrt{3} \times 11000 \times 0.8}$

$I = 59 \ \text{A}$

Drop $= IZ$

$= 59 \times 41$

$= 2419$

$= 2.41 \text{kV}$

The voltage to be injected is 2.41 kV

The ratings of transformer and devices are selected by taking a factor of safety of 2.
APPENDIX 7

ASSEMBLY LANGUAGE PROGRAM FOR NINE-LEVEL INVERTER

del equ 0ch
del1 equ 0dh
del2 equ 0eh
org 000h
bsf status,5
movlw 00h
movwf trisb
movlw 00h
movwf trisa
bcf status,5

start: movlw 00h
movwf portb
call dalay1
movlw 44h
movwf portb
call dalay2
movlw 99h
movwf portb
call dalay3
movlw 11h
movwf portb
call dalay4
movlw 55h
movwf portb
call dalay5
movlw 11h
movwf portb
call dalay4
movlw 99h
movwf portb
call dalay3
movlw 44h
movwf portb
call dalay2
movlw 00h
movwf portb
call dalay1
movlw 00h
movwf portb
call dalay1
movlw 88h
movwf portb
call dalay2
movlw 66h
movwf portb
call dalay3
movlw 22h
movwf portb
call dalay4
movlw AAh
movwf portb
call dalay5
movlw 22h
movwf portb
call dalay4
movlw 66h
movwf portb
call dalay3
movlw 88h
movwf portb
call dalay2
movlw 00h
movwf portb
call dalay1
goto start

delay1: movlw 178
movwf dell

loop1: nop
nop
decfsz dell,1
goto loop1
return

delay2: movlw 240
movwf del
loop2: nop
    nop
    decfsz dell,1
    goto loop2
    return

delay3: movlw 290
    movwf del

loop3: nop
    nop
    decfsz dell,1
    goto loop3
    return

delay4: movlw 185
    movwf del

loop4: nop
    nop
    decfsz dell,1
    goto loop4
    return
delay5: movlw  715
       movwf del

loop5: nop
       nop
       decfsz dell,1
       goto loop5
       return

ASSEMBLY LANGUAGE PROGRAM FOR H-BRIDGE INVERTER

Main Program

ORG 000H
       MOV P1, #00H

START: MOV P1, #55H
       call delay1
       MOV P1, #00H
       call delay2
       MOV P1, #0aaH
       call delay1
       MOV P1, #00H
       call delay2
       SJMP START
DELAY SUBROUTINE

delay1:
    MOV r1, #250

loop:   nop
        nop
        djnz r1, loop
        ret

delay2:
    MOV r1, #0ah

loop1:
    djnz r1, loop1
    ret
APPENDIX 8

Various system data like, bus data and line data used for simulation circuits are given below in the following tabular columns.

Table A8.1 Data for 8-bus

<table>
<thead>
<tr>
<th>BUS NO</th>
<th>VOLTAGE</th>
<th>LOAD IMPEDANCE</th>
<th>LINE IMPEDANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Resistance</td>
<td>Inductance</td>
</tr>
<tr>
<td>1</td>
<td>6350</td>
<td>R1 3Ω</td>
<td>L1 10mH</td>
</tr>
<tr>
<td>2</td>
<td>-</td>
<td>R8 100Ω</td>
<td>L8 50mH</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
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<td>L11 50mH</td>
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### Table A8.2 Regulation constants for H.T. O.H. lines using various conductors at 50 c/s per 100 kVA per km 11 kV lines

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<tr>
<th>Sl No.</th>
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<th>Commercial Name</th>
<th>Resistance at 40°C Ω/Km</th>
<th>Resistance Ω/Km</th>
<th>POWER FACTOR</th>
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<th>0.55</th>
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<th>0.65</th>
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<th>0.85</th>
<th>0.90</th>
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<td></td>
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<td>0.0806</td>
<td>0.0844</td>
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### Table A8.3 Data for 22 KV lines

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<th>Phase to phase Voltage</th>
<th>Equivalent Copper area sq.mm</th>
<th>Equivalent spacing in metre</th>
<th>Resistance at 40°C Ohms/K.M.</th>
<th>Resistance Ohms/K.M.</th>
<th>Regulation of constant in percentage for a Power Factor of</th>
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<td>0.8 lag</td>
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Table A8.5 Data for 66 kV lines

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<th>Equivalent spacing of conductors in meters (ft.)</th>
<th>Resistance at 40°C Ω/Km</th>
<th>Percentage Regulation at lagging Power Factor</th>
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## Table A8.6 Data for 110 KV lines

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<th>Equivalent Copper area in mm²</th>
<th>Resistance at 40°C Ω/Km</th>
<th>Equivalent spacing of conductors in meters (ft.)</th>
<th>Percentage Regulation at lagging Power Factor</th>
<th>Power Factor</th>
</tr>
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<td>0.00042 0.00038 0.00025</td>
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