CHAPTER 3

EFFECT OF STRUCTURAL AND DOPING PARAMETER VARIATIONS ON $f_t$, NQS DELAY, INTRINSIC GAIN AND NF IN N-TYPE FINFETS

In this chapter, the effect of structural and doping parameter variations on $f_t$, NQS delay, intrinsic gain and NF in 30 nm gate length FinFET have been studied qualitatively by performing extensive TCAD simulations. The quantitative study is done by performing a simple sensitivity experiment as well as through Plackett-Burman’s DOE approach. The individual and overall ranking for the parameters are given.

3.1 INTRODUCTION

Even though initially, many double gate devices were suggested in the area of multi-gate transistors, double gate FinFETs are considered as a serious contender for channel scaling. Because of their quasi-planar structure they are compatible with the existing CMOS technology. The current flow in the channel is parallel to the plane of the wafer, and thus the label quasi-planar despite what appears to be a non-planar fin (Swahn and Hassoun 2006). FinFET originally dubbed as the folded-channel MOSFET promises self-alignment of the double gates (Hisamoto et al 1998). Abundant literatures are available on FinFETs (Chang et al 2000; Tang et al 2001; Ortiz-Conde and Garcia-Sanchez 2003; Yang et al 2007). Since, these devices use ultrathin bodies as their channel, suppression of SCEs can be achieved with undoped channels instead of the usual high doping density channels. The absence of
dopant atoms in the channel reduces the mobility degradation by eliminating impurity scattering and avoiding random microscopic dopant fluctuations (Ortiz-Conde and Garcia-Sanchez 2007). FinFETs have high current drive and offer substantially better control over leakage and short channel effects (Swahn and Hassoun 2008).

Figure 3.1 depicts the typical structure of a FinFET. Like a traditional MOSFET, FinFET is composed of a channel, a source, a drain and a gate. The channel is embodied in a fin protruding out of the wafer plane. There is a dielectric layer called the hard mask on top of the silicon fin. The hard mask is to prevent the formation of parasitic inversion channels at the top corners of the device (Colinge 2008). The fin is fabricated out of either undoped or lightly doped silicon. The gates of the FinFET are created by wrapping the gate material around the three sides of the silicon fin, resulting in self-aligned front and back gates.

Figure 3.1: FinFET Structure
From a circuit perspective, double gate MOSFETs (FinFETs) operate in a manner similar to MOSFETs. When a potential larger than the threshold voltage ($V_T$) is applied between the gates of the double gate device and source, current flows from the drain to source. The double gates, however, allow modulating the channel from two sides instead one. The two gates together strongly influence the channel potential, reducing the drain impact and leading to the better ability to switch off the channel current. DIBL is thus reduced and the sub-threshold swing is improved (Swahn and Hassoun 2006).

FinFET-based digital building blocks are explored in the literature abundantly. For example FinFET-based SRAM cells have been studied (Tawfik et al 2007; Kang et al 2010). Like MOSFET, FinFET should also be characterized for their process variations and it is studied (Xiong and Boker 2003; Choi et al 2007; Khan et al 2008; Thakker et al 2010). Long term reliability issues like negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), etc. are studied by Vita et al (2011). Low field mobility of these devices has been explored (Gamiz et al 1999; Uchida et al 2003; Khakifirooz and Antoniadis 2004).

FinFET-based analog building blocks/RF receivers have also been investigated extensively (Knoblinger et al 2007; Siprak et al 2009). RF performance of FinFETs is studied (Wambacq et al 2006; Parvias et al 2007; Lederer et al 2009; Lin et al 2011). In the above mentioned literature, the effect of fin width on $f_i$ and maximum frequency of oscillation ($f_{max}$) has been investigated. The source/drain series resistance in FinFETs largely limits the device RF performance, and the losses due to the gate resistance increases with reducing gate length. Nuttinck et al (2007) has studied about the source/drain resistance impact on RF performance. A systematic sensitivity analysis of FinFET RF performance is missing presently.
In this chapter, nine different geometrical parameters and two doping related parameters of FinFET are varied over a wide range to study their effect on $f_t$, NQS delay, intrinsic gain and noise figure. Following this, the various parameters are ranked by performing sensitivity analysis and PB DOE approach. The outline of this chapter is as follows. Next section deals with the description and calibration of the device. Section 3.3 explains about the parameter space for the wide range study. Section 3.4 discusses the simulation results. Finally in Section 3.5 conclusions are given.

### 3.2 DEVICE DESCRIPTION AND CALIBRATION

The effect of process parameters, gate length ($L_g$), underlap ($L_{un}$), fin width ($W$), gate oxide thickness ($T_{ox}$), channel doping ($N_{ch}$), and source/drain doping ($N_{SD}$) on $f_t$ are studied with the 2D simulations. Some of the parameters like fin height ($H$), source/drain cross-sectional area, fin taper angle, corner radius and hard mask height ($HM$) cannot be studied with 2D simulations. So these parameters are studied with 3D simulations.

Figure 3.2 shows the 2D structure of the FinFET. The 3D device structure is shown in Figure 3.3(a). Figure 3.3(b) shows a 2D cut of the above 3D structure which depicts the fin cross section i.e. in Figure 3.3(b) source to drain axis runs perpendicular to the page. Figure 3.3(c) depicts the cross-sectional view from the side of the FinFET device with gate oxide removed. Figure 3.4 is a 2D schematic diagram which shows various parameters of this study and the parameters related to 3D simulation are shown in Figure 3.3(b).
Figure 3.2: 2D structure of FinFET
Figure 3.3: (a) 3D structure of FinFET (b) Enlarged portion of the rounded region (c) Cross-sectional view from the side of FinFET
Figure 3.4: Schematic of 2D structure of FinFET
3.2.1 Calibration

The simulator is calibrated against the published results on FinFETs (Sabry et al. 2009). For the doped materials, the carriers will normally scatter with the impurities leading to the degradation of mobility. So tuning of the parameter file is done mainly in doping dependent mobility models. For the doping dependent mobility model, we have used Lombardi model with calibrated parameters in the silicon parameter file. The Lombardi model takes into account of the surface contribution due to phonon scattering and surface scattering combined with the bulk mobility. The Lombardi model parameters are accessible in the parameter set EnormalDependence. So Lombardi model is taken as an appropriate model (SDevice 2008-09). This model has been used in the literature to calibrate the device simulator (Shrivastava et al. 2008).

Doping dependent mobility degradation is given in by

\[
\frac{1}{\mu} = \frac{1}{\mu_b} + \frac{D}{\mu_{ac}} + \frac{D}{\mu_{sr}}
\]  

(3.1)

where \( \mu \) is the total mobility, \( \mu_b \) is the bulk mobility, \( \mu_{ac} \) is the mobility due to acoustic phonon scattering and \( \mu_{sr} \) is the mobility due to surface roughness scattering. \( D = \exp(-x/l_{\text{crit}}) \) (where \( x \) is the distance from the interface and \( l_{\text{crit}} \) is a fitting parameter) is a damping that switches off the inversion layer terms far away from the interface.
The contribution due to surface roughness scattering is given by

\[
\mu_{sr} = \left( \frac{(F_\perp/F_{ref})^{A^*}}{\delta} + \frac{F_\perp^3}{\eta} \right)^{-1}
\]  

(3.2)

where \( F_{ref} \) is the reference field whose value equals to 1V/cm, \( F_\perp \) is the transverse electric field normal to the semiconductor-insulator surface. The exponent \( A^* \) is given by

\[
A^* = A + \frac{\alpha_\perp (n + p) N_{ref}^{\nu}}{(N_{A,0} + N_{D,0} + N_1)^{\nu}}
\]  

(3.3)

where \( n \) and \( p \) denote the electron and hole concentrations respectively. The reference doping concentration \( N_{ref} = 1 \text{cm}^{-3} \) cancels the unit of the term raised to the power \( \nu \) in the denominator. The parameter \( \alpha \) is sensitive to \( I_{ON} \) and \( \delta \) is sensitive to \( I_{OFF} \) in the parameter set.

Figure 3.5 shows the simulated \( I_D-V_G \) characteristics of FinFETs with \( I_{OFF} = 8.59 \text{ nA}/\mu\text{m} \) in log scale and \( I_{ON} = 2.83 \text{ mA}/\mu\text{m} \) in linear scale. Figure 3.6 shows the simulated \( I_G-V_G \) characteristics of FinFETs. It can be seen that the gate current initially decreases and then increases because of gate induced drain leakage (GIDL). The structural and doping parameters are taken from the nominal device as given in Table 3.1. Figure 3.7 shows the simulated \( I_D-V_G \) characteristics of FinFETs for various hard mask heights. The effect of the parasitic top gate can be seen from Fig. 3.7. It can be observed that the current decreases as the hard mask height is increased from 50 nm to 100 nm.
Figure 3.5: $I_D$-$V_G$ characteristics of FinFETs of gate length 30 nm with $I_{OFF} = 8.59 \text{ nA/µm}$ (log scale) and $I_{ON} = 2.83 \text{ mA/µm}$ (linear scale)
3.3 PARAMETER SPACE

The process parameters considered here are $L_g$, $L_{un}$, $T_{ox}$, $W$, $H$, source/drain cross-sectional area, fin taper angle, corner radius, HM, $N_{ch}$ and $N_{SD}$. These eleven parameters are varied over a range of values to capture their effect on $f_t$, NQS delay, intrinsic gain and NF. Table 3.1 gives the dimensions of the nominal device and the range for the various parameters studied.
Table 3.1: Dimensions of the nominal device and their range of values in FinFETs

<table>
<thead>
<tr>
<th>Process parameters</th>
<th>Nominal value</th>
<th>Range of values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate length (L&lt;sub&gt;g&lt;/sub&gt;)</td>
<td>30 nm</td>
<td>20 nm - 40 nm</td>
</tr>
<tr>
<td>Fin width (W)</td>
<td>4 nm</td>
<td>3 nm - 10 nm</td>
</tr>
<tr>
<td>Fin height (H)</td>
<td>4 nm</td>
<td>2 nm - 7 nm</td>
</tr>
<tr>
<td>Underlap (L&lt;sub&gt;un&lt;/sub&gt;)</td>
<td>3 nm</td>
<td>1 nm - 8 nm</td>
</tr>
<tr>
<td>Source/Drain cross sectional area</td>
<td>22.5 nm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>16 nm&lt;sup&gt;2&lt;/sup&gt; - 48 nm&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>Oxide thickness (T&lt;sub&gt;ox&lt;/sub&gt;)</td>
<td>1 nm</td>
<td>0.5 nm - 3 nm</td>
</tr>
<tr>
<td>Fin-taper angle</td>
<td>2°</td>
<td>0° - 5°</td>
</tr>
<tr>
<td>Corner radius</td>
<td>1 nm</td>
<td>0 nm - 2 nm</td>
</tr>
<tr>
<td>Hard mask height (HM)</td>
<td>10 nm</td>
<td>0 nm - 100 nm</td>
</tr>
<tr>
<td>Channel doping (N&lt;sub&gt;ch&lt;/sub&gt;)</td>
<td>1X10&lt;sup&gt;16&lt;/sup&gt;/cm&lt;sup&gt;3&lt;/sup&gt;</td>
<td>1X10&lt;sup&gt;15&lt;/sup&gt;/cm&lt;sup&gt;3&lt;/sup&gt;-1X10&lt;sup&gt;19&lt;/sup&gt;/cm&lt;sup&gt;3&lt;/sup&gt;</td>
</tr>
<tr>
<td>Source/drain doping (N&lt;sub&gt;SD&lt;/sub&gt;)</td>
<td>1X10&lt;sup&gt;20&lt;/sup&gt;/cm&lt;sup&gt;3&lt;/sup&gt;</td>
<td>1X10&lt;sup&gt;18&lt;/sup&gt;/cm&lt;sup&gt;3&lt;/sup&gt;-2X10&lt;sup&gt;20&lt;/sup&gt;/cm&lt;sup&gt;3&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

3.4 RESULTS AND DISCUSSION

The various parameters mentioned previously are varied to study their impact on f<sub>t</sub>, NQS delay, intrinsic gain and noise figure. There are two sub-sections (i) Wide range variation of various parameters to understand the general behavior of f<sub>t</sub>, NQS delay, intrinsic gain and noise figure and (ii) Ranking of the parameters where the parameter variations are ± 10%. While the parameters are varied over a wide range source cross sectional area should not become smaller than the fin cross sectional area and this was taken care by coupling these parameters while structure generation. This constraint is removed when the variations are small i.e. ± 10%.
3.4.1 Wide range variations

The parameters to be varied and their range are listed down in the Table 3.1.

3.4.1.1 Impact on $f_t$

Figure 3.8 (a) and (b) shows the 3D structure of FinFET for smaller and larger gate lengths respectively.

![Figure 3.8: FinFET for (a) smaller gate length (b) larger gate length](image)

Figure 3.9 shows the variation of $f_t$ against gate length ($L_g$). It can be observed from Figure 3.9 that $f_t$ decreases monotonically. The well-known $g_m$ degradation for higher gate lengths leads to this behavior.
Figure 3.9: Variation of $f_t$ with respect to gate length in FinFETs

Figure 3.10 (a) and (b) shows the 3D structure of FinFET for smaller and larger underlaps respectively. The hard mask is removed for clarity.

Figure 3.10  FinFET for (a) smaller underlap (b) larger underlap
Figure 3.11 depicts the plot between $f_t$ and underlap ($L_{un}$). It can be seen from Figure 3.11 that $f_t$ initially increases and then decreases with respect to $L_{un}$. Increasing $L_{un}$ reduces the fringing capacitance and thereby $C_{gg}$ (Fatemeh et al 2010). $C_{gg}$ can be expressed as

$$C_{gg} = \frac{C_{ox}C_{si}}{C_{ox} + C_{si}} + C_{ov} + C_{fringing}$$  \hspace{1cm} (3.4)$$

where $C_{gg}$ is the gate capacitance, $C_{ox}$ is the oxide capacitance, $C_{si}$ is the silicon body capacitance, $C_{ov}$ is the gate to source/drain overlap capacitance and $C_{fringing}$ is the fringing capacitance and is given by (Shrivastava and Fitzpartrick 1982)

$$C_{fringing} = \frac{WK\varepsilon_d\ln\frac{\pi W}{\sqrt{L_{un}^2 + T_{ox}^2}}}{\pi} e^{\frac{|L_{un} - T_{ox}|}{|L_{un} + T_{ox}|}}$$  \hspace{1cm} (3.5)$$

where $K$ is the relative dielectric constant, $\varepsilon_d$ is dielectric permittivity. When $L_{un}$ increases current degrades and thereby $g_m$ monotonically decreases. The combined behavior of $g_m$ and $C_{gg}$ is responsible for the $f_t$ trend seen in Figure 3.9.

Figure 3.11: $f_t$ versus underlap in FinFETs
Figure 3.12 (a) and (b) shows the 3D structure of FinFET for smaller and larger fin widths respectively.

When fin width (W) is varied we may either face volume inversion or may not which depends upon the channel doping level (Lin et al 2003). Volume inversion is a phenomenon that appears in very thin or narrow film multi-gate MOSFETs due to the fact that the inversion carriers are not confined near the Si/SiO₂ interface, as predicted by classical device physics, but rather at the center of the film. It can be observed both in double gate and triple gate SOI MOSFETs (Ouisse 1994; Baie et al 1995).

When the channel doping is $1\times10^{16}$/cm³ volume inversion is not seen. This behavior is seen in Figure 3.13. Therefore, the increase in W increases current and thereby $g_m$ and $f_t$. For the channel doping around $1.5\times10^{18}$/cm³, volume inversion effect is seen which causes $f_t$ to increase initially and then to decrease with respect to W. Figure 3.14 shows this kind of behavior between $f_t$ and W. Figure 3.15 shows the electron density profile taken along the fin width.
Figure 3.13: Variation of $f_t$ with respect to $W$ without volume inversion in FinFETs

Figure 3.14: Variation of $f_t$ with respect to $W$ with volume inversion in FinFETs
Figure 3.15: Electron Density versus distance along the width

Figure 3.16 (a) and (b) shows the 3D structure of FinFET for thinner and thicker gate oxide thicknesses respectively.

Figure 3.16: FinFET for (a) thinner gate oxide (b) thicker gate oxide

Figure 3.17 shows the variation of $f_t$ with gate oxide thickness ($T_{ox}$). It can be observed from Figure 3.17, that for oxide thicknesses below 2 nm, when we move from thicker to thinner gate oxide thickness, $f_t$ decreases. The mobility degradation due to vertical gate electrical field comes into picture which can be seen in Figure 3.18. Also the increase in $C_{gg}$ is more
compared to that of $g_m$ (Suryagandh et al 2004). Thus $f_t$ decreases with gate oxide scaling. For very thick oxides, $f_t$ once again decreases as usual.

Figure 3.17: Variation of $f_t$ against gate oxide thickness in FinFETs

Figure 3.18: Variation of mobility along the channel in FinFETs
Figure 3.19 (a) and (b) shows the 3D structure of FinFET for smaller and larger source/drain (S/D) cross-sectional areas respectively. Cross sectional areas of source and drain regions are increased through selective epitaxial technique. The resulting structure is commonly referred as Raised Source and Drain (RSD) (Colinge 2008).

![Figure 3.19: FinFET for (a) smaller S/D cross-sectional area (b) larger S/D cross-sectional area](image)

The cross-sectional area reduces the parasitic resistance. Figure 3.20 shows $f_t$ as a function of source/drain cross-sectional area. It can be noticed from Figure 3.20 that $f_t$ decreases with respect to source/drain cross-sectional area. Even though the cross-sectional area reduces the resistance it increases the parasitic capacitance. This results in reduced $f_t$. 
Figure 3.20: Variation of $f_t$ with respect to source/drain cross sectional area in FinFETs

Figure 3.21 (a) and (b) shows the 3D structure of FinFET for smaller and larger fin heights respectively.

Figure 3.21: FinFET for (a) smaller fin height (b) larger fin height
Figure 3.22 depicts the variation of $f_t$ with respect to fin height (H). It can be observed that $f_t$ is affected by fin height variation when it is smaller than the fin width whereas $f_t$ is not affected by the fin height variation when it is larger than the fin width. When the fin height is greater than the fin width, the increase in fin height increases both $g_m$ and $C_{gg}$ equally. So $f_t$ is expected to be independent of $H$ in this regime.

![Figure 3.22: Variation of $f_t$ with respect to fin height in FinFETs](image)

Figure 3.23(a) and (b) shows the 3D structure of FinFET for smaller and larger fin tapers respectively. Drain, gate oxide and hard mask are removed for clarity. The fin taper changes the available channel width, and $g_m$ and $C_{gg}$ are expected to get affected equally. But, the mobility may change due to fin taper. The simulation results show that $f_t$ is almost independent of fin taper angle. This is reflected in Figure 3.24.
Figure 3.23: FinFET for (a) smaller fin taper (b) larger fin taper

Figure 3.24: Variation of $f_t$ with respect to fin taper angle in FinFETs

Figure 3.25 (a) and (b) shows the 3D structure of FinFET for smaller and bigger corner radiiuses respectively.
Figure 3.25: FinFET for (a) smaller corner radius (b) bigger corner radius

Figure 3.26 shows variation of $f_t$ with respect to corner radius. When the corner is rounded with bigger radius, the fin has larger amount of gate oxide in those regions. Therefore the $g_m$ and $C_{gg}$ are expected to go down and thus $f_t$ is less significant to corner radius which can be observed in Figure 3.26.

Figure: 3.26 $f_t$ versus corner radius in FinFETs
Figure 3.27 (a) and (b) shows the 3D structure of FinFET for smaller and larger hard mask heights respectively.

Figure 3.27: FinFET for (a) smaller hard mask height (b) larger hard mask height

Figure 3.28 depicts variation of $f_t$ with respect to hard mask height. The variation of hard mask height depends on the variation of channel width which is least significant to $f_t$. From Figure 3.28, it can be noted that $f_t$ is not significant to variation in hard mask height except for some initial values.

Figure 3.28: Variation of $f_t$ with respect to hard mask height in FinFETs
Figure 3.29 show the variation of $f_t$ against $N_{ch}$. Threshold voltage of DGFET/FinFET is least significant up to $1 \times 10^{17}/\text{cm}^3$ (Xiong and Boker 2003), from which it can be reasoned out that $f_t$ is also least significant at lower channel doping levels. The same behavior is seen in Figure 3.29. At higher doping levels, $f_t$ decreases due to mobility degradation thereby resulting in $g_m$ degradation.

![Figure 3.29 $f_t$ versus channel doping in FinFETs](image)

Figure 3.29 $f_t$ versus channel doping in FinFETs

When source/drain doping ($N_{SD}$) increases, $I_{ON}$ and $g_m$ increase due to the lowered parasitic series resistance and thereby $f_t$ is expected to increase. Figure 3.30 which shows the variation of $f_t$ with $N_{SD}$ reflects the same.

![Figure 3.30: $f_t$ versus source/drain doping in FinFETs](image)

Figure 3.30: $f_t$ versus source/drain doping in FinFETs
3.4.1.2 Impact on NQS delay

The eleven different process parameters are varied one at a time, according to the range given in Table 3.1 and their impact on NQS delay is studied in this section. NQS delay is extracted as discussed in Section 2.3.3 at a frequency of 200 GHz. To reason out the simulation result, the expression given by Allen et al (2002) is used. For a particular NQS delay, the NQS frequency \( f_{NQS} \) is given by

\[
 f_{NQS} = \frac{\alpha \mu_{eff} (V_{GS} - V_T)}{2\pi L_g^2}
\]

(3.6)

where \( \alpha \) is the fitting parameter depending on the accuracy required for the simulation to an NQS event, \( \mu_{eff} \) the mobility, \( V_{GS} \) the gate bias and \( V_T \) the threshold voltage of the transistor.

Figures 3.31 show the variation of NQS delay (extracted at 200 GHz) with respect to various parameters. Intuitively, NQS delay should show a reverse trend to the variation of parameters compared to \( f_t \) and this can be observed in Fig. 3.31. For example, Figure 3.31 (a) shows the variation of NQS delay with respect to \( L_g \). It can be seen that the delay increases with respect to \( L_g \). This can be compared with Fig. 3.9. Equation 3.6 predicts that as \( L_g \) increases \( f_{NQS} \) decreases i.e. for the given frequency NQS delay increases. Figure 3.31(b) shows the variation of NQS delay with respect to \( L_{un} \). It can be observed that the delay increases as we move from nominal \( L_{un} \). Once again, the reverse trend was observed in \( f_t \) versus \( L_{un} \) plot Fig. 3.11
Figure 3.31 (Continued)
3.4.1.3 Impact on intrinsic gain

As discussed in 2.3.1, the different structural and doping related parameters are varied one at a time, according to the range given in Table 3.1 and their impact on intrinsic gain is studied in this section. Since intrinsic gain depends on both $g_m$ and $R_o$, their combined behavior brings the increasing or decreasing tendency with respect to the parameter variation. In the studied region, $R_o$ dominates and decides the trends seen in the Fig. 3.32. It can be observed from Fig. 3.32 and the plots of Section 3.4.1.1 that $f_i$ and intrinsic gain trade off with each other in general.
Figure 3.32 (Continued)
Figure 3.32: (a)-(k) Intrinsic gain versus structural and doping parameters in FinFETs

3.4.1.4. Impact on noise figure

In this section the parameters are varied one at a time, according to the range given in Table 3.1 and their impact on noise figure is analyzed. NF is extracted using the Equation 2.8 as discussed in Section 2.3.5, at a frequency of 10 GHz. The results can be reasoned out using the following expression which relates the noise figure and $f_t$.

$$NF = 1 + \left(\frac{f_0}{f_t}\right)K$$

(3.7)

where $f_o$ is the resonant frequency, $f_t$ is the unity gain frequency and $K$ is the noise factor scaling coefficient. It can be observed from Equation 3.7 that NF is inversely proportional to $f_t$, and so the trends of various parameters with respect to noise figure. This can be evidently seen from Fig. 3.33.
Figure 3.33 (Continued)
Figure 3.33: (a)-(k) Noise figure versus structural and doping parameters in FinFETs

3.4.2 Ranking of the parameters

The ranking of the parameters is done by simple sensitivity analysis as well as using screening experiment method. In the former case, ranking is obtained using the sensitivity coefficients. In the latter case, the ranking is obtained from screening experiment where Plackett-Burman DOE is formed as discussed in Section 2.5. Sensitivity analysis is done by varying one parameter at a time (discussed in Section 2.4). The independent vector is given by

\[ X = [L_g, L_{un}, W, T_{ox}, \text{RSD}, H, \text{Taper}, \text{corner radius}, \text{HM}, N_{ch}, N_{SD}] \]
The response vector is given by \( Y = [f_t, \text{NQS delay}, \text{intrinsic gain and NF}] \).
The sensitivity coefficients for various parameters are calculated as discussed in Section 2.4 and their ranking is given in Table 3.2.

The ranking of the parameters are given in Table 3.2. It could be observed that the ranking of various responses vary from each other. These ranking orders can be reasoned as in Section 3.4.1. There are few differences compared to wide range variations discussed in Section 3.4.1. In this section the source-drain cross sectional area and fin cross sectional (fin width and fin height) area are independent where as it is coupled in Section 3.4.1 to avoid the fin cross section becoming larger than the source-drain cross section. So the results of 3.4.1 and 3.4.2 show some differences.

Table 3.2: Ranking for the structural and doping parameters for FinFETs based on the sensitivity study

<table>
<thead>
<tr>
<th>Factors</th>
<th>Rank</th>
<th>( f_t )</th>
<th>NQS delay</th>
<th>Intrinsic gain</th>
<th>NF</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_g )</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>( L_{un} )</td>
<td>3</td>
<td>4</td>
<td>6</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>( W )</td>
<td>7</td>
<td>2</td>
<td>1</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>( T_{ox} )</td>
<td>5</td>
<td>6</td>
<td>4</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>RSD</td>
<td>11</td>
<td>9</td>
<td>10</td>
<td>9</td>
<td></td>
</tr>
<tr>
<td>( H )</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Fin Taper</td>
<td>8</td>
<td>11</td>
<td>9</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Corner Radius</td>
<td>10</td>
<td>7</td>
<td>7</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>( HM )</td>
<td>6</td>
<td>5</td>
<td>8</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>( N_{ch} )</td>
<td>9</td>
<td>8</td>
<td>11</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>( N_{SD} )</td>
<td>4</td>
<td>10</td>
<td>5</td>
<td>8</td>
<td></td>
</tr>
</tbody>
</table>
To rank the parameters using screening experiments the procedure described in the Section 2.5 is followed. Unlike sensitivity study here more than one parameter can change at a time. The response is written as a function of input variables as a first order polynomial expression and the ranking is performed by the values of the coefficients (already discussed in detail in Section 2.5). The equation for the output parameter \( f_t \) is given as

\[
f_t(L_g, L_{un}, W, T_{ox}, \text{RSD}, H, \text{Taper}, \text{Radius}, \text{HM}, N_{ch}, N_{SD}) = \beta_{L_g} L_g + \\
\beta_{L_{un}} L_{un} + \beta_W W + \beta_{T_{ox}} T_{ox} + \beta_{\text{RSD}} \text{RSD} + \beta_H H + \beta_{\text{Taper}} \text{Taper} + \beta_{\text{Radius}} \text{Radius} + \\
\beta_{\text{HM}} \text{HM} + \beta_{N_{ch}} N_{ch} + \beta_{N_{SD}} N_{SD}
\]

(3.8)

In a similar manner, the equation for the other output parameters, NQS delay, intrinsic gain and NF can be written. The individual ranks computed after regression modeling using their coefficient values, for the responses under consideration, are tabulated in Table 3.3. The overall ranking for the parameters is evaluated by adding all the output coefficient values and arranging in the decreasing order which is given in Table 3.4.

Table 3.3: Individual ranking for the structural and doping parameters for FinFETs based on PB screening experiments

<table>
<thead>
<tr>
<th>Rank</th>
<th>Factors</th>
<th>( f_t )</th>
<th>NQS delay</th>
<th>Intrinsic gain</th>
<th>NF</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( L_g )</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>( L_{un} )</td>
<td>3</td>
<td>8</td>
<td>9</td>
<td>6</td>
</tr>
<tr>
<td>6</td>
<td>( W )</td>
<td>6</td>
<td>2</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>( T_{ox} )</td>
<td>5</td>
<td>6</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>8</td>
<td>( \text{RSD} )</td>
<td>8</td>
<td>7</td>
<td>11</td>
<td>8</td>
</tr>
<tr>
<td>2</td>
<td>( H )</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>11</td>
<td>( \text{Fin Taper} )</td>
<td>11</td>
<td>9</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>7</td>
<td>( \text{Corner Radius} )</td>
<td>7</td>
<td>11</td>
<td>6</td>
<td>7</td>
</tr>
<tr>
<td>10</td>
<td>( \text{HM} )</td>
<td>10</td>
<td>10</td>
<td>7</td>
<td>11</td>
</tr>
<tr>
<td>9</td>
<td>( N_{ch} )</td>
<td>9</td>
<td>4</td>
<td>8</td>
<td>9</td>
</tr>
<tr>
<td>4</td>
<td>( N_{SD} )</td>
<td>4</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>
Table 3.4: Overall ranking for the structural and doping parameters for FinFETs based on PB screening experiments

<table>
<thead>
<tr>
<th>Overall Rank</th>
<th>Factors</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$L_g$</td>
</tr>
<tr>
<td>2</td>
<td>$H$</td>
</tr>
<tr>
<td>3</td>
<td>$L_{un}$</td>
</tr>
<tr>
<td>4</td>
<td>$W$</td>
</tr>
<tr>
<td>5</td>
<td>$N_{SD}$</td>
</tr>
<tr>
<td>6</td>
<td>$T_{ox}$</td>
</tr>
<tr>
<td>7</td>
<td>Corner Radius</td>
</tr>
<tr>
<td>8</td>
<td>$N_{ch}$</td>
</tr>
<tr>
<td>9</td>
<td>RSD</td>
</tr>
<tr>
<td>10</td>
<td>HM</td>
</tr>
<tr>
<td>11</td>
<td>Fin Taper</td>
</tr>
</tbody>
</table>

To evaluate the efficiency of the screening experiments, random numbers are generated using Pseudo-Random Number (PRN) generator with the $\mu$ value given in Table 3.5 for all the parameters with their $3\sigma$ equal to 10% of their mean or nominal values. All the parameters are assumed to have Gaussian distribution and are assumed to be statistically independent of each other. In one set of simulations all the 11 parameters are varied randomly for the device. In the second set only the top 5 parameters were varied, ignoring the contribution from rest of the 6 parameters by keeping them at their nominal value. All the statistics pertaining to device parameters along with their distributions were extracted. The statistics that are computed in both the cases are summarized in Table 3.5.
Table 3.5: Statistics for top 5 significant parameters and all 11 parameters

<table>
<thead>
<tr>
<th>Output Parameter</th>
<th>5 Parameters</th>
<th>11 Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Mean (µ)</td>
<td>Standard Deviation(σ)</td>
</tr>
<tr>
<td>f_t (GHz)</td>
<td>708</td>
<td>117.78</td>
</tr>
<tr>
<td>NQS delay (degrees)</td>
<td>5.12</td>
<td>1.05</td>
</tr>
</tbody>
</table>

From the Table 3.5, it may be observed that, the mean and standard deviation by considering for the top 5 parameters and by considering all the parameters match closely.

3.5 CONCLUSION

In this chapter, the conventional FinFET device is studied for structural and doping parameter variation. Nine structural and two doping parameters are taken as input and their effect on $f_t$, NQS delay, intrinsic gain and noise figure have been studied. The inputs are varied over a wide range to understand the general behavior. Then the parameters are ranked quantitatively through the systematic studies i.e. using sensitivity analysis and Plackett-Burman DOE screening method. The individual as well as an overall ranking have been provided for the input parameters. $L_g$ and H occupy the top most rank whereas fin taper and HM occupy the last two ranks.