CHAPTER 1

INTRODUCTION

1.1 RF SILICON TECHNOLOGY

The everlasting speed in the wireless communication requires increased amount of computation with limited power. The future of mobile wireless communication networks will include Multiple Input Multiple Output (MIMO), fourth generation/fifth generation (4G/5G), etc. With this continued innovation in the wireless technology, it becomes mandatory to follow the Moore’s law and to provide electronics with all the time increasing performance with reduced price (Ermolov 2007). So the success behind the wireless communication would be given to the CMOS technology. The steady downscaling of transistor dimensions over the past two decades has been the main stimulus to the growth of silicon integrated circuits (ICs) and the information industry. The more an IC is scaled, the higher will be its packing density, the higher its circuit speed, and the lower its packing dissipation. These have been key in the evolutionary progress leading to today’s computers and communication systems, that offer superior performance, dramatically reduced cost per function, and much-reduced physical size compared to their predecessors (Taur 2002).

With operating frequencies in commercial wireless products reaching up to 2.4 GHz, and much higher frequencies under consideration for the future, Radio Frequency (RF) technology presents a challenge to active
device design and integration (Chen et al 2001). A 2.1 GHz merged CMOS low noise amplifier (LNA) and mixer is first fabricated in 0.35µm technology (Sanjanni et al 2001). For the frequencies 5.8 GHz and 10 GHz, LNAs are fabricated using 130 nm CMOS technology (Song et al 2008; Battista et al 2008). Many high frequency RF transceivers are explored in CMOS technology (Issakov et al 2009; Huang and Wentzioff 2011; Zhang et al 2011).

Figure 1.1 is the chart showing the operating frequency range used in CMOS technology.

![Figure 1.1: Chart showing the operating frequency range used in CMOS technology](image)

It should also be pointed out that the non-silicon-based RF circuits like LNA, oscillator, mixer, etc. explored in the literature use frequencies above 210 GHz. To name a few, a 35 GHz GaAs FET oscillator is first studied in the literature (Dow et al 1986). Two years later, 94 GHz low noise
GaAs FET oscillator is investigated by Bermudez et al (1988). A HEMT-based G-band mixer operating in the frequency range around 210 GHz has been discussed (Kallfass et al 2008).

Functional level integration or system on chip (SOC) solution i.e. the integration of memory, digital block, analog block and RF block, is another aspect because of which the CMOS gains the economic success. For example, the applications such as wireless LAN and Bluetooth, and GSM cellular transceivers and GPS receivers use RF Integrated circuits. The applications of SOCs are explored in the literature (Lahiri and Raghunathan 2004; Zhao et al 2008). The progress in CMOS technology has made it well suited for RF and microwave operations at high level of integration, and the continuous improvement of the device performance has made it a contender for low-power and eventually low-cost radio front end (Larson 2003).

As the RF market emerges, novel process steps, materials, and device structures are likely to be introduced to silicon in order to improve the quality of the RF components and so the performance of the integrated RF system. In light of the new ways of utilizing the established silicon processes and the potential innovations, “silicon RF technology” qualifies as a new paradigm. Many literatures are available stating the advantages in silicon RF technology (Long and Copeland 1997; Long 2000; Szmyd 2001; Yoon et al 2002). Figure 1.2 shows the evolution of RF silicon technology with the novel devices classified as quasi-planar FinFET (Tang et al 2001) and planar, self-aligned double gate MOSFETs called Pagoda and Super Self-aligned Double Gate (SSDG) respectively (Guarini et al 2001; Lee et al 1999).
MULTI-GATE FET TECHNOLOGY

As the CMOS device dimensions were shrinking for the past two to three decades it faced many problems. As the dimensions of transistors are shrunk, the close proximity between the source and the drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region, and undesirable effects, called the short-channel effects start plaguing MOSFETs. The solutions to these problems can be classified as channel engineering and source-drain engineering. Even besides the proposed solutions, the relentless march past of 'the application of Moore’s law and scaling' has slowed down as the dimensions gone below 100 nm. Even though the CMOS technology encounters many problems at lower dimensions, the main problem is the short-channel effect due to which the sub-threshold performance of the CMOS device degrades.

As the CMOS dimension, in particular the channel length, is scaled to the nanometer regime (<100 nm), the electrical barriers in the device begin to lose their insulating properties because of thermal injection and quantum mechanical tunneling (Taur et al 1997). This results in a rapid rise of the
standby power of the chip, placing a limit on the integration level as well as on the switching speed. Next problem is related to the process variation. As the dimensions reduce, new processing steps are needed which increase the sources of variation. The impact of variability increases as we move into lower dimensions which degrade the analog and RF performance significantly (Pelgrom et al 1989). To address the issues faced during scaling, there is a need for innovation in the device engineering and new nano devices based on different principles of physics.

Partially depleted silicon MOSFETs are the successors of earlier SOS (Silicon-On-Sapphire) devices. PDSOI (Partially depleted silicon on insulator) MOSFETs were first used for niche applications such as radiation-hardened or high-temperature electronics. At the turn of the century PDSOI technology became main stream as major semiconductor manufacturers started to use it to fabricate high-performance microprocessors. The low-voltage performance of PDSOI devices can be enhanced by creating a contact between the gate electrode and the floating body of the device. Such a contact improves the sub threshold slope, body factor and current drive, but limits the device operation to sub-1V supply voltages (Colinge 2008).

Fully depleted SOI devices have a better electrostatic coupling between the gate and the channel. This results in a better linearity, sub threshold slope, body coefficient and current drive. FDSOI technology is used in a number of applications ranging from low-voltage, low-power to RF integrated circuits (Colinge 2008). Drain induced barrier lowering (DIBL) and short channel effects pop up because the gate loses the control over the channel. The control can be gained by having more than one gate. Silicon-on-insulator technology allows us to do this with little effort compared to the bulk technology.

In a continuous effort to increase the current drive and better control short-channel effects, silicon-on-insulator MOS transistors have evolved from classical, planar, single-gate devices into three-dimensional
devices, multi-gate structures (double, triple- or quadruple- gate devices). It is worth noting that, in most cases, the term a double gate refers to a single gate electrode that is present on two opposite sides of the device. Similarly, the term triple gate is used for a single gate electrode that is folded over three sides of the transistor. One remarkable exception is the MIGFET (Multiple Independent Gate FET) where two separate gate electrodes can be biased with different potentials. Figure 1.3 is the diagram showing the various classifications of multi-gate devices.

![Figure 1.3: Figure showing the various classifications of multi-gate devices](image)

FinFETs, due to their quasi-planar structure they are compatible with existing CMOS technology. They are considered as the potential alternative to CMOS since they allow controlling SCE without heavily doping the channel that is detrimental to the carrier low-field mobility (Jurczak et al
2009) and reduced sensitivity to random dopant fluctuations (Xiong and Boker 2003). Recently a new device called Junctionless transistors comes into existence. Since they do not have junctions, the process is highly simplified and it reduces the need for ultrafast annealing techniques (Colinge et al 2010).

GAA device is one of the implementation of vertical-channel, double gate SOI MOSFET which is a planar MOSFET with the gate electrode wrapped around the channel region. The original GAA device was a double gate device, even though the gate was wrapped around all sides of the channel region, because the silicon island was much wider than thick (Colinge 2008). Nowadays, most people use the GAA acronym for quadruple-gate or surrounding-gate devices having a width-to-height ratio much closer to unity (Moselund et al 2005; Coulie et al 2006). Figure 1.4 is the chart showing the various classifications of FinFET devices.

![Figure 1.4: Chart showing the various classifications of FinFET devices](image-url)
1.3 SCALING AND RF PERFORMANCE

Analog applications need high output resistance, intrinsic gain, and \( g_{m}/I_D \) ratio whereas RF applications need high unity gain cut-off frequency \( (f_t) \), maximum oscillation frequency \( (f_{\text{max}}) \), noise figure (NF), non-quasi static (NQS) delay and gain-bandwidth (GBW) product. As the transistor size shrinks down to deep sub micrometer, the RF performance of the devices has been improved in terms of speed \( (f_t) \) and noise \( (NF_{\text{min}}: \text{minimum noise figure}) \) according to the ITRS (2006). Apart from these, non-linearity is also an important RF parameter. Inevitable external parasitic elements, including \( C_{gb} \) (gate–bulk capacitance), however, become more detrimental to RF performance with scaling down of the transistors (Morifuji et al 1999). In this work, the RF metrics, \( f_t \), NQS delay, intrinsic gain and noise-figure, are taken into consideration and these four parameters are discussed below in brief.

1.3.1 Unity Gain Cut-off Frequency \( (f_t) \)

\( f_t \) is one of the important metric in RF applications. RF performances including \( f_t \) in MOSFETs have been improved with scaling down technology (Dambrine et al 2003; Suk et al 2009). Considering a classical small-signal equivalent circuit for MOSFET, \( f_t \) in MOSFETS is given by Dambrine et al (2003)

\[
f_t \approx \frac{g_m}{2\pi C_{\text{gin}} \left[ 1 + 2 \frac{C_{\text{Miller}}}{C_{\text{gin}}} \right]^{1/2}}
\]

\[
f_t = \frac{f_c}{\sqrt{1 + 2 \frac{C_{\text{Miller}}}{C_{\text{gin}}}}} \tag{1.2}
\]
With \( C_{\text{gin}} = C_{\text{gsi}} + C_{\text{overlap}} + C_{\text{fringing}} \) and \( C_{\text{Miller}} = C_{\text{gdi}} + C_{\text{overlap}} + C_{\text{fringing}} \) with \( g_m \), the trans-conductance, \( C_{\text{gin}} \), the total gate-to-source input capacitance and \( C_{\text{Miller}} \), the total gate-to-drain capacitance. It should be added that physics-based simulations show that \( C_{\text{gdi}} \) is very low and \( C_{\text{Miller}} \) is strongly conditioned by the value of \( C_{\text{overlap}} \) (in a regime of channel saturation) which depends on the source/drain extension (SDE) process. \( f_c \) is the intrinsic cut-off frequency determined by the ratio of \( g_m / 2\pi C_{\text{gin}} \). It measures the intrinsic ability of field effect transistor (FET) to amplify high frequency signals.

For a complete device, including extrinsic elements, we can define \( f_t \) as the frequency at which the short circuit small signal current gain of the device drops to unity, indicative of the speed of the intrinsic device. \( f_t \) is calculated by

\[
f_t = \frac{g_m}{2\pi C_{\text{gg}}}
\]

where \( C_{\text{gg}} \) is the combination of \( C_{\text{gs}}, C_{\text{gd}}, \) overlap capacitance and any other fringing capacitance. FinFET based RF applications are abundantly available in the literature (Kranti and Armstrong 2007; Wambacq et al 2007; Scholten et al 2010).

1.3.2 Non-Quasi Static (NQS) Effects

With the continuous improvement in the performance of MOS transistors resulting from technology scaling, the number of RF circuits implemented by CMOS technology has significantly increased (Harada et al 2000; Shenai et al 2000). An accurate compact high-frequency MOSFET model becomes essential. One major concern with the accuracy in using these models is the NQS effects. This is because most simulations of integrated CMOS circuits are performed under the quasi-static (QS) approximation.
which ignores the carrier-transit delay in the channel. For RF applications, it is necessary to use NQS models at and near cut-off frequencies, while most digital applications can be still dealt with QS approximation (Nakayama et al 2004). Many reports have already illustrated the problem of ignoring the NQS effect in high-frequency simulation (Paulous and Antoniads 1983; Tsividis and Masetti 1984; Tsividis and Suyama 1994; Vandarnme and Badenes 2000).

Low frequency models are usually derived from DC analysis by using the quasi static approach. This quasi static approximation assumes that the charge density at any position in the channel changes instantaneously with the applied voltages (Carlos and Schneider 2007), i.e., it assumes the transit time in the channel to be zero. Since the channel transit time is not zero, analyses based on the quasi-static approximation introduce errors for rapidly changing terminal voltages due to the distributed nature of the device. Models that take into account of the distributed nature of the device are described as NQS models. For modeling NQS behavior, time dependence of semiconductor equations has to be taken into account. The NQS effects impose a frequency limit to the analog circuits. This is not only due to decreasing amplification, but phase shift effects may already become relevant at lower frequencies (Smeds and Klaasen 1995; Tsividis 1999). Besides NQS effects, various parasitic capacitances will come into picture at radio frequencies.

The scaling characteristics of $f_t$ in MOSFETs and FinFETS are studied in the literature (Kao et al 2006; Jagannathan et al 2006; Subramanian et al 2003; Nuttinck et al 2007). The effect of scaling on the NQS behavior of MOSFETs is studied by Srinivasan and Bhat (2003). The scaling characteristics of $f_t$ and $f_{NQS}$ in MOSFETs are studied under different scenarios. For uniform and non-uniform channel doping, $f_t$ and $f_{NQS}$ are
investigated by Srinivasan and Bhat (2005), for with and without supply voltage scaling, $f_t$ and $f_{NOS}$ are studied by Srinivasan and Bhat (2005 a).

1.3.3 Intrinsic gain

From analog perspective, the high intrinsic gain is a strong argument to use multi-gate devices in future technology nodes, as it overcomes one of the most critical scaling issues in planar bulk CMOS. In FinFETs, the high intrinsic gain is due to the very low output conductance (Fulde 2010).

Intrinsic gain in FinFETs has been explored in many papers. For example, the SDE is used to improve the gain of FinFETS (Kranti and Armstrong 2007; Kranti and Armstrong 2007a). The suitability of FinFETs for low power analog circuits having higher intrinsic gain is studied (Fulde et al 2007). In Junctionless FETs, better intrinsic gain is achieved compared to the inversion mode devices (Doria et al 2011).

1.3.4 Noise Figure

RF circuits operating in GHz region demands very low noise figure. The RF noise of the transistors in the first stage is the predominant cause of the LNA noise figure. LNA is a very critical circuit and it must satisfy many requirements, such as low noise figure, high gain, high linearity, good impedance matching and good reverse isolation (Razavi, 1998).

The noise performance of a single and double gated device is compared and a significant improvement in NF is observed in double gated MOSFET (Dollfus et al 2006). The low frequency noise of triple gate FinFETs has been studied (Lukyanchikova et al 2009). Low frequency noise in Junctionless transistors is investigated (Jang et al 2011). The noise
performance of inversion mode and Junctionless devices is studied and compared in (Pushparaj et al 2011).

1.4 MOTIVATION FOR THIS WORK

Multi-gate devices have so far mostly been studied with digital applications in mind, but analog circuits are still unavoidable in several applications, such as audio systems, A/D converters, RF filters. Essentially, the silicon RF technology uses mixed signal processing ICs. SOI-based FinFET structures are seen as a promising alternate for the conventional single gate CMOS devices in the nanometer regime to tackle the short channel effects due to their process compatibility. FinFET carried the idea of MOS devices into nanometer regime. Recently, a new device called Junctionless transistors, are built on the FinFET structure. They do not have junctions and due to its process simplification, they are also a potential alternate for CMOS technology in the nanometer era. Among the surrounding gate devices, GAA devices have gaining importance nowadays. There are many RF parameters to optimize these multi-gate devices and we have taken $f_t$, NQS delay, intrinsic gain and NF which are considered to be the most important RF metrics.

The aim of the thesis is to explore the RF performance metrics, $f_t$, NQS delay, intrinsic gain and NF, in three potential multi-gate devices. The effect of the structural, doping and work function (WF) variations on $f_t$, NQS delay, intrinsic gain and NF in the multi-gate devices like FinFET, Junctionless transistor and GAA device have been investigated. The parameters are ranked by performing a simple sensitivity study and Plackett-Burman design of experiments (DOE). Since the gate electrode work function engineering plays a vital role in the multi-gate devices, a comparative study of the work function variation on AC and DC characteristics of Junctionless transistors is studied in a separate chapter. Also the performance analysis of
the dual metal gate work function in Junctionless devices has been investigated.

1.5 CONTRIBUTION OF THIS THESIS

- Effects of the structural and doping parameters on $f_t$, NQS delay, intrinsic gain and NF have been studied qualitatively in FinFETs.
  
  - Quantitative study is done by performing a simple sensitivity study and Plackett-Burman DOE.

- Effects of the structural and doping parameters on $f_t$, NQS delay, intrinsic gain and NF have been studied qualitatively in Junctionless FETs.
  
  - Quantitative study is done by performing a simple sensitivity study and Plackett-Burman DOE.

- Effect of the gate electrode work function variation in conventional and Junctionless FinFETs.

- Characterization of the dual metal gate electrode work function in Junctionless transistors.
  
  - Suggestion of the permissible work function range.

- Effect of the structural, doping parameters and WF on $f_t$, NQS delay, intrinsic gain and NF have been studied qualitatively in conventional and Junctionless GAA transistors.
  
  - Quantitative study is done by performing a simple sensitivity study and Plackett-Burman DOE.
1.6 ORGANIZATION OF THIS THESIS

In Chapter 2, TCAD simulator and the simulation methodologies used in this thesis have been discussed. In Chapter 3, the effect of the structural and doping parameters on $f_t$, NQS delay, intrinsic gain and NF have been studied qualitatively in FinFETs and ranking of the parameters is done using sensitivity analysis and Plackett-Burman DOE experiment. The effect of the structural and doping parameters on $f_t$, NQS delay, intrinsic gain and NF in Junctionless FETs is investigated in Chapter 4. Chapter 5 and chapter 6 are devoted for gate electrode work function engineering. A comparative study of the work function variation in conventional and Junctionless FETs is considered in chapter 5. The performance analysis of the dual metal gate work function in Junctionless transistor is presented in chapter 6. Finally in Chapter 7, the effect of the structural and doping parameters variation on $f_t$, NQS delay, intrinsic gain and NF in GAA devices is evaluated. Chapter 8 discusses the conclusion and future work to be carried out.