CHAPTER 6

PERFORMANCE ANALYSIS OF JUNCTIONLESS FINFETS WITH DUAL METAL WORK FUNCTION GATE ELECTRODE

In this chapter, dual metal gate (DMG) electrode work function concept is applied in Junctionless transistors. Three different DMG structures along with the single metal gate (SMG) are studied and their performance with respect to the \( I_{ON} \), \( f_t \), \( R_o \), NQS delay, intrinsic gain and NF are compared. Two different gate lengths, 100 nm and 50 nm, and two different gate oxide thicknesses, 1 nm and 3 nm, are explored. Two of the DMG structures, namely DMG-I and II show superior performance compared to SMG devices. A permissible range of work functions which show performance enhancement against SMG device are suggested.

6.1 INTRODUCTION

Conventional MOSFET device is symmetrical in nature. Researchers tried to improve the performance of this device by introducing asymmetry into it. In literature, the asymmetry was first introduced into the MOSFET by means of channel doping profile (Odanaka and Hiroki 1997), also known as asymmetrical halo implanted device. The asymmetry with respect to source/drain doping was also studied by Chen et al (1998) wherein they investigated the effect of having extension doping only on the drain side. This was known as asymmetric lightly doped drain (LDD) device. Another
way to bring the asymmetry into the device is having dual gate materials, known as double/dual metal gate (DMG) device.

DMG engineering technique was first proposed by Long et al (1999) for MOSFET, in which two different materials having different work functions are merged together to form a single gate of a bulk type N-MOSFET. Out of the two portions of the gate, the material closer to the source has higher work function compared to the material closer to the drain which implies that the threshold voltage under source side gate material is higher than that under drain side gate material. As a result, the electric field and electron velocity along the channel suddenly increase near the interface of the two gate materials, resulting in increased gate transport efficiency.

The gate work function engineering allows the DMG devices to have a much lower doping concentration in the channel region as compared to its SMG counterpart to get the same $V_T$ value. The DMG structure can suppress short-channel effects due to the screening effect, which is induced by a step change of the potential along the channel. The novel attributes for DMG devices are the improved carrier transport efficiency and transconductance, reduced channel length modulation and drain conductance, reduction of DIBL and suppression of hot-carrier effect (Long et al 1999; Saxena et al 2002; Chakraborthy et al 2008). DMG applied in bulk CMOS devices have shown higher gain, output resistance, cutoff frequency, etc., in the sub threshold regime (Chakraborthy et al 2008). The novel features of fully depleted (FD) DMG SOI MOSFET are explored theoretically and compared with those of a compatible SOI MOSFET (Chaudhry and Kumar et al 2004).

The idea of dual metal gate work function was carried over to FinFETs by Matsukawa et al (2008) and Mohankumar et al (2010). The structure used in Mohankumar et al work is called as DMG-II. In 2001,
Kedzierski et al. reported the studies on asymmetrical double gate FinFET wherein they have compared its performance against symmetrical double gate device. In this work the structure of DMG is called DMG-III. Apart from DMG-II and DMG-III, there is another structure DMG-I (Vadizadeh and Fathipour 2008). All the three are shown in Figure 1(b), (c) and (d). All the studies quoted above are dealt with the inversion mode devices.

In this chapter, the performance of DMG structures, in double gate Junctionless devices with respect to $I_{\text{OFF}}$, $I_{\text{ON}}$, $f_t$, $R_o$, NQS delay, intrinsic gain an NF are studied. All the three DMG structures are explored in this study, for two different gate length and gate oxide thickness variations. The DMG devices are compared with the single metal gate (SMG) devices. A permissible range of work functions which show performance enhancement against SMG device is suggested. The organization of this chapter is as follows. Section 6.2 discusses about the description of the devices and $I_D$-$V_G$ calibration and Section 6.3 tells about the results and discussions. Finally in Section 6.4 conclusions are given.

6.2 DEVICE DESCRIPTION and CALIBRATION

Four device structures are explored in this study, one traditional structure i.e. single metal (work function) double gate Junctionless device (SMG) and three dual metal gate (dual work functions) devices (DMG-I, DMG-II and DMG-III). Figure 6.1 depicts all the four device structures discussed above where M1 and M2 are used to denote the two different gate metals with WF1 and WF2 as their work functions respectively. All the structures use a doping concentration of $1 \times 10^{19}$/cm$^3$. The gate length ($L_g$), gate oxide thickness ($T_{ox}$), fin width and supply voltage ($V_{DD}$) are 100 nm, 3 nm, 10 nm and 2 V respectively.
Figure 6.1: (a) (b) (c) (d) Cross-sectional view of Junctionless transistors
SMG, DMG-I, DMG-II, and DMG-III respectively
Since the results related to DMG based Junctionless devices are not found in literature, SMG device has been calibrated against the published results by tuning the silicon parameter library file and this parameter file is used in DMG device simulations. As stated above, SMG Junctionless device is calibrated with the published results to match $I_{ON}$ and $I_{OFF}$ (Leung and Chui 2011). The quoted reference uses a gate length of 32 nm and an oxide thickness of 1 nm. From the saturation $I_D$-$V_G$ characteristics, $V_T$, $I_{ON}$ and $I_{OFF}$ are extracted and from $I_D$-$V_D$ characteristics, $R_o$ is extracted at $V_{GS} = \frac{V_{DD}}{2}$. As already stated in 2.3.2, from the standard AC simulations $f_t$ is extracted when $Y_{21}(f) \left| \frac{1}{Y_{11}(f)} \right|$ equals one. NQS delay is extracted at a frequency of 10 GHz, intrinsic gain is extracted at $V_{DD}/2$ and NF is extracted at a frequency of 1 GHz.

6.3 RESULTS AND DISCUSSION

6.3.1 Effect of Dual Metal Gate Work Function on $I_{ON}$, $R_o$, $f_t$, NQS Delay, Intrinsic Gain and NF

Figure 6.2 shows the $I_D$-$V_G$ characteristics of SMG and DMG (I, II, and III). $V_T$ of all the devices are matched to 0.278V through work function adjustment. It can be seen that DMG-I and DMG-II have higher drive currents compared to SMG device whereas DMG-III has slightly lesser drive current. This is in line with the reasoning given by Long et al (1999) i.e. enhancing the electric field, and therefore the electron velocity, near the source, plays a significant role in the overall carrier transport efficiency of the DMG-FET.
Figure 6.2: $I_D-V_G$ characteristics of SMG and DMG-I, II, and III with $V_T$ matched to 0.278V

The electric field distribution along the channel for DMG-I, II, III and SMG are shown in Figure 6.3. The bias points corresponding to Figure 6.3 are $V_{GS}=V_{DS}=2$ V, for all the devices (SMG, DMG-I, DMG-II and DMG-III). It can be seen from Figure 6.3 that SMG and DMG-III show only one peak (in drain) in their electric field distribution along the channel from source to drain whereas DMG-I and II show two peaks (in the channel as well as in the drain). This is responsible for the increased drive currents in DMG-I and II.
Figure 6.3: Electric field distribution along the channel for DMG-I, II, III and SMG

As we increase WF2 the electric field closer to the source region (refer Figure 6.3) decreases. Therefore the velocity of charge carriers at source is lesser for larger values of WF2 resulting in reduced currents. Figure 6.4 depicts the variation of $f_t$ with respect to WF2 for two fixed WF1 i.e. 5.5 eV and 5.4 eV, in DMG-I. When the work function difference, $(WF_1 - WF_2)$, is more positive both WF1 and WF2 have no control on $f_t$. As the work function difference decreases (i.e. WF2 increases for a fixed value of WF1) $f_t$ is affected by both WF1 and WF2. Higher WF1 always yields higher $f_t$ whereas higher WF2 yields lower $f_t$. Figure 6.5 shows the variation of $R_o$ with respect to WF2 for two fixed WF1 (5.4 eV and 5.5 eV) in DMG-I. Figure 6.6 shows the variation of NQS delay with respect to WF2 for two fixed WF1 (5.4 eV and 5.5 eV) in DMG-I. As already discussed, delay should show a
reverse trend of $f_t$ and this is observed from Figure 6.6. Figure 6.7 shows the variation of intrinsic gain with respect to WF2 for two fixed WF1 (5.4 eV and 5.5 eV) in DMG-I. Since the gain depends on the combined behavior of $g_m$ and $R_o$, it is seen that the gain follows the same trend of $R_o$ (refer Figure 6.5). Figure 6.8 shows the variation of NF with respect to WF2 for two fixed WF1 (5.4 eV and 5.5 eV) in DMG-I. It is seen that the NF for the higher WF1 is lower and that of lower WF1 is higher and this may be due to the reverse trend of $f_t$ (refer Figure 6.4).

![Figure 6.4: Variation of $f_t$ with respect to WF2 for DMG-I](image)

DMG-I

Figure 6.4: Variation of $f_t$ with respect to WF2 for DMG-I
Figure 6.5: Variation of $R_o$ with respect to WF2 for DMG-I

Figure 6.6: Variation of NQS delay with respect to WF2 for DMG-I
Figure 6.7: Variation of intrinsic gain with respect to WF2 for DMG-I

Figure 6.8: Variation of NF with respect to WF2 for DMG-I
Figures 6.9 to 6.13 show \( f_t \), \( R_o \), NQS delay and intrinsic gain and NF versus WF2 plots for all the three DMGs. It can be noticed that DMG-I and II show better performance in terms of \( f_t \), \( R_o \), and intrinsic gain compared to DMG-III. But the NF characteristics showed in Figure 6.13 depicts a better performance of DMG-III compared to DMG-I and DMG-II. The work function discontinuities in the gate electrode of DMG-I and DMG-II (Figure 6.1 b and c) increases the \( S_{gg}^1 \) (Figure 6.14) in Equation 2.8 and results in slightly higher NF compared to DMG-III.

Figure 6.9: Comparison of \( f_t \) with respect to WF2 for a fixed WF1=5.5eV for DMG-I, II, III
Figure 6.10: Comparison of $R_0$ with respect to WF2 for a fixed WF1=5.5eV for DMG-I, II, III

Figure 6.11: Comparison of NQS delay with respect to WF2 for a fixed WF1=5.5eV for DMG-I, II, III
Figure 6.12: Comparison of intrinsic gain with respect to WF2 for a fixed WF1=5.5eV for DMG-I, II, III

Figure 6.13: Comparison of NF with respect to WF2 for a fixed WF1=5.5eV for DMG-I, II, III
Figure 6.14: Comparison of $S_{gg}$ with respect to WF2 for a fixed WF1=5.5eV for DMG-I, II, III

6.3.2 Permissible ranges of Work Function

Since, various work function values for M1 and M2 are possible for the given device, a bound for M2 (i.e. WF2) for the given M1 (i.e. WF1) is sought. The work function of M1 (WF1) is varied from 5.1 eV to 5.9 eV in steps of 0.1 eV. Figure 6.15 gives $I_{ON}$ and $I_{OFF}$ variations with respect to WF2 for the given WF1=5.2 eV. The criteria for the bound are $I_{ON}$ and $I_{OFF}$ i.e. the resultant DMG structure should show higher $I_{ON}$ compared to SMG and $I_{OFF}$ should be less than 1 nA/$\mu$m. $I_{ON}$ of SMG device is 1347 $\mu$A/$\mu$m and the constraint can be written as,

$$I_{OFF} \leq 1 \text{nA}/\mu\text{m}$$

$$I_{ON} \geq 1347 \mu\text{A}/\mu\text{m}$$
Figure 6.15: Variation of $I_{\text{ON}}$ and $I_{\text{OFF}}$ with respect to WF2 for a fixed WF1=5.2 eV. The permissible upper and lower bounds of $I_{\text{ON}}$ and $I_{\text{OFF}}$ are shown.

With these constraints, the bounds for WF2 are depicted in Figure 6.15 for the given WF1, for DMG-I. These bound values change when WF1 is varied. Similar bounds can be obtained for DMG-II and DMG-III also. Table 6.1 shows the permissible or bound values of WF2 for DMG-I, II and III, for various WF1. Table 6.1 also depicts the range of $I_{\text{ON}}$, $f_{\text{c}}$, $R_{\text{os}}$, NQS delay, intrinsic gain and NF.
Table 6.1: Permissible upper and lower bounds of WF2 for various WF1 for DMG- I, II and III along with SMG

<table>
<thead>
<tr>
<th>DMG-I</th>
<th>DMG-II</th>
<th>DMG-III</th>
<th>SMG</th>
</tr>
</thead>
<tbody>
<tr>
<td>WF1(eV)</td>
<td>WF2(eV)</td>
<td>WF1(eV)</td>
<td>WF2 (eV)</td>
</tr>
<tr>
<td>5.1</td>
<td>5.4 to 5.5</td>
<td>5.1</td>
<td>5.6 to 5.9</td>
</tr>
<tr>
<td>5.2</td>
<td>5.4 to 5.5</td>
<td>5.2</td>
<td>5.5 to 5.8</td>
</tr>
<tr>
<td>5.3</td>
<td>5.3 to 5.5</td>
<td>5.3</td>
<td>5.2 to 5.7</td>
</tr>
<tr>
<td>5.4</td>
<td>4.5 to 5.4</td>
<td>5.4</td>
<td>4.5 to 5.5</td>
</tr>
<tr>
<td>5.5</td>
<td>4.5 to 5.4</td>
<td>5.5</td>
<td>4.5 to 5.3</td>
</tr>
<tr>
<td>5.6</td>
<td>4.5 to 5.3</td>
<td>5.6</td>
<td>4.5 to 5.1</td>
</tr>
<tr>
<td>5.7</td>
<td>4.5 to 5</td>
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<tr>
<td>5.8</td>
<td>4.5</td>
<td>5.8</td>
<td>-</td>
</tr>
<tr>
<td>5.9</td>
<td>-</td>
<td>5.9</td>
<td>-</td>
</tr>
</tbody>
</table>

$I_{ON} = 1353 \, \mu A/\mu m$ to $1548 \, \mu A/\mu m$
$f_t = 243 \, GHz$ to $286 \, GHz$ and $R_o=41K\Omega$ to $2083K\Omega$
NQS delay= 4 degrees to 34 degrees
Intrinsic gain=123 to 4022
NF=0.3 dB to 0.5 dB

$I_{ON} = 1348 \, \mu A/\mu m$ to $1503 \, \mu A/\mu m$
$f_t=249 \, GHz$ to $284 \, GHz$ and $R_o=41K\Omega$ to $661K\Omega$
NQS delay= 4 degrees to 31 degrees
Intrinsic gain=85 to 940
NF=0.3 dB to 0.4 dB

$I_{ON} = 1348 \, \mu A/\mu m$ to $1451 \, \mu A/\mu m$
$f_t=254 \, GHz$ to $259 \, GHz$ and $R_o=54K\Omega$ to $69K\Omega$
NQS delay= 4 degrees to 30 degrees
Intrinsic gain=77 to 198
NF=0.3 dB to 0.4 dB

$I_{ON}=1347 \, \mu A/\mu m$
$f_t=255 \, GHz$
$R_o=71K\Omega$
NQS delay= 6 degrees
Intrinsic gain=130
NF=0.3 dB
From the table it can also be observed that DMG-I and II provide better performance in terms of $I_{ON}$, $f_t$, $R_o$, and intrinsic gain compared to SMG device. According to the literature, the intrinsic gain and $f_t$ of DMG-II should be high compared to that of SMG (Mohankumar et al 2010). This is evident from the Table 6.1. DMG-III does not show any performance enhancement with respect to SMG device and subsequently DMG-III is ignored. The only advantage of DMG-III is easy fabrication. Figures 6.16 and 6.17 depict the results of Table 6.1 in a different way. It gives the contour plot of the two work functions WF1 and WF2 for the two devices DMG-I and DMG-II. Any combination of work functions within the contour region offers better performance (in terms of $I_{ON}$) compared to SMG device. With respect to $f_t$, NQS delay, intrinsic gain and NF this is not true i.e. when we get a maximum performance with respect to $f_t$ we do not get maximum performance with respect to NQS delay, intrinsic gain and NF. Similar is the case for other parameters too.

Table 6.2 and 6.3 gives the percentage improvement of DMG-I and DMG-II over SMG in terms of $f_t$, NQS delay, intrinsic gain and NF. In a particular row, the bold faced big lettered column show the maximum performance with respect to that row parameter whereas the other columns of that particular row show the percentage improvement in other response parameters. The $f_t$ row in Table 6.2 gives the improvement in $f_t$ for device with maximum $f_t$ from the operating region given by Figure 6.16. The other rows in the Table 6.2 and 6.3 are read in the same way. It can be noticed that there is no improvement with respect to NF i.e. the maximum possible NF performance is as that of SMG device.
Figure 6.16: Contour plot of WF1 and WF2 for DMG-I for $L_g=100$ nm and $T_{ox}=3$ nm

Figure 6.17: Contour plot of WF1 and WF2 for DMG-II for $L_g=100$ nm and $T_{ox}=3$ nm
Table 6.2: Percentage improvement of DMG-I over SMG

<table>
<thead>
<tr>
<th>Maximum Performance</th>
<th>$f_t$</th>
<th>NQS delay</th>
<th>Intrinsic gain</th>
<th>NF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_t$</td>
<td><strong>12.15%</strong></td>
<td>5.26%</td>
<td>27.6%</td>
<td>-0.2%</td>
</tr>
<tr>
<td>NQS delay</td>
<td>10.58%</td>
<td><strong>33.3%</strong></td>
<td>25.6%</td>
<td>-1.1%</td>
</tr>
<tr>
<td>Intrinsic gain</td>
<td>11.15%</td>
<td>13.35%</td>
<td><strong>29.93%</strong></td>
<td>-1.7%</td>
</tr>
<tr>
<td>NF</td>
<td>`9.34%</td>
<td>8.43%</td>
<td>12.57%</td>
<td>No change</td>
</tr>
</tbody>
</table>

Table 6.3: Percentage improvement of DMG-II over SMG

<table>
<thead>
<tr>
<th>Maximum Performance</th>
<th>$f_t$</th>
<th>NQS delay</th>
<th>Intrinsic gain</th>
<th>NF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_t$</td>
<td><strong>11.37%</strong></td>
<td>20%</td>
<td>6.11%</td>
<td>-0.26%</td>
</tr>
<tr>
<td>NQS delay</td>
<td>10.98%</td>
<td><strong>33.3%</strong></td>
<td>6.05%</td>
<td>-1.7%</td>
</tr>
<tr>
<td>Intrinsic gain</td>
<td>11.23%</td>
<td>25.2%</td>
<td><strong>6.23%</strong></td>
<td>-2.4%</td>
</tr>
<tr>
<td>NF</td>
<td>9.21%</td>
<td>7.1%</td>
<td>5.92%</td>
<td>No change</td>
</tr>
</tbody>
</table>

Different values for $L_g$ and $T_{ox}$ change the range of both WF1 and WF2. Table 6.3 shows the WF1 and WF2 bound values for two different $L_g$ and $T_{ox}$, for both DMG-I and II.
Table 6.3: WF1 and WF2 bound values for $L_g = 100$ nm, 50 nm and $T_{ox} = 1$ nm, 3 nm

<table>
<thead>
<tr>
<th>$L_g$ (nm)</th>
<th>$T_{ox}$ (nm)</th>
<th>DMG-I</th>
<th>DMG-II</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>WF1(eV)</td>
<td>WF2(eV)</td>
</tr>
<tr>
<td>100</td>
<td>3</td>
<td>5.1 to 5.8</td>
<td>4.5 to 5.4</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>5.1 to 5.7</td>
<td>4.5 to 5.5</td>
</tr>
<tr>
<td>50</td>
<td>3</td>
<td>5.4 to 5.8</td>
<td>4.5 to 5.3</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>5.1 to 5.7</td>
<td>4.5 to 5.4</td>
</tr>
</tbody>
</table>

Figures 6.18 and 6.19 depict the electric field distribution and electron mobility respectively along the channel for DMG-I and DMG-II at two different work functions (4.5 eV and 5.2 eV), from which we can find the average mobility and average electric field in the channel thereby average velocity can be calculated.

![Electric field distribution along the channel for DMG-I&II at 4.5 eV and 5.2 eV](image-url)
It has been found that the average velocity of DMG-I (velocity=0.2 X10^6 m/s) is higher than that of DMG-II (velocity=0.18 X10^6 m/s), for the lower work function ranges and it is vice versa (the velocity of DMG-I is 0.184X10^6 m/s and that of DMG-II is 0.189 X10^6 m/s) for the higher work functions. This explains the NQS delay behavior because NQS delay basically represents the response time of the carriers.

Figure 6.19: Mobility along the channel for DMG-I&II at 4.5 eV and 5.2 eV
6.4 CONCLUSION

In this chapter, the performance of DMG in double gate Junctionless devices with respect to $I_{OFF}$, $I_{ON}$, $f_t$, $R_n$, NQS delay, intrinsic gain and NF was studied. Three different DMG structures were considered in this work and compared against the SMG structure. Two different gate lengths, 100 nm and 50 nm, and two different gate oxide thicknesses, 1 nm and 3 nm, were explored. Having the drive current as a constraint, the permissible range of work functions which show performance enhancement against SMG device is extracted. The permissible work function value differs with respect to gate length and gate oxide thickness. The overall value of $WF_1$ ranges from 5.4 eV to 5.7 eV and the corresponding range of $WF_2$ is from 4.5 eV to 5.2 eV. Out of the three structures, DMG-III does not show any performance enhancement with respect to SMG device. DMG-I and II show superior performance compared to SMG device except NF. The best NF performance of DMG-I and DMG-II is same as that of SMG device.