CHAPTER 5

EFFECT OF GATE ELECTRODE WORK FUNCTION VARIATION ON DC AND AC PARAMETERS IN CONVENTIONAL AND JUNCTIONLESS FINFETS

In this chapter, the effect of gate electrode work function variation on DC (threshold voltage, drive current, leakage current and output resistance) and AC (unity gain cut-off frequency, non-quasi static delay, input impedance, intrinsic gain and noise figure) characteristics in 30 nm gate length conventional and Junctionless FinFETs has been investigated.

5.1 INTRODUCTION

Polysilicon with dual type doping (N or P) has conventionally been used as highly conductive gate materials for bulk MOSFETs. Metals as an alternate to poly gate have been explored in the literature (King et al 2002). This means that a gate work function should be in such a way that the Fermi energy lies between the conduction band edge and midgap of silicon for NMOS devices, and between midgap and the valence band edge of silicon for pMOS devices. The gate electrode work function plays a vital role in the control of the threshold voltage ($V_T$). According to the ITRS roadmap, the absolute value of threshold voltage will be about 0.2 to 0.3 V for 20-nm, low-power MOSFET devices (Xiong and Bokor 2003). $V_T$ of a long-channel MOSFET is classically defined as,
\[ V_T = \phi_{ms} + 2\phi_f + \frac{Q_D}{C_{OX}} - \frac{Q_{SS}}{C_{OX}} \]  

(5.1)

where \( Q_{SS} \) represents the charges in the gate dielectric, \( C_{OX} \) is the gate oxide capacitance, \( \phi_{ms} \) is the work function difference between the semiconductor and the gate electrode, \( \phi_f \) is the difference between the semiconductor Fermi level \( E_F \) and the intrinsic semiconductor Fermi level \( E_{Fi} \), and \( \phi_f \) is the Fermi potential given by,

\[ \phi_f = \frac{KT}{q} \ln \frac{N_d}{N_i} \]  

(5.2)

In a planar bulk MOSFET, strong inversion occurs when the band bending (surface potential) at the semiconductor surface reaches \( 2\phi_f \) and \( Q_D \) is the depletion charge in the channel. In a fully depleted double-gate MOSFET \( Q_D \) is given by Equation 5.3

\[ Q_D = \frac{q}{2} WN_a \]  

(5.3)

The contribution of the depletion charge \( Q_D \) to the threshold voltage is negligible unless the doping concentration is very high. Since very thin silicon fins are used as channel in FinFETs, heavy doping in the channel is generally avoided to reduce the process variation impact also called random dopant effect (Xiong and Bokor 2003). This forces us to go for metal gates with appropriate work functions in the conventional FinFETs.

The variation in work function with alloy composition has important implications in microelectronics where the desire to precisely control device characteristics without affecting material stability and process
ability. Although the barrier height in metal-semiconductor contacts can be profoundly influenced by oxides, contamination, and surface states, the work function difference between two materials is often used as a first estimate of the electronic barrier height of two joined materials (Sze and Ng 2006). The usual gate materials Aluminum and Copper have work functions 4.26 eV and 4.94 eV respectively whereas Platinum has the highest work function of 5.93 eV. More information about the work function of various elements can be found in (Lide 2008). The literature also reports the dependency of work function on the thickness of the material deposited, in the nanometer regime as shown in Fig. 5.1 (Yan 1992). The range of metal work function considered in this study is from 4.4 eV to 5.9 eV which is in feasible range.

Figure 5.1: Effective work function as a function of film thickness
The threshold voltage of a multiple gate FET (MuGFET) is primarily determined by the effective work function of the gate stack (the work function of the gate electrode and the charges in the gate dielectric or at the interfaces). Figure 5.2 shows the required gate stack work function for various devices (Colinge 2008).

Figure 5.2: Gate work functions for different device types. High Performance (HP) and Low Power (LP) planar bulk MOSFETs need work functions close to the silicon band edges, while HP and LP multi-gate MOSFETs need work function values close to the midgap of the silicon.
Apart from the random dopant effect poly gates also suffer from poly depletion effect which is a serious issue at shorter channel lengths. Work function engineering has been tried out to suppress the parasitic conduction path at the corners (Han et al 2008). Gate electrode work function plays a very important role in the Junctionless devices also. Junctionless devices being a normally ON device, the work function difference between the channel (silicon fin) and gate electrode is supposed to deplete the channel (fin) at zero gate voltage for the proper operation of the device.

The effect of work function on conventional MOSFET and FinFET has been explored in the literature. For example, Hwang et al (2010) has explored the effect of work function on AC characteristics like $f_t$ and gate capacitance. As for as considering Junctionless transistors, research works on the variation in DC characteristics like threshold voltage, sub threshold slope (SS), DIBL and drive current with respect to gate length (both physical and effective), fin width, doping concentration, temperature and line edge roughness (LER) are available in the literature (Colinge et al 2009; Lee et al 2010; Lee et al 2010 b; Choi et al 2011; DeSouza et al 2011; Leung and Chui 2011). But, the effect of work function variation is yet to be explored in Junctionless devices.

The device input impedance also plays an important role in radio frequency circuit design since it defines both the power transfer and the noise equivalent circuit at a device’s input. This input impedance is a parallel-series combination of several capacitive and resistive components. It depends primarily on both the resistance of the physical poly-silicon gate and the channel resistance as seen from the gate but is not necessarily equal to their sum (Bandi et al 2006). The channel resistance is usually accounted for by
using NQS models (Ou et al 1998; Kordalski and Stefanski 2003). The output resistance is also one of the most important device parameters for analog applications.

In this chapter the impact of work function variation on DC and AC/Analog/RF characteristics in both conventional and Junctionless double gate devices is studied. $V_T$, $I_{ON}$, $I_{OFF}$ and $R_o$ are studied under DC parameters, and $f_t$, NQS delay, input impedance ($Z_{11}$), intrinsic gain and NF are studied under AC characteristics. Section 5.2 discusses about the description and calibration of the device. Section 5.3 discusses the simulation results and discussions. Finally Section 5.4 provides conclusion.

5.2 DEVICE DESCRIPTION AND CALIBRATION

All the simulations are carried out at 2D level. The device structures are generated using SDE. Figure 5.3(a) shows 2D structure of the conventional double gate (DG) transistor. Figure 5.3(b) depicts 2D structure of the Junctionless DG transistor.
Figure 5.3(a): 2D Structure of conventional DG
Figure 5.3 (b): 2D Structure of Junctionless DG
The doping dependent mobility models for conventional and Junctionless devices are included in the device simulations as already discussed in their corresponding chapters. Both the devices are calibrated against the published results (Kranti and Armstrong 2007; Lee et al 2010 a) by tuning the silicon parameter library file. After calibration, the device dimensions are brought to the requirements as given in Table 5.1.

**Table 5.1: Dimensions of the conventional and Junctionless DG**

<table>
<thead>
<tr>
<th>Process parameters</th>
<th>Conventional DG</th>
<th>Junctionless DG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Length ($L_g$)</td>
<td>30 nm</td>
<td></td>
</tr>
<tr>
<td>Fin Width (W)</td>
<td>10 nm</td>
<td></td>
</tr>
<tr>
<td>Gate oxide thickness ($T_{ox}$)</td>
<td>1 nm</td>
<td></td>
</tr>
<tr>
<td>Channel doping ($N_{ch}$)</td>
<td>$1 \times 10^{15}$/cm$^3$</td>
<td>$2 \times 10^{19}$/cm$^3$</td>
</tr>
<tr>
<td>Source/Drain doping ($N_{SD}$)</td>
<td>$1 \times 10^{20}$/cm$^3$</td>
<td>$2 \times 10^{19}$/cm$^3$</td>
</tr>
<tr>
<td>Supply Voltage ($V_{DD}$)</td>
<td>1 V</td>
<td></td>
</tr>
</tbody>
</table>

Figure 5.4 (a) and (b) show the simulated $I_D$-$V_G$ characteristics of DG FinFET and Junctionless FET in the log and linear scales, respectively. It can be seen from Figure 5.4(a) that $I_{OFF}$ of both the devices are matched to 0.59 nA/µm. It can be observed from Figure 5.4(b) that the Junctionless devices offer lesser $I_{ON}$ (997.5 µA/µm for FinFET and 676.5 µA/µm for Junctionless device) compared to inversion mode devices, for the given $I_{OFF}$.

Figure 5.4 (c) shows the simulated $I_G$-$V_G$ characteristics of DG FinFET and Junctionless FET. Figure 5.5 (a), (b) and (c) show the simulated $I_D$-$V_G$, $I_D$-$V_D$ and C-V characteristics respectively for MOSFET, FinFET and Junctionless FETs.
Figure 5.4(a): Simulated $I_D$-$V_G$ characteristics of DG devices of gate length 30 nm with matched $I_{OFF} = 0.59$ nA/µm (log scale)

Figure 5.4(b): Simulated $I_D$-$V_G$ characteristics of DG devices of gate length 30 nm (linear scale)
Figure 5.4(c): Simulated $I_G$-$V_G$ characteristics of DG devices of $T_{ox}=1\text{nm}$

Figure 5.5(a): Simulated $I_D$-$V_G$ characteristics of MOSFET, FinFET and Junctionless devices of $L_g=30\ \text{nm}$
Figure 5.5(b): Simulated $I_D$-$V_D$ characteristics of MOSFET, FinFET and Junctionless devices of $L_g = 30$ nm

Figure 5.5(c): Simulated C-V characteristics of MOSFET, FinFET and Junctionless devices of $L_g = 30$ nm
5.3 RESULTS AND DISCUSSION

The work function (WF) is varied from 4.4eV to 5eV and 5.3eV to 5.9eV for conventional and Junctionless devices respectively. Outside these ranges, threshold voltage of the devices either becomes too high resulting in very less $I_{ON}$ or too low resulting in too high $I_{OFF}$. DC parameters, $V_T$, $I_{ON}$, $I_{OFF}$ and $R_o$ and AC parameters $f_t$, NQS delay, $Z_{11}$, intrinsic gain and NF are extracted with respect to this work function variation, and are discussed below one by one. The bias points of $R_o$, NQS delay, $Z_{11}$, intrinsic gain and NF are fixed at $V_{DD}/2$.

5.3.1 Effect of Work Function on $V_T$, $I_{ON}$, $I_{OFF}$ and $R_o$

Figure 5.6 depicts the variation of $V_T$ with respect to work function for both the conventional and Junctionless devices. This $V_T$ extraction is done by means of peak $g_{in}$ method. It can be seen from Figure 5.6 that $V_T$ increases for both conventional and Junctionless device. Another observation from Figure 5.6 is that the work functions in the range of 4.6 eV to 5 eV for conventional FinFETs, and 5.3 eV to 5.8 eV for Junctionless FETs offers similar $V_T$. Figures 5.7 and 5.8 show the variation of conduction band energy along the channel for two WFs, for conventional DG and Junctionless DG respectively with drain at $V_{DS}=1$ V and gate at $V_{GS}=0$ V. Since the increase in WF provides more barriers, $V_T$ increases with WF. It can also be observed from Figure 5.6 that the rate of change in $V_T$ with respect to work function is slightly smaller in the Junctionless devices compared to conventional FinFETs. This behavior of the Junctionless devices may be attributed to its bulk conducting nature.
Figure 5.6: Variation of $V_T$ with respect to WF for conventional and Junctionless DG devices

Figure 5.7: Conduction band energy of conventional DG devices along the channel for two WFs
The increase in $V_T$ with respect to WF for the Junctionless can be reasoned out by observing the conduction band energy and electron density perpendicular to the channel at $V_{DS}= 1$ V and $V_{GS}=0$ V. Figure 5.9 depicts the conduction band energy of Junctionless DG which is taken perpendicular to the channel for different work functions at $V_{DS}= 1$ V and $V_{GS}=0$ V. It may be observed that as the work function is increased, the bands bend upwards more and more. Figure 5.10 depicts the electron density of Junctionless DG which is taken perpendicular to the channel for different work functions at $V_{DS}= 1$ V and $V_{GS}=0$ V. As the bends move upwards, the electron density gets decreased, resulting in the increase of $V_T$. This behavior is clearly seen in Figure 5.10. Figure 5.11 shows the electron density of conventional and Junctionless devices for the matched $I_{OFF}$. 
Figure 5.9: Conduction band energy of Junctionless DG devices perpendicular to the channel for different WFs at $V_{DS} = 1$ V and $V_{GS} = 0$ V

Figure 5.10: Electron density of Junctionless DG devices perpendicular to the channel for different WFs at $V_{DS} = 1$ V and $V_{GS} = 0$ V
Figure 5.11: Electron density of conventional and Junctionless DG devices

Figure 5.12 shows the variation of $I_{\text{ON}}$ w. r. t work function, for conventional and Junctionless devices. Since, $I_{\text{ON}}$ trades off with the $V_T$, the inverse behavior are expected with respect to WF variation. From Fig. 5.12 those work functions in the range of 4.7 eV to 5 eV for conventional FinFETs, and 5.3 eV to 5.7 eV for Junctionless FETs give similar $I_{\text{ON}}$. Similar to $V_T$ behavior, the rate of change in $I_{\text{ON}}$ with respect to work function change is smaller in Junctionless devices compared to conventional FinFETs. This can be again reasoned out in a similar manner as that of $V_T$ variation with respect to work function. Figure 5.13 shows the $I_{\text{OFF}}$ variation with respect to WF for conventional and Junctionless DG. The decrease in $I_{\text{OFF}}$ can be reasoned out with Figures 5.7 and 5.8. It may be observed from Fig. 5.7 and Fig. 5.8 that increase in WF provides more barriers resulting in the decreased $I_{\text{OFF}}$. 
Figure 5.12: Variation of $I_{ON}$ with respect to WF for conventional and Junctionless DG devices

Figure 5.13: Variation of $I_{OFF}$ with respect to WF for conventional and Junctionless DG devices
Figure 5.14 shows the output resistance versus work function plots of conventional and Junctionless devices, for different gate biases (0.2V, 0.4 V, 0.6V and 0.8V). Due to less DIBL, Junctionless devices offer higher output resistance, for the given bias. These low values of DIBL are attributed to the absence of a drain junction. The blocking of current flow in the off state is not due to a reverse-biased drain junction but to “squeezing” off the carriers out of the channel region. When the device is off, the drain-source voltage drop occurs in the drain itself, and not in the channel region (under the gate) as in a regular device. As already discussed in the Chapter 4, the influence of the drain electric field on the channel region is much smaller than in the inversion- mode device, resulting in a smaller DIBL.

![Figure 5.14: Variation of $R_o$ with respect to WF for conventional and Junctionless DG devices](image)

**Figure 5.14: Variation of $R_o$ with respect to WF for conventional and Junctionless DG devices**
5.3.2 Effect of Work Function on $f_t$, NQS delay, $Z_{II}$, Intrinsic Gain and NF

Figure 5.15 depicts the $f_t$ variation with respect to work function. It can be observed from Fig. 5.15 that $f_t$ in conventional devices is almost independent of work function variation. But, the Junctionless devices show variation in $f_t$ when work function is changed. Gate capacitance ($C_{gg}$) in conventional devices is less significant to work function because of the screening effect which is normally observed in the inversion mode devices (Hwang et al 2009). $f_t$ also does not show any significant change with respect to work function. But, $C_{gg}$ in Junctionless devices show significant dependency on work function. $C_{gg}$ combined with the trans-conductance ($g_m$) at bias points where $f_t$ is extracted, results in the $f_t$ behavior with respect to work function as is shown in Figure 5.15.

Figure 5.15: Variation of $f_t$ with respect to WF for conventional and Junctionless DG devices
Figure 5.16 shows the NQS delay versus work function graphs of conventional and Junctionless devices, for 200 GHz. For both the devices, the NQS delay increases as expected. Towards the higher work function values both conventional and Junctionless transistors faces huge NQS delay. Towards the lower range of work function, the NQS delay of Junctionless devices is more sensitive to work function variation compared to conventional FinFETs.

Figure 5.16: Variation of NQS delay with respect to WF for conventional and Junctionless DG devices
Figures 5.17 and 5.18 depict the real part (Re $Z_{11}$) and imaginary (Im $Z_{11}$) part of the input impedance ($Z_{11}$) versus work function, for the conventional and Junctionless devices for two different frequencies, 1GHz and 10 GHz. (Re $Z_{11}$ and Im $Z_{11}$ are calculated from the standard AC simulations. TCAD simulation yields Y-parameter matrix which are converted into Z-parameter using standard formulae).

The input impedance may be given by the following expression (Ponton et al 2009).

$$Z_{11} = \frac{1}{g_m} \frac{1}{1+ j \frac{f}{f_t} + \frac{f_t}{2}} \quad (5.4)$$

The above expression can be used only for reasoning out the trends of the Figure 5.17 and 5.18. They need not predict the correct values of input impedance i.e., Re $Z_{11}$ is inversely proportional to $g_m$ and $g_m$ decreases with respect to work function as shown in Figure 5.19. The combined behavior of $g_m$ and $f_t$ (which is again a function of $g_m$, and also $C_{gg}$) give rise to the trends seen in the Figures 5.17 and 5.18. It has been reported that $g_m$ for Junctionless devices is lower compared to conventional devices (Doria et al 2011). So it is expected that the Junctionless devices will show larger Re $Z_{11}$ and Im $Z_{11}$ compared to conventional devices.
Figure 5.17: Variation of real part of $Z_{11}$ with respect to WF for conventional and Junctionless DG devices

Figure 5.18: Variation of imaginary part of $Z_{11}$ with respect to WF for conventional and Junctionless DG devices
Figure 5.19: Variation of $g_m$ with respect to WF for conventional and Junctionless DG devices

Figure 5.20 depicts the graph of the variation of intrinsic gain with respect to WF for conventional and Junctionless devices. It can be seen that gain increases for both the devices. As the work function increases $g_m$ decreases whereas $R_o$ increases and $R_o$ dominates throughout the range of work function considered in this study. This results in the increased intrinsic gain. Figure 5.21 depicts the graph of the variation of NF with respect to WF for conventional and Junctionless devices. It is observed that for conventional transistor NF increases with respect to WF and for Junctionless devices, NF decreases with respect to WF.

This behavior can be understood by plotting the alpha and $S_{dd}^I$ used in the noise figure extraction (Refer Equation 2.8) as a function of work function. Alpha versus work function plots for conventional device shows an increasing trend while a flat trend is observed for Junctionless device (Fig. 5.22). $S_{dd}^I$ is plotted in Fig. 5.23 which decreases with work function for both the devices. The combined behavior is reflected in the noise figure versus work function graphs.
Figure 5.20: Variation of intrinsic gain with respect to WF for conventional and Junctionless DG devices

Figure 5.21: Variation of NF with respect to WF for conventional and Junctionless DG devices
Figure 5.22: Variation of alpha with respect to WF for conventional and Junctionless DG devices

Figure 5.23: Variation of $S_{dd}$ with respect to WF for conventional and Junctionless DG devices
To make it formal, the work function of the nominal devices (both conventional and Junctionless) are varied by ±10% to get the sensitivities with respect to \( f_t \), NQS delay, intrinsic gain and NF. These results are as expected i.e. the Junctionless devices are more sensitive compared to conventional double gate devices with respect to all the response parameters.

5.4 CONCLUSION

The effect of gate electrode work function on DC and AC parameters are studied in 30 nm gate length conventional and Junctionless double gate devices. Junctionless devices being bulk conducting device, behaves differently with respect to work function variation compared to surface conducting conventional devices. In general, the Junctionless devices are more sensitive to gate electrode work function variation. With respect to \( f_t \), the change is 0.1 GHz and 4 GHz for ±10 % variation in the work function, for conventional and Junctionless devices respectively. Similarly for NQS delay, the change is 11° and 15°, and for intrinsic gain the change is 34 and 77, and for NF the change is 0.3dB and 1dB, for ± 10 % change in the work function from the nominal value, for conventional and Junctionless devices respectively.