CHAPTER 4

NEW OTRA BASED WAVEFORM GENERATORS

4.1 INTRODUCTION

Sinusoidal/square wave generator circuits are the most important building blocks in the design of analogue and digital integrated circuits. These waveform generators find many applications in communication, instrumentation and measurement, and control systems. Sinusoidal/square waveform generators along with other circuits are often employed to produce various standard signals, such as triangular wave, pulse wave, square, saw tooth etc. [1-3]. These signals can be used as a test signal for the automatic test and measurement, a local oscillator for frequency translation, clock pulses for digital circuits and also in audio and speech processing. Moreover, the generated signals with phase noise become the most important in frequency domain for the radio frequency (RF) applications.

Signal generator or oscillators can be classified as

i) Sinusoidal/linear/harmonic oscillators

ii) Non-sinusoidal/non-linear/relaxation oscillator

This chapter is devoted to the realization of some novel active circuits by using an operational transresistance amplifier (OTRA). At first, the discussion begins with the realization of novel sinusoidal oscillator circuits based on a generalized configuration which is followed by two novel quadrature sinusoidal oscillator realizations. At last, the chapter ends with the design description of two new square-wave generators based on single OTRA.

4.2 SINUSOIDAL OSCILLATORS USING SINGLE OTRA

Sinusoidal oscillators are essential parts in many electronic systems. It can be used in testing, instrumentation and telecommunication systems. An electronic device that generates sinusoidal oscillations of desired frequency is known as sinusoidal oscillator. The period or frequency of the oscillator is determined by the external circuitry. Most of the oscillators can be viewed as feedback circuits, where part of the output signal is ‘feedback’ to the input signal. The functional block diagram of the sinusoidal oscillator with positive feedback is shown in Fig. 4.1.

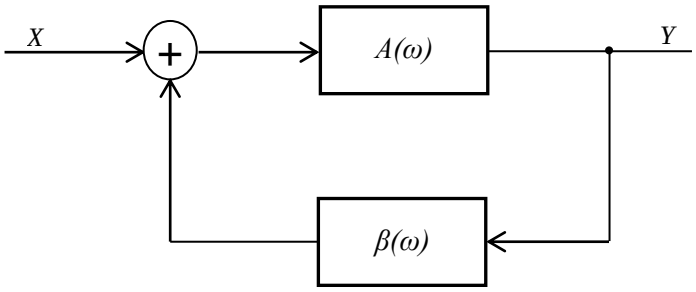


Fig. 4.1 Functional block diagram of a sinusoidal oscillator

A(ω) and β(ω) are the gains of the amplifier and frequency selective feedback network respectively. *X* and *Y* are the input and output signals. The closed loop transfer function of the block diagram shown in Fig. 4.1 becomes

$$\frac{Y}{X} = \frac{A(\omega)}{1 - A(\omega)\beta(\omega)} \tag{4.1}$$

From equation (4.1), the characteristic equation can be written as

$$1 - A(\omega)\beta(\omega) = 0 \tag{4.2}$$

According to the Barkhausen criterion, the system will sustain steady-state oscillations at a specific frequency only when the open-loop gain is equal to unity $A(\omega)\beta(\omega) = 1$. At this condition, the closed-loop gain becomes infinite and produces a finite output for the zero input signals. The Barkhausen criterion is widely used in the design of electronic oscillators and also in the design of the feedback circuits to prevent them from oscillations. All the proposed sinusoidal oscillator circuits in the following subsections satisfied the Barkhausen criterion.

4.2.1 GROUNDED RESISTANCE/CAPACITANCE SINUSOIDAL OSCILLATORS

In the previous chapters, some sinusoidal oscillators based on OTRA with some disadvantages were discussed. However, during the study of the sinusoidal oscillator circuits available in the literature, it was found that a generalized configuration can be implemented to generate more number of sinusoidal oscillators with a grounded resistance or capacitance. The proposed generalized configuration for generating sinusoidal oscillator is shown in Fig. 4.2.

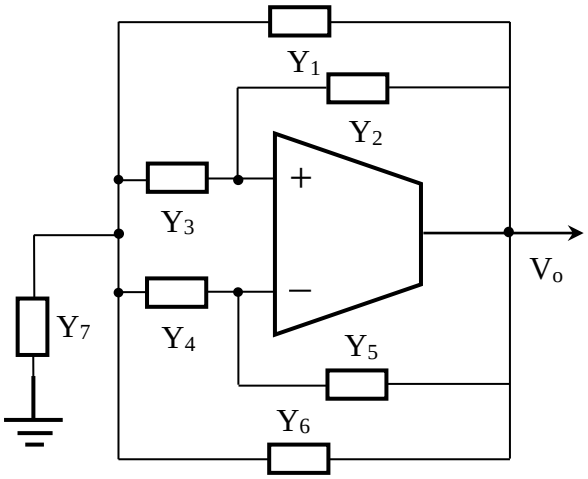


Fig. 4.2 Generalized configuration of the Single OTRA based sinusoidal oscillators

Several oscillator circuits can be generated by exploiting the generalized configuration shown in Fig. 4.2. By substituting the resistors and capacitors in place of Y_i (where i = 1 to 7) several oscillator circuits can be realized. The minimum component oscillator circuit generated from the generalized configuration is shown in Fig. 4.3.

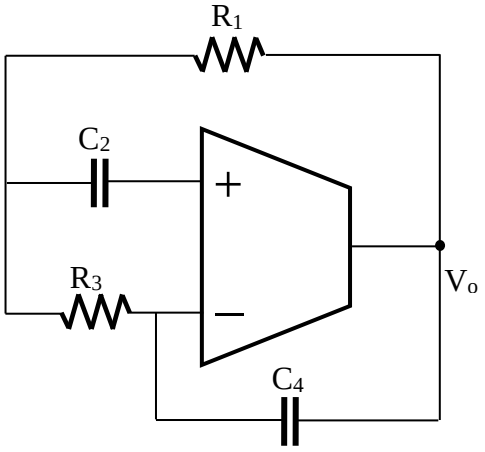


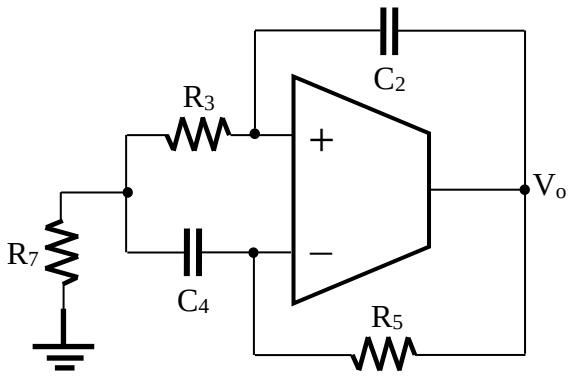
Fig. 4.3 Minimum component RC sinusoidal oscillator

The oscillator circuit shown in Fig. 4.3 can also be called as minimum passive component RC sinusoidal oscillator circuits. The admittance values chosen for the Fig. 4.3 are $Y_1 = G_1$, $Y_2 = 0$, $Y_3 = sC_2$, $Y_4 = G_3$, $Y_5 = sC_4$, $Y_6 = 0$ *and* $Y_7 = 0$. This circuit generates oscillations with two resistors, two capacitors and one OTRA. By proper selection of the admittances Y_1, Y_2, Y_3, Y_4, Y_5, Y_6 and Y_7 of the generalized configuration shown in Fig. 4.2, many oscillator circuits can be realized. Some-of the

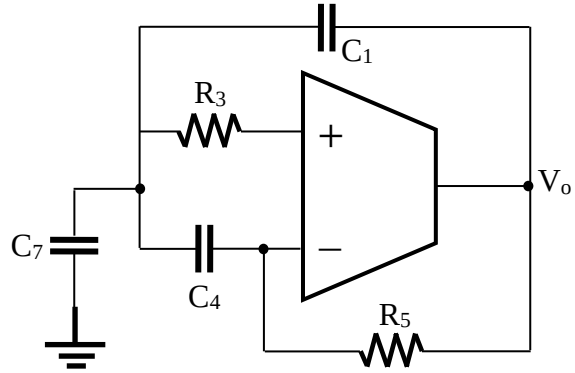
useful oscillator circuits generated from the generalized configuration with the admittances shown in Table. 4.1 are shown in Fig. 4. 4

Table. 4.1 Selected passive components for the generalized configuration shown in 4.2

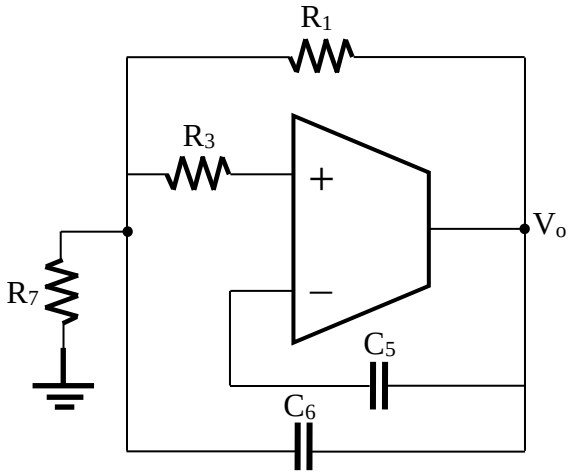
Proposed designs	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
(a)	0	sC_2	R_3	sC_4	R_5	0	R_7
(b)	sC_1	0	R_3	sC_4	R_5	0	sC_7
(c)	R_1	0	R_3	0	sC_5	sC_6	R_7
(d)	0	R_2	R_3	sC_4	R_5	sC_6	R_7
(e)	0	R_2	sC_3	R_4	0	sC_6	R_7
(f)	0	sC_2	R_3	sC_4	R_5	R_6	R_7
(g)	0	sC_2	R_3	sC_4	0	R_6	R_7
(h)	sC_1	R_2	sC_3	R_4	R_5	0	0
(i)	sC_1	sC_2	R_3	R_4	R_5	0	0
Y_i's are admittance of passive components							



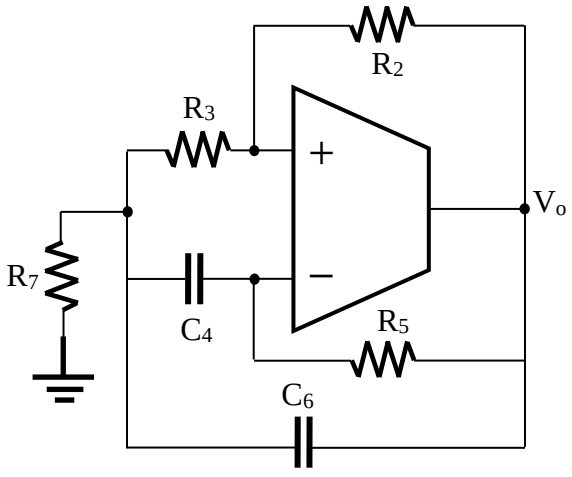
(a) Proposed oscillator circuit-I



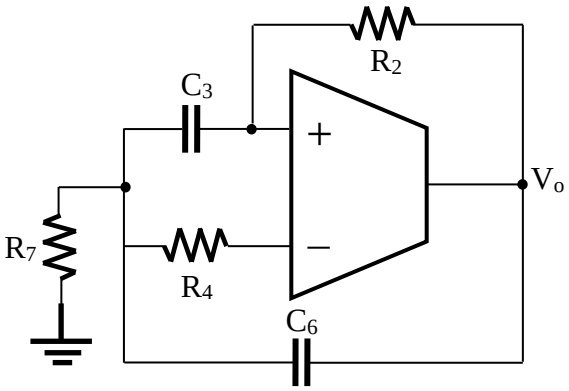
(b) Proposed oscillator circuit-II



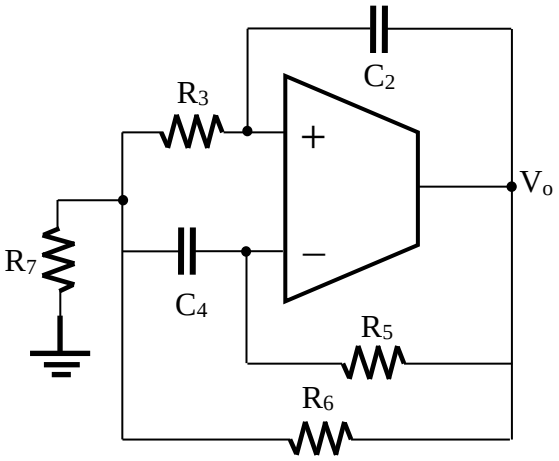
(c) Proposed oscillator circuit-III



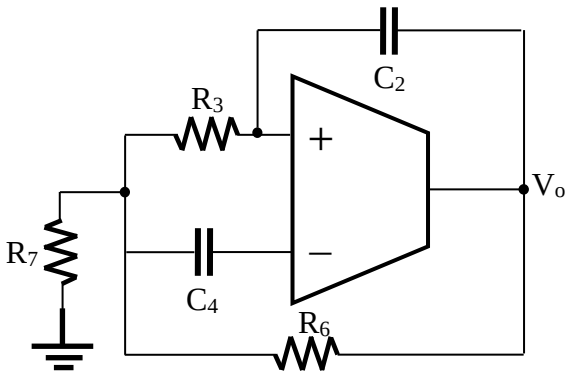
(d) Proposed oscillator circuit-IV



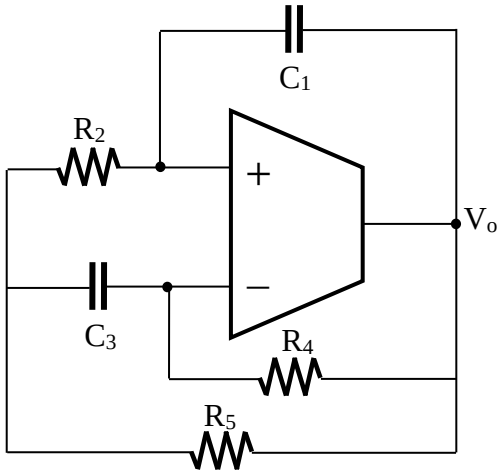
(e) Proposed oscillator circuit-V



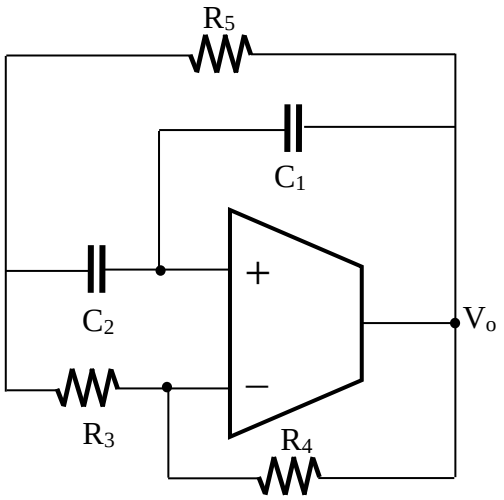
(f) Proposed oscillator circuit-VI



(g) Proposed oscillator circuit-VII



(h) Proposed oscillator circuit-VIII

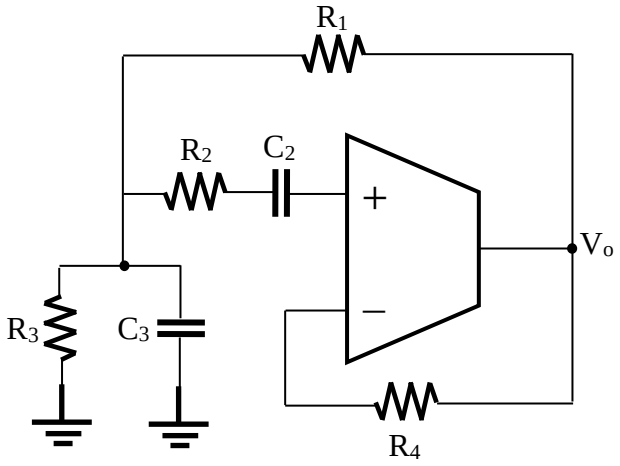


(i) Proposed oscillator circuit-IX

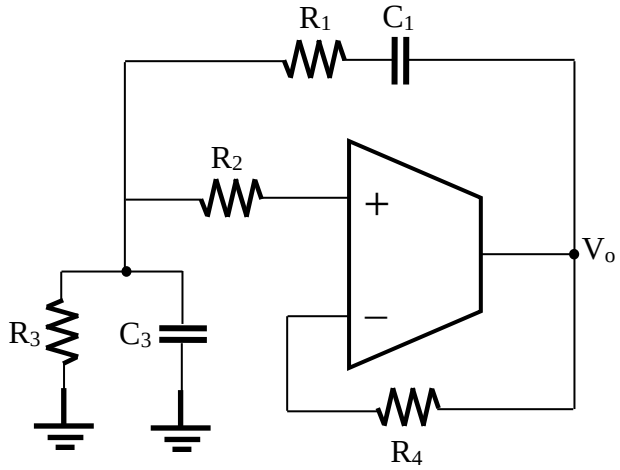
Fig. 4.4 Oscillator circuits realized from the generalized configuration

The advantage of the proposed circuits in Fig. 4.4 is a grounded resistance R_7, which can be replaced with a grounded capacitor or a JFET (Junction Field Effect Transistor) to realize a voltage controlled oscillator. Two grounded passive component oscillators can also be derived from the generalized configuration shown in Fig. 4.2. The proposed resistance and capacitance grounded sinusoidal oscillators are shown in Fig. 4.5 (a) and (b).

The proposed resistance and capacitance grounded sinusoidal oscillator circuits require single OTRA and six passive components to generate the oscillations.



(a) Grounded resistance and capacitance oscillator-I



(b) Grounded resistance and capacitance oscillator-II

Fig. 4.5 Grounded resistance and capacitance sinusoidal oscillators

4.3 QUADRATURE SINUSOIDAL OSCILLATORS

Quadrature oscillator is an important building block for many electronics and communication applications. A quadrature oscillator typically provides two sinusoids with a 90^o phase difference, which is useful in telecommunications for quadrature mixer, in single-sideband generators, in direct-conversion receivers, used for measurement purposes in vector generators or selective voltmeters.

The principle of quadrature generation is to couple two oscillators and injecting a portion of each oscillators output with the same frequency into other oscillator, such that they operate with a 90^o phase shift. Quadrature oscillators can be designed as either second order or third order oscillators. The major advantage of the second order

oscillators is compact realization with less number of passive components and active components.

4.3.1 PROPOSED QUADRATURE OSCILLATOR CIRCUITS

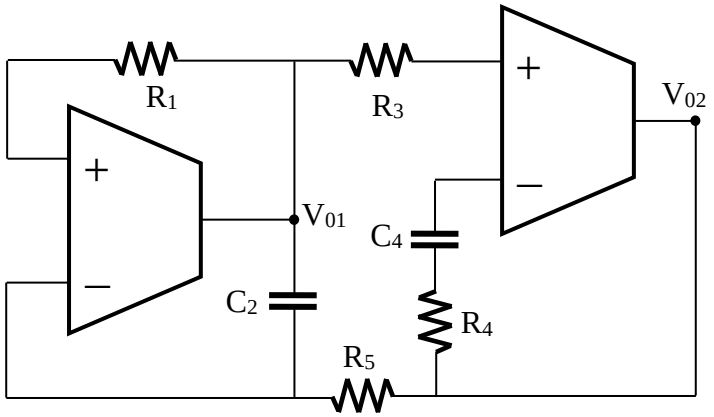


Fig. 4.6 Proposed quadrature sinusoidal oscillator circuit-I

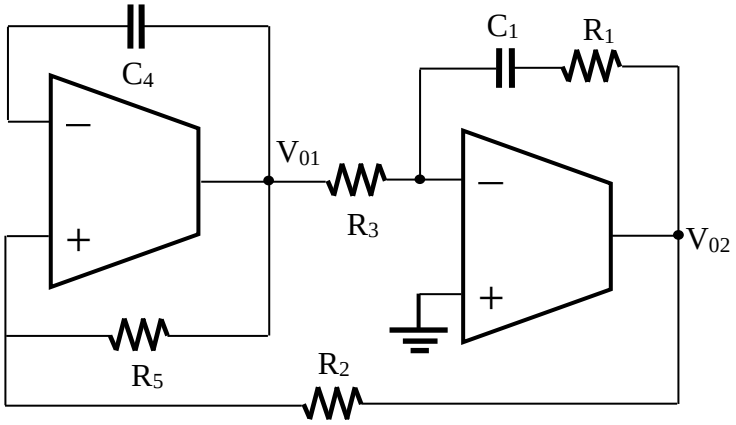


Fig. 4.7 Proposed quadrature sinusoidal oscillator circuit-II

The proposed quadrature sinusoidal oscillators are shown in Fig. 4.6 and Fig. 4.7. These quadrature oscillators require two OTRAs and few passive components to generate the oscillations with 90^{o} phase shift.

4.4 SQUARE WAVEFORM GENERATORS

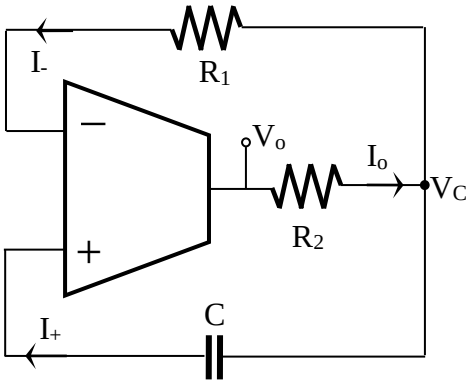
A square waveform is a kind of non-sinusoidal waveform, most commonly used in electronics and signal processing applications. An ideal square wave alternates regularly and instantaneously between two saturation levels. Square waves are usually encountered in digital switching circuits for triggering synchronous logic circuits at

precisely determined logic intervals. They are used as timing references or clock signals, because of their fast transitions between bollen logic levels (1's and 0's). Square waveform generators along with other circuits are able to generate triangular, saw-tooth and pulse waveforms.

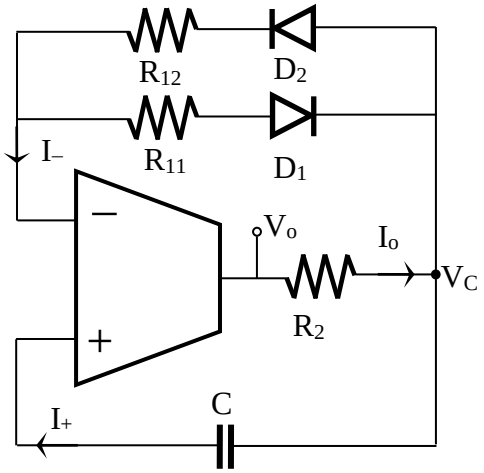
4.4.1 PROPOSED SQUARE WAVEFORM GENERATOR CIRCUITS

The proposed square wave generators are shown in Fig. 4.8. The first proposed circuit in Fig. 4.8 (a) is designed with one OTRA, and a few passive components. This circuit shown in Fig. 4.8 (a) can be able to produce the square waveform with almost equal and fixed on-duty and off-duty cycles. The proposed circuit in Fig. 4.8 (b) is to contrive by using one OTRA, two diodes and a few passive components. The second proposed circuit in Fig. 4.8 (b) is adroit to vary on-duty and off-duty cycles independently. The working principle of the proposed circuits can be explained with the expected output waveform shown in Fig. 4.9.

From Fig. 4.9, it could be construed that the output square-wave (V_o) has two saturation levels V_{sat}^{+} and V_{sat}^{-}. Assuming initially, V_o is at any one of these two saturation levels. If the output voltage V_o is at negative saturation level V_{sat}^{-} and changing it's state from V_{sat}^{-} to V_{sat}^{+}, which indicates that the current at the non-inverting terminal I_+ becomes more than the current at the inverting terminal I_- of the OTRA. At this moment, the voltage V_C of the capacitor C starts to increase from the lower threshold value V_{TL} to the final value V_{sat}^{+}. At the end of on-duty cycle, the capacitor voltage V_C is charged up to the upper threshold voltage V_{TH}, instead of V_{sat}^{+}.



(a) Square waveform generator-I



(b) Square waveform generator-II

Fig. 4.8 Proposed square waveform generator circuits

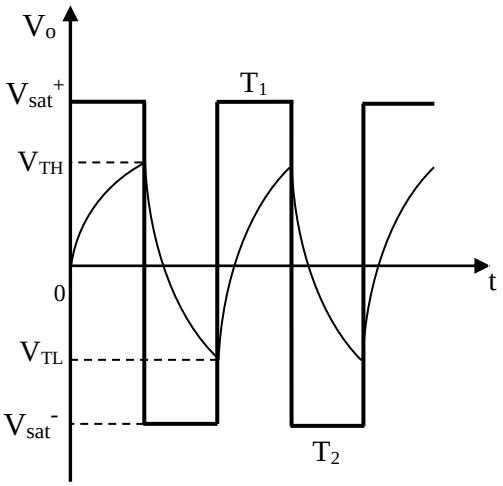


Fig. 4.9 Expected output waveform of the proposed square-wave generators

At this point of time, the current at the non-inverting terminal I_+ becomes less than the current at the inverting terminal I_- of the OTRA. Then the output changes its state from the upper saturation level V_{sat}^+ to the lower saturation level V_{sat}^- and the capacitor voltage V_C will start discharging to the lower threshold value V_{TL} instead of V_{sat}^-. Hence, the output voltage V_o changes its state from the on-duty cycle or higher saturation level V_{sat}^+ to off-duty cycle or lower saturation level V_{sat}^- when the non-inverting terminal current is equal to the inverting terminal current $I_+ = I_-$.

4.5 SUMMARY

In this chapter, the designs of new OTRA based waveform generators are presented. A generalized configuration to realize sinusoidal oscillators is presented with a single OTRA. Several possible realizations of sinusoidal oscillator circuits from the generalized configuration are discussed. All the presented sinusoidal oscillator circuits entail single OTRA. Twelve sinusoidal oscillators are realized from the generalized configuration.

In these twelve oscillator circuits, seven oscillator circuits are realized with a grounded passive component. Two special case oscillator circuits are also presented in this chapter with grounded resistance and capacitance. Most of the oscillator circuits realized from the generalized configuration is able to control the condition of oscillation and frequency of oscillation independently. In addition to the above oscillator circuits, two quadrature sinusoidal oscillator circuits are presented in this chapter. The proposed quadrature sinusoidal oscillators have the advantage of controlling the condition of oscillation and frequency of oscillation independently. At the end, two square waveform generators along with a few passive components are presented. The working of square waveform generator circuits and the transaction between the positive saturation level and negative saturation level is discussed in detail. The mathematical analysis of the newly proposed circuits is given in the next chapter.