

OPERATIONAL TRANSRESISTANCE AMPLIFIER (OTRA)

2.1 INTRODUCTION

As signal processing extends to higher frequencies, circuit designers are detected, that the traditional design methods based on voltage op-amps are no longer adequate. It is well known that the traditional operational amplifiers have a bandwidth which is dependent on the closed loop voltage gain [1-7]. The attempt to overcome this problem has led to the interest in circuits which operate in current-mode. These circuits employ current processing techniques to improve dynamic speed capability, providing a constant bandwidth virtually independent of the gain. In the last decade, a new current mode device called an operational transresistance amplifier attracted considerable attention of the analogue IC designers. The operational transresistance amplifier is a high gain current input and voltage output analogue building block [31-44]. The circuit symbol of the OTRA is shown in Fig. 2.1. The input and output terminal relations of an OTRA can be characterized by matrix given below Fig. 2.1. For ideal operation, the transresistance gain R_m approaches infinity forcing the input currents to be equal. Low input and output impedances, a bandwidth independent of the device gain can be considered as the main advantage of the OTRA. Current differencing amplifier and Norton amplifier are the commercially available names of OTRA. These commercial realizations allow input current to flow only in one direction and do not have internal ground at the input terminals. The former disadvantage, limited the functionality of the OTRA, whereas, the latter forced to use external DC bias current leading complex and unattractive designs.

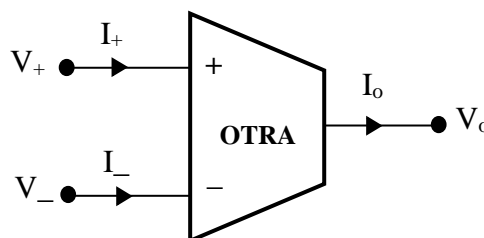


Fig. 2.1 OTRA circuit symbol

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_o \end{bmatrix} \quad (2.1)$$

$$V_+ = V_- = 0 \quad (2.2)$$

$$V_o = I_+ R_m - I_- R_m \quad (2.3)$$

In order to overcome these disadvantages of the OTRA, some topologies are proposed in the literature, second generation current conveyor based OTRA implementation is proposed in [32, 35] and [36]. A new norton amplifier based OTRA on current follower configuration with class-AB output stage for low power realization is proposed in [37] and also shows a fully differential implementation to reduce the accurate matching required for current matching. A new CMOS fully differential OTRA design for the low voltage with low power supplies in the submicron technology is reported in [41].

2.2 CMOS OPERATIONAL TRANSRESISTANCE AMPLIFIER (OTRA)

2.2.1 SALAMA OTRA

In OTRA both the input and output terminals are characterized by low impedance, thereby eliminating response limitations incurred by capacitive time constants. The input terminals are virtually grounded leading to circuits that are insensitive to stray capacitance. Ideally, the transresistance gain, R_m , approaches infinity and forces the two input currents I_+ and I_- to be equal. Practically, the transresistance gain is finite and its effect should be considered along with finite input resistance, output resistance and the frequency limitations associated with the OTRA. Fig. 2.2 shows a simple, non-ideal model of the OTRA with a finite input and output resistance. The input terminals are not virtually grounded, but at a finite voltage determined by the finite input resistance. Also the output voltage is determined by the finite output resistance and the input offset difference current.

Salama *et al.*, proposed a CMOS OTRA circuit based on the modified differential current conveyor circuit (MDCC) and a common source amplifier [32]. The common source amplifier provides the high gain stage and MDCC provides the current

differencing operation. The CMOS implementing of salama OTRA is shown in Fig. 2.3.

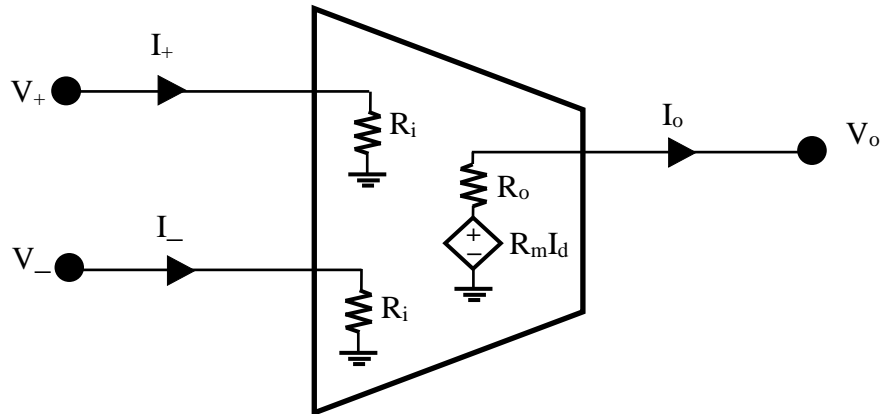


Fig. 2.2 Non-ideal model of OTRA

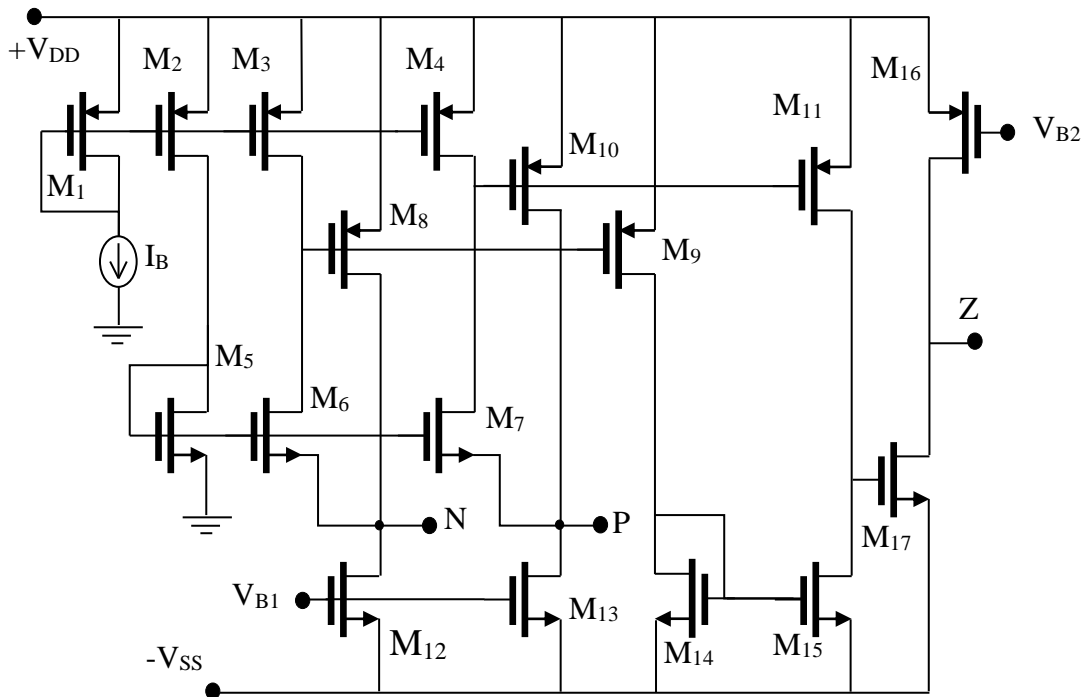


Fig. 2.3 CMOS implementation of the Salama OTRA

Assuming all the transistors are operating in the saturation region, the circuit operation can be explained as follows. The current mirror formed by (M_1-M_4) forces equal current (I_B) in the transistors M_5 , M_6 and M_7 . This operation derives the gate to source voltages of M_5 , M_6 and M_7 to be equal and, consequently, forces the two input terminals to be virtually grounded. The current mirrors formed by the transistor pairs M_3 and M_4 ; M_8 and M_9 ; M_{10} and M_{11} ; M_{14} and M_{15} provide the current differencing

operation, whereas, the common source amplifier formed by M_{17} achieves the high gain stage. The current biasing I_B , is connected to the transistors M_1 with common gate and thus biases the transistors M_1 to M_4 . Transistors M_3, M_6, M_8, M_9 and M_4, M_7, M_{10}, M_{11} form two loops which transmit the current I_P and I_N respectively. Hence the output voltage is produced with currents of M_9 and M_{11} , which biases the output stage transistors in the OTRA design.

2.2.2 SIMULATION RESULTS

The performance of the Salama OTRA is simulated using Cadence Spectre simulation models and its basic functionality with a central value of specifications at a specific biasing and sizing conditions of the circuit is estimated.

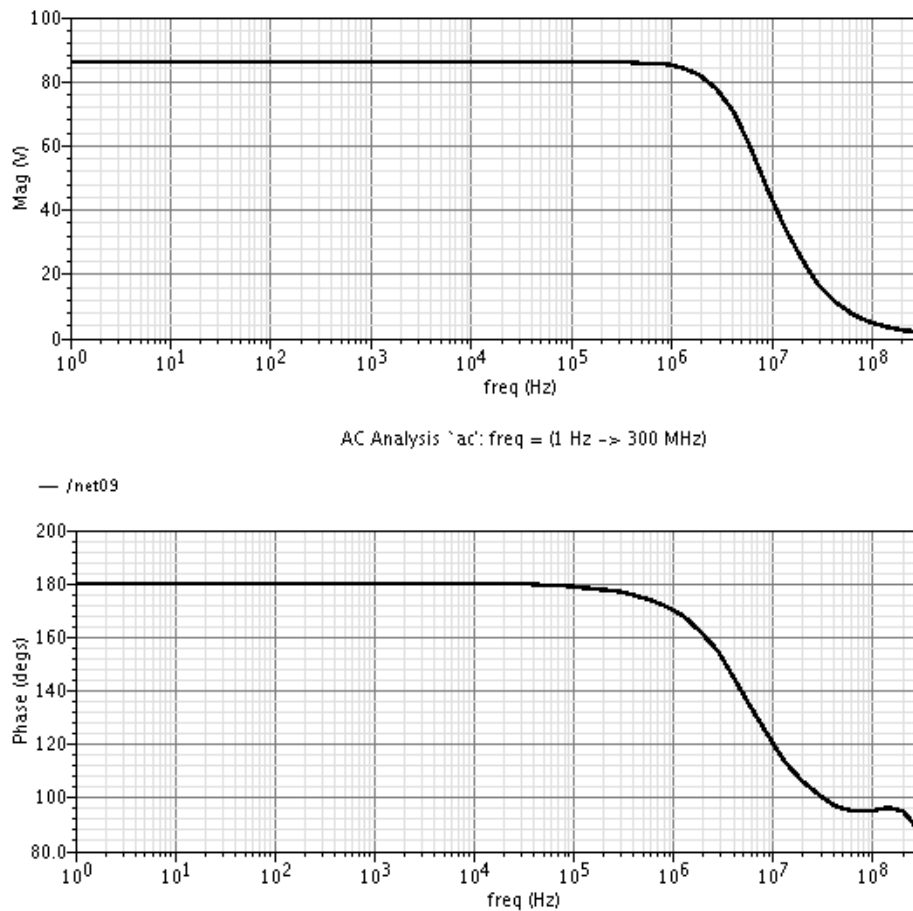


Fig. 2.4 Frequency response of the Salama OTRA

The biasing current $I_B = 5 \mu\text{A}$, biasing voltages $V_{B1} = -1 \text{ V}$ and $V_{B2} = 1.8 \text{ V}$ are used for the simulation of Salama OTRA. Fig. 2.4 shows the magnitude and phase response simulation results of the Salma OTRA. From this AC characteristic, the open loop transresistance gain of the OTRA is $80.1 \text{ dB}\Omega$ and the transresistance gain bandwidth is 11.3 MHz . Fig. 2.5 shows the output voltage of the OTRA for different

values of inverting input and non-inverting input currents. From this plot, the input current differential range is from $-30 \mu\text{A}$ to $+30 \mu\text{A}$. The input resistance plot for the Salama OTRA is shown in Fig. 2.6 and the output resistance plot is shown in Fig. 2.7. The Salama OTRA is simulated with a supply voltage of $\pm 1.8 \text{ V}$.

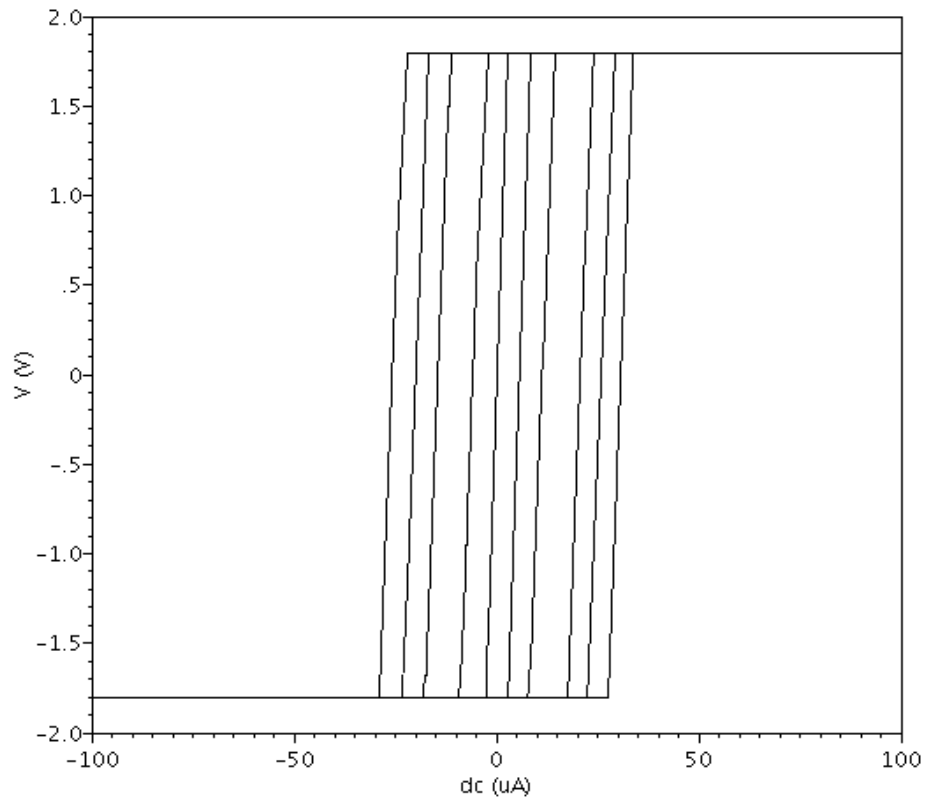


Fig. 2.5 Output voltage at terminal Z in Fig. 2.3

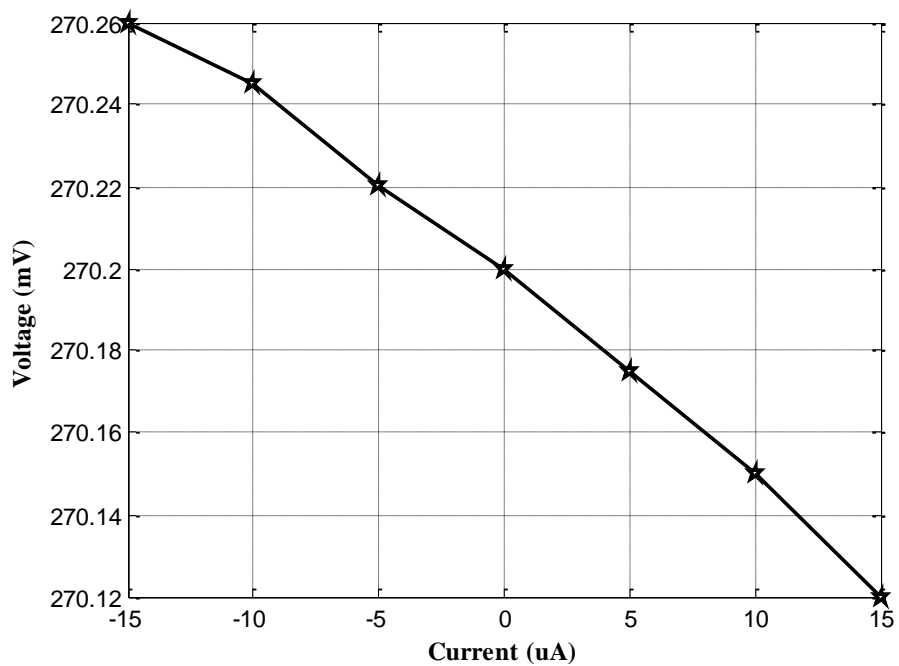


Fig. 2.6 Input resistance plot for the circuit in Fig. 2.3

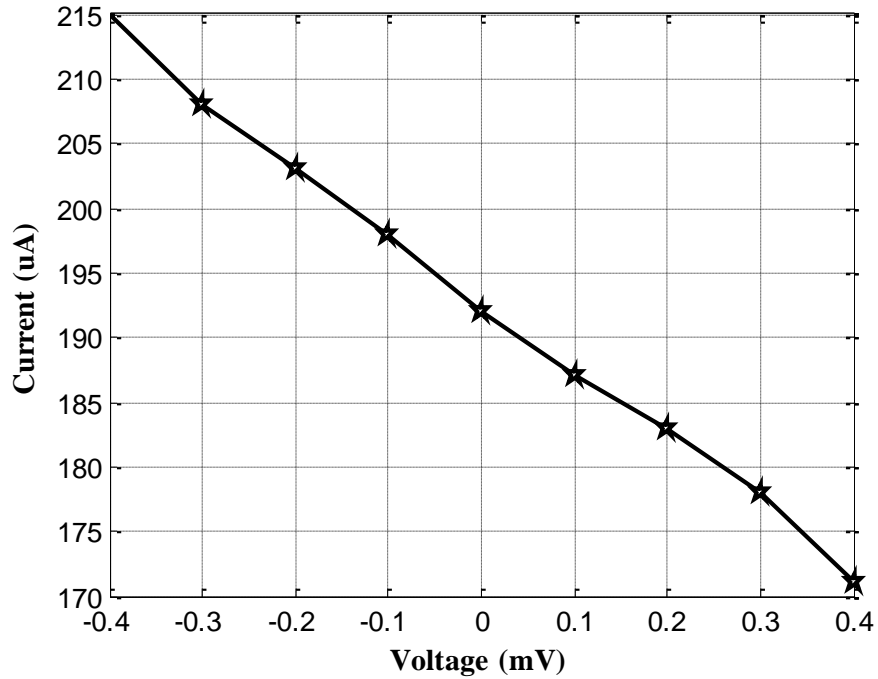


Fig. 2.7 Output resistance plot for the circuit in Fig. 2.3

2.2.3 OTRA USING A CURRENT DIFFERENCING BUFFERED AMPLIFIER

Ali Toker *et al.*, proposed a new CMOS implementation for current differencing buffered amplifier (CDBA) in [33]. The CDBA can easily be implemented by CMOS transistors by using the configuration shown in Fig. 2.8. This CDBA CMOS implementation can also be used as OTRA and current feedback operational amplifier (CFOA). This CMOS implementation consists of a differential current controlled current source (DCCCS) followed by a voltage buffer. Assuming all the transistors are in the saturation region, the circuit operation is explained as follows. The current mirrors formed by the transistors M_1 , M_3 and M_5 forces equal currents in the transistors M_9 and M_{10} . The current mirrors M_2 , M_4 and M_6 forces equal current in the transistors M_7 and M_8 . M_1 and M_2 transistors sources are connected to ground. This operation makes the gate to source voltages of the transistors M_1 - M_6 to be equal and consequently, forces the two input terminals to be virtually grounded. The current mirror transistors from M_1 to M_{10} and transistors M_{11} and M_{12} provides current differencing operation, whereas, the rest of the circuit provides a high gain stage. The bias currents I_0 are given to biases the transistors M_1 - M_6 . By removing the output terminal W in the CMOS implementation shown in Fig. 2.8, it will be converted as OTRA. The transistor M_5 and M_6 can be removed to form a CFOA.

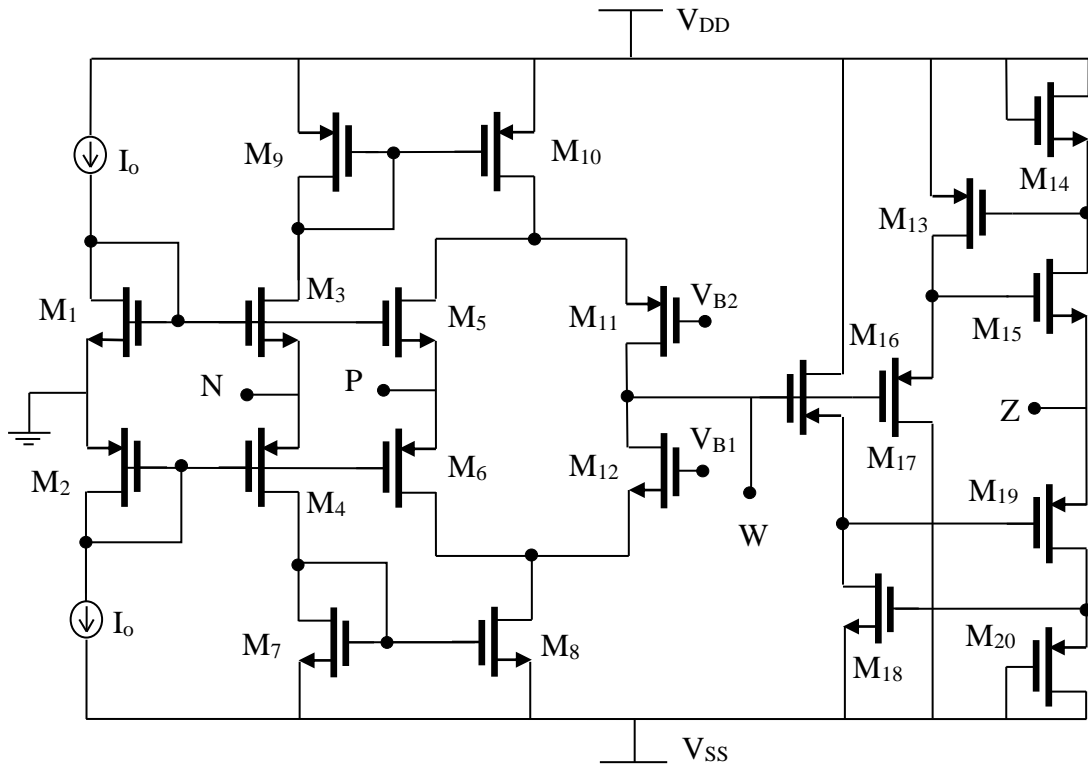


Fig. 2.8 Device level implementation of OTRA

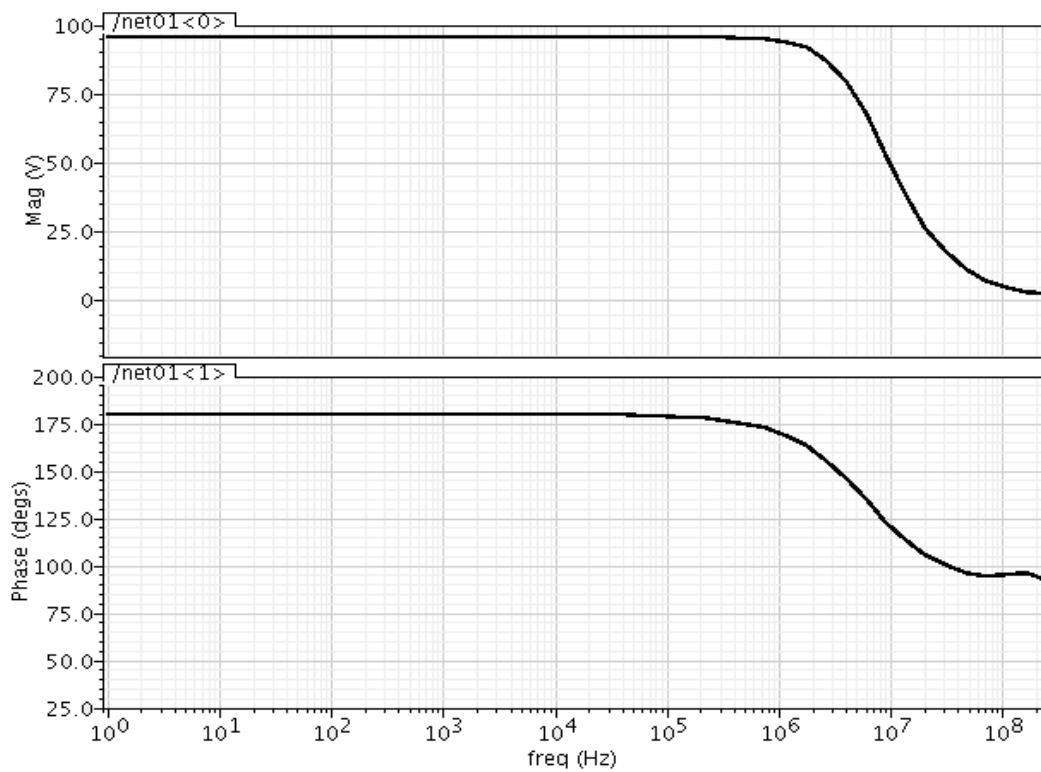


Fig. 2.9 Frequency response of the CMOS circuit shown in Fig. 2.8

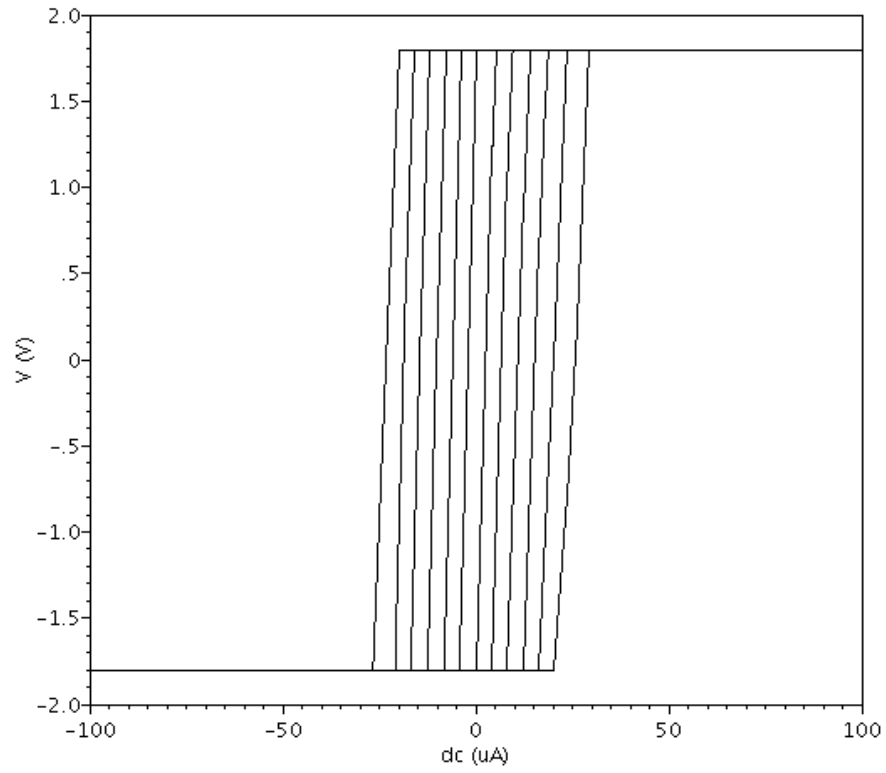


Fig. 2.10 Output voltage at terminal Z in Fig. 2.8

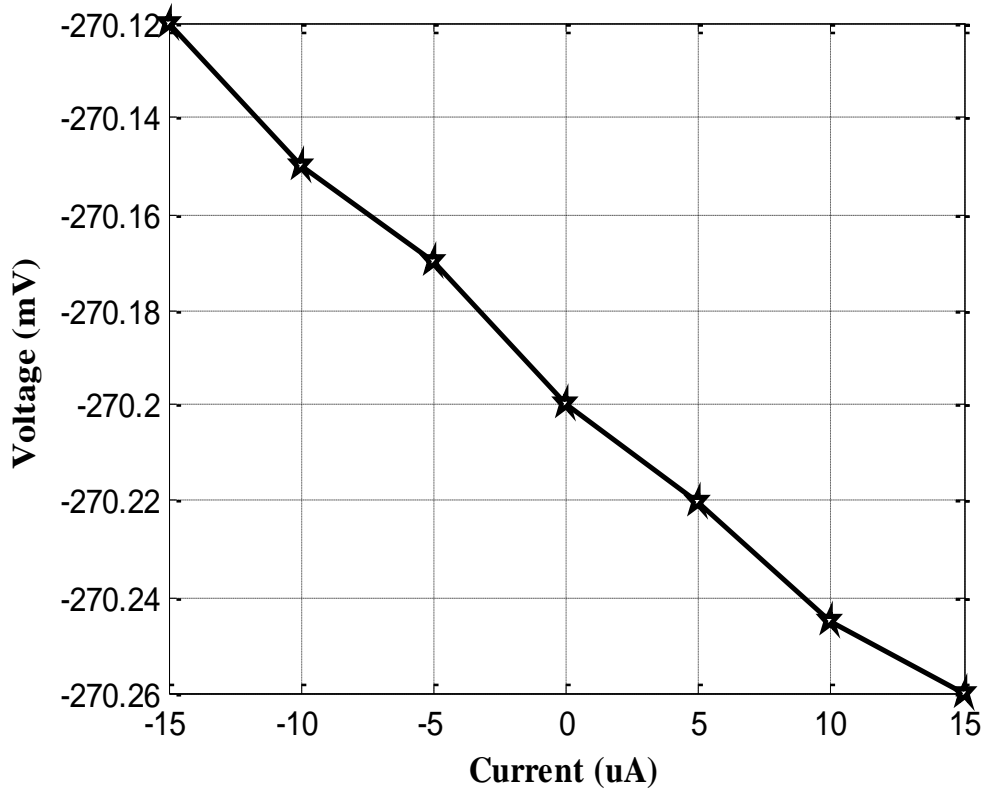


Fig. 2.11 Input resistance plot for the circuit shown in Fig. 2.8

2.2.4 SIMULATION RESULTS

The functionality of the CMOS OTRA shown in Fig. 2.8 is simulated by using Cadence Spectre simulation models. The biasing current $I_o = 20 \mu\text{A}$, biasing voltage $V_{g1} = 0.8 \text{ V}$ and $V_{g2} = -0.8 \text{ V}$ with a supply voltage of $\pm 1.8 \text{ V}$ is applied to the CMOS circuit shown in Fig. 2.8. The magnitude and phase response simulation results of the OTRA depicted in Fig. 2.8 is shown in Fig. 2.9. From this AC characteristic, the open loop transresistance gain of the OTRA is $93.31 \text{ dB}\Omega$ and the transresistance gain bandwidth is 5.3 MHz . The output voltage of the OTRA for different values of inverting input and non-inverting input currents is shown in Fig. 2.10. The input and output resistance plots are shown in Fig. 2.11 and 2.12.

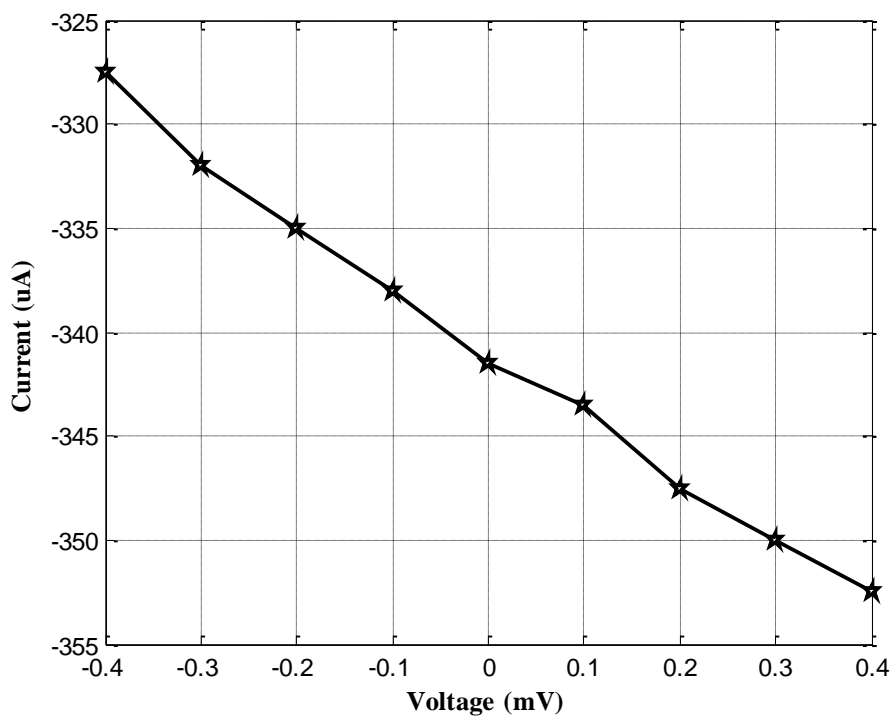


Fig. 2.12 Output resistance plot for the circuit shown in Fig. 2.8

2.3 OTRA IMPLEMENTATION USING IC AD 844

The operational transresistance amplifier can also be implemented using the commercially available IC called a current feedback operational amplifier (CFOA) AD 844 AN [46-49]. The CFOA is a three terminal active device. The circuit symbol of the CFOA is shown in Fig. 2.13. The OTRA implementation using the IC AD 844 AN is shown in Fig. 2.14. Two AD 844 AN ICs and a resistor are used to construct the OTRA. The non-inverting terminals of the AD 844 ANs have been grounded, to

simulate the virtual ground, for the terminals of the OTRA. The following equations can be obtained from the Fig. 2.14.

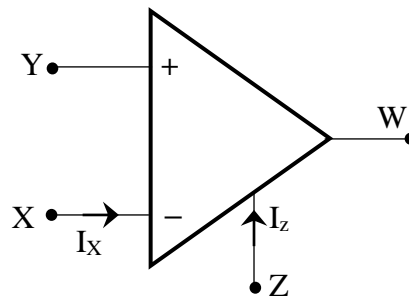


Fig. 2.13 CFOA (AD 844) circuit symbol

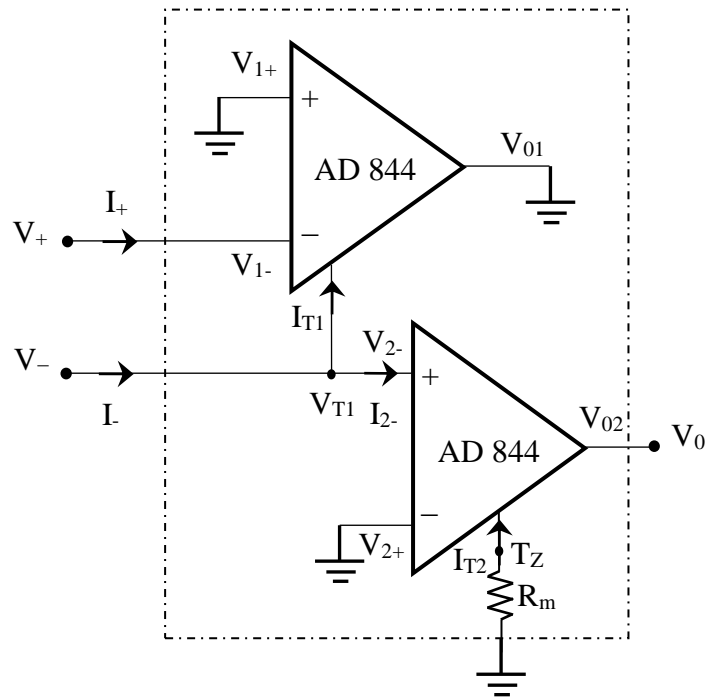


Fig. 2.14 Implementation of OTRA using AD 844 ICs

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_W \end{bmatrix} \quad (2.4)$$

$$V_+ = V_{1-} = V_{1+} = 0 \quad (2.5)$$

$$V_- = V_{2-} = V_{2+} = 0 \quad (2.6)$$

$$V_{01} = V_{T1} = V_{2-} = V_{2+} = 0 \quad (2.7)$$

$$I_{T1} = I_{1-} = I_+ \quad (2.8)$$

$$I_{T2} = I_{2-} = I_- - I_{T1} = I_- - I_+ \quad (2.9)$$

$$V_0 = V_{T2} = -R_m \times I_{T2} = R_m (I_+ - I_-) \quad (2.10)$$

Therefore, the behavior of the OTRA is obtained with the schematic shown in Fig. 2.14. In this figure, if the T_Z node of the second AD 844 AN is open circuited then the transresistance gain R_m is infinite ($R_m = \infty$). With the schematic shown in Fig. 2.14, the proposed circuits in chapter 4 can be implemented on laboratory bread board to check the theoretical analysis.

2.4 SUMMARY

In this chapter, the OTRA characteristics are given in detail. The ideal OTRA based terminal relations are presented along with the OTRA non-ideal model. The CMOS OTRA realizations proposed in [32, 33] are redesigned using cadence gpdk 180 nm technology. Spectre simulation models are used to simulate the CMOS OTRAs. Two CMOS OTRA realizations are presented in this chapter. The simulation results of input terminal resistance, output terminal resistance and the frequency response of the OTRA are included in this chapter. The OTRA prototype model is also presented in this chapter using two AD 844 AN ICs. This prototype model is helpful in the performance evaluation of OTRA based circuits on a laboratory breadboard.