Chapter 1

Introduction

1.1 Motivation and Background

The process of designing, fabricating and testing an analog chip requires certain expertise and is often long and expensive. In contrast design of digital integrated circuits is fully automated. Historically the simpler nature of digital circuits, as compared to analog circuits, has led to the development of libraries and synthesis tools for fast synthesis of digital circuits. To reduce the cost and time-to-market field programmable gate arrays (FPGA) and complex programmable logic device (CPLD) are widely used for prototyping of large-scale digital integrated circuits.

The primary benefit of implementing signal processing systems in analog is the potential for large savings in power consumption [1]. One of the main factors in power consumption is ADC (Analog to Digital Converter). Digital signal processing systems need ADC because nature of signals is analog. The power consumption of ADC does not follow technology-scaling laws. While ADC resolution has been increasing roughly 1.5 bits every five years, the power performance has remained the same [1].

Prototyping techniques for analog circuits analogous to FPGAs have been recently introduced, of which some references are given at the end of this proposal [1-14]. This technique is known as FPAA (Field Programmable Analog Array). Different FPAA design techniques have been proposed including switched-capacitor (SC), Op-Amp-based and transconductor-based designs.

FPAA are not optimal for all solutions in contrast to FPGAs. This again results from complex nature of analog circuits, which needs more factors to be addressed such as bandwidth, linearity, signal-to-noise ratio, frequency response, etc. FPAAs are made using configurable analog blocks (CAB) and interconnection networks, which are used to provide required interconnection among Cabs. Unlike FPGAs, circuit functionality is much more sensitive to parasitics introduced by the programming devices in FPAA. So the design of FPAAs architecture and CABs are mutually dependent. To design an efficient FPAA, a designer needs to comprise between flexibility and the number of programmable switches in the signal path while designing FPAA architectures and the CAB topologies.

Analog circuitry is advantageous for wireless and remote applications where compactness and low power consumption are important. Overall, analog ICs are being applied in signal processing, wireless communications, monitoring and control. Field-Programmable Analog Arrays (FPAA), which offer rapid prototyping on a single IC, are proving to be a very useful tool for the design of working analog and mixed-signal ICs. Several commercial FPAA designs have been published, operating in both the continuous-time and discrete-time domains [15]. Many university-based FPAAs have also been proposed [13,16-20]. Growing popularity of analog and mixed signal ICs has provided the impetus to explore innovative designs implemented with CMOS VLSI technology. Reduction of design turn around time is another vital issue. While designers in digital domain can fall back on programmable devices like PLD, CPLD, FPGA etc. to try out innovative designs with lesser physical design efforts and time, similar facilities are not available for analog design community.

The design of the Configurable Analog Block (CAB), the basic cell used in FPAAs, is usually influenced by a number of factors, including the functionality and performance features of circuits to be prototyped, the area-efficiency of routing resources dictated by the CAB design itself and the supporting semiconductor process technology. The computational elements like Transistors, Op-amps, OTA are used for CAB design. Summery of FPAA granularity is given in Table 1.1. [15].

Table 1.1. Summary of FPAA granularity

Granularity	Computational Element	Advantage	Disadvantage	Primary Application
Fine	Transistors	Small simple CAB design Generic building block	Large no of switches Large parasitics	Evolvable Hardware
Medium	Op-Amp OTA Current conveyor	Semi generic building block Moderate CAB design Large verity of CAB/interconnect designs	Limited size Severe functionality / performance trade-off	Filters , amplifiers, Signal conditioning, Low-level signal processing
Coarse	Fourier processor "Expert cell"	Higher performance Easier user interface	Limited flexibility Limited functionality	Filters Signal conditioning

The operational transconductance amplifier (OTA) is a fundamental building block in analog (mixed-signal) design and its performance characteristics are the foundation of system level characteristics. In comparison to the operational amplifier, the transconductance amplifier offers excellent frequency response, is readily programmable by a DC bias current and requires a small amount of silicon chip design area. Good performance is attainable with both bipolar and MOS implementations. Although it can be used in feedback applications, the OTA finds many applications as an open-loop amplifier element. In those applications, linearity and accuracy of the transconductance gain are the major interest [9-11,21-22,23-25].

Operational Transconductance Amplifier (OTA) is an active current mode building block similar to voltage mode counterpart of operational amplifier. Many current mode building blocks such as OTA, switched current (SI) cell, switched capacitor (SC) cell, current conveyor, differential difference amplifier (DDA) etc. can be used for realisation of linear and non-linear analog systems. Because of its structural simplicity and convenient controllability, OTA can be found to a better candidate. OTA is an active voltage to current (V-I) converter. Output current of the device varies with the input voltage. Further, OTA is an excellent current mode device to realise high frequency resistor less analog designs. In this background scenario, we have embarked on design and optimization of an OTA based FPAA to realise wide varieties of high frequency analog filters and communication circuits. Such a FPAA structure can be economically fabricated with CMOS VLSI technology.

1.2 Prototyping of Analog Integrated Circuits

1.2.1 Introduction

In its most general form, an FPAA is a monolithic collection of analog building blocks, a user controllable routing network used for passing signals between the building blocks and a collection of memory elements used to define both the function and structure [17]. Fig. 1.1 shows a conceptual block diagram of an FPAA, including a set of Configurable Analog Blocks (CABs) and a routing network [17]. Configuration memory is provided for the blocks and interconnects.

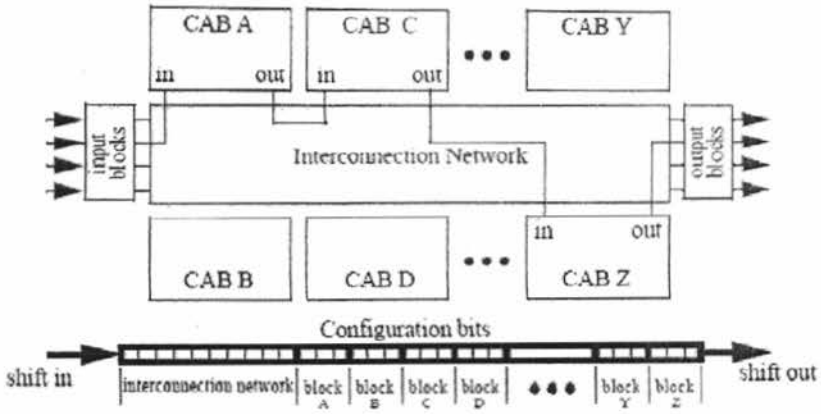

Figure 1.1 FPAA Conceptual block diagram

The flow chart of analog synthesize using FPAA is illustrated in Fig. 1.2 [17]. This flowchart details the computer-aided design (CAD) methodology, which is used to synthesize an analog circuit onto an FPAA [17]. In a schematic editor, the user enters a schematic netlist of the desired circuit; the schematic can be at one of many logical levels, from behavioral down to transistor-level depending on the synthesizing capabilities of the CAD tool. The CAD tool then decomposes the schematic into basic units and synthesizes it in terms of the resources available on the FPAA. Then the circuit is placed and routed, and the original schematic is back annotated. Verification is performed to see if the mapping of the circuit onto the FPAA meets all design specifications. If not, the whole procedure can be repeated within a matter of minutes. When design specifications are met, a configuration bit string is generated by the CAD tool and downloaded onto the FPAA IC, instantiating the designer's circuit. The downloading is usually performed using the parallel port of a personal computer; often the configuration bits can also be stored in an on-board EEPROM. If the designer decides to change the circuit, then redesigning and reprogramming the IC can be done in a matter of hours instead of the months it would take to redesign and fabricate a new ASIC.

1.2.2 Rapid Prototyping of Analog Systems

The process of designing, fabricating, and testing an analog chip requires certain expertise and is often long and expensive. As shown in Fig. 1.3 the process is like designing digital ASICs (application specific integrated circuits), except that there are fewer tools and libraries available to the designer. The traditional analog design cycle often requires several iterations of the fabrication process, which with the simulation, VLSI layout, and testing phases can easily consume a year or more for typical IC designs. However, the use of a reconfigurable analog chip, dubbed a FPAA, would dramatically reduce the design cycle by removing the fabrication stage from the iterative process.

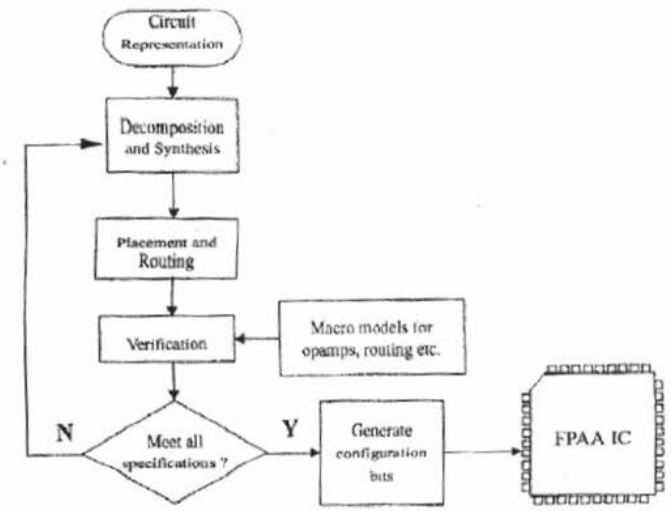

Fig.1.2 Analog synthesize process using FPAA

Thus, many designs may be tested and modified within a single day. Like FPGAs, FPAAs are not optimal for all solutions. They are, however, very useful for many situations, and a solution can be found for many problems not requiring full functionality. Relative to custom designed analog circuits, a design implemented on an FPAA results in

higher parasitics as well as increased die area for a given design; therefore, the design always possesses some inefficiencies (i.e., lower bandwidth and higher consumed power). On the other hand, since analog circuit design is often time consuming, these adverse characteristics are well balanced by markedly decreased time to market [26].

FPAAs have been of interest for some time, but historically, these devices have had very few programmable elements and limited interconnect capabilities, making them limited in their usefulness and versatility. The next generation FPAA needs to correct these problems in order to extend the usefulness and acceptance of FPAAs. The FPAAs can be used to implement high order filtering, in addition to having a large number of fine and medium grain, programmable analog blocks (e.g., operational transconductance amplifiers (OTAs), transistor elements, capacitors, etc.).

1.2.3 Low Power Signal Processing

The future of FPAAs lies in their ability to speed the implementation of advanced low-power signal processing systems. Growing demand for complex information processing on portable devices has motivated a lot of contemporary research in the design of power efficient signal processing systems [15]. For analog systems to be desirable to the largely digital signal processing community, they need to provide a significant advantage in terms of size and power and yet still remain relatively easy to use and integrate into a larger digital system.

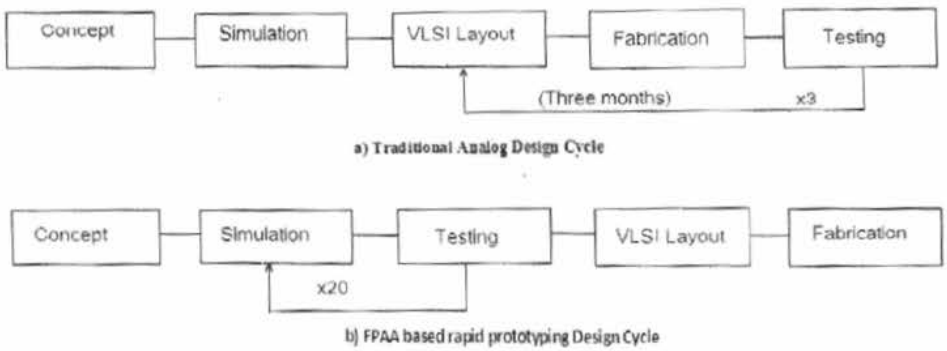

Figure1.3 Design cycle

Fig. 1.3 illustrates the advantages of designing analog ICs using an FPAA based rapid prototyping technology as opposed to the traditional design cycle of VLSI layout and fabrication. The traditional analog design cycle often requires 3 or more iterations of the fabrication process, which extends the development process to over a year. With an FPAA based system, designs can be synthesized, tested, and modified 20 or more times within a matter of days instead of years [20]. Wide variety of analog functions required in electronic systems and the complexity of the signals (frequency, time, signal levels, parasitics), analog system design is very specialized and supported by a diverse set of CAD tools. The drive towards shorter design cycles for analog integrated circuits has demanded the development of high performance analog circuits that are reconfigurable and suitable for CAD methodologies. This has been the motivation for research in the area of FPAAs, which seek to provide accurate, low-cost, rapid prototyping techniques for analog and mixed analog digital circuits–a long awaited development for circuit designers. Commercial products introduced recently, along with progress made at University research laboratories, indicate renewed interest and further accomplishment in achieving this goal [5-6, 12-14,27-28].

1.3 Brief Summary of the Thesis

In this thesis design and optimization of an OTA-based FPAA with a new architecture in 0.35um CMOS process is presented. Optimization methods are explored by which area, power dissipation, tuning range and versatility of programming can be optimized while keeping the main specifications of OTAs intact. CABs and routing network are optimally designed, sized and implemented at the schematic level in 0.35um mixed-mode CMOS process and are verified using CADENCE simulations tools. The design space is explored to investigate the validity of the design from optimization aspect. Therefore the architecture of the final FPAA is adaptable for those practical applications, which are demanding low power programmable solutions. To save the area a new architecture for the FPAA architecture is also presented. The presented FPAA was designed and optimized for implementing a set of commonly used analog signal processing functions including adjustable transconductors, programmable continuous time filtering and analog multiplication.

1.4 Structure of the Thesis

This thesis is organized as follows.

In Chapter 1, motivation and background behind selection of this work as well as scenario of rapid prototyping and analog signal processing is discussed.

In Chapter 2, applications of Continuous Time FPAAs, background and related technologies and design are reviewed. A survey of the literature dealing with reported FPAAs and OTA-based FPAAs is given.

In Chapter 3, a method for sizing and optimization of a CMOS OTA, used in analog FPAA is presented. Basic analog design flow is also presented in chapter 3.

In Chapter 4, basic principle of OTA, OTA as a CAB, OTA architecture selection, preliminary design and simulation of Cross-coupled OTA and Cross- couple OTA with source degeneration in 0.35 CMOS process are presented.

In Chapter 5, aside from CAB components, different interconnect structures are discussed for FPAAs. The choice of an interconnection architecture and its implementation will influence the routability of prototyped circuits and their performance.

In Chapter 6, various methods for optimal determination of the component values and transistor dimensions in CMOS OTAs are introduced. In circuit design optimization, a circuit and its performance specifications are given and the goal is to automatically determine the device sizes in order to meet the given performance specifications while minimizing a cost function, such as a weighted sum of the active area or power dissipation.

Scaling of analog modules is not obeying scaling rules of digital circuits. Therefore migration from one technology to another needs comprehensive redesigns in analog circuits. The design and optimization flow is used to scale the OTA-based FPAA from 2um to 0.35um CMOS technology. This design and optimization procedure is presented in detail in chapter 7. Accordingly OTA and its internal modules were optimized to get the best performance specifications for the CABs in 0.35um CMOS technology.

Since area and efficiency are main concerns a new routing architecture is presented in chapter 8, which reduces redundancy of the FPAA architecture, i.e. reducing the number of unused CABs while an analog processing function is implemented using designed FPAA.

Development of integrated OTAs has led to new filter configurations with reduced number of resistive components. This has given rise to OTA-C filters, using only active devices and capacitors, making it more suitable for integration. The realization of the basic filter components like resistors, inductors and gyrators etc. are presented in chapter 9. A realization of 6^{th} and 12^{th} order Butterworth Filter using FPAA, designed in this thesis, is also presented in chapter 9.

In Chapter 10 application of OTA as a multiplier is presented, which plays an important role in analog signal processing systems. Also chapter 10 presents a review of different analog multiplier architectures, which have been proposed over the last fifteen years. The multiplier structures are simulated in Cadence Analog Design Environment using Spectre circuit simulator to obtain their characteristics such as input range, linearity, input noise and power consumption.

A new structure for the analog multiplier is proposed in chapter 10. This multiplier uses cross-coupled OTA and has low power dissipation while at the same time keeping good linearity.

Chapter 11 gives the conclusion and future work upon the research work presented in this thesis.

Analog and Simulation options for Spectre, used for all simulations carried in this thesis, are given in appendix A.