Chapter 11

Conclusion and Future Scope

A GP-based and simulation-based optimization design methodology was developed in this thesis. This methodology was applied for optimal migration of OTA-based FPAA from 2um to 0.35um technology. Since power and costs were the primary concerns the CMOS technology was preferred. Cadence Analog Circuit Optimizer was used for the simulation-base optimization part.

Different OTA architectures were analyzed. Cross-coupled OTA architecture was chosen due to its high linearity, large tuning range and low power consumption. The different architectures for floating voltage source, used in cross-coupled OTA, were investigated.

Those circuits, which were taken from reference papers, were first simulated in 2um CMOS technology, to confirm the results given in the reference papers.

All FPAA modules were redesigned for the required specifications and optimized for low-power consumption in 0.35um technology, using the methodology, given in this thesis. All core FPAA modules were simulated carefully using proper simulation options in Cadence ADE.

The CMOS OTA was sized initially using MATLAB Optimization toolbox applying convex optimization approach. Then the design was further optimized by Cadence Analog Circuit Optimizer to include second order effects. Since the initial

design uses GP method the globally optimum solution is obtained. The results were verified by detailed analog simulation using Cadence Analog Design Environment (ADE) and their results were compared. Power was minimized, Tuning range was improved and Total Harmonic distortion was reduced. Thus the designed OTA can be used for low voltage Portable Applications. It was found that by choosing the Cross-Coupled OTA architecture linearity is improved. All the supporting blocks like CMFB, Floating voltage source, Programmable current source were designed and simulated in 0.35um technology. The simulation results show that the designed OTA exhibits potential to be used for SOC, FPAA and Continuous-time filtering applications.

The different types of FPAA, especially OTA-based FPAA were studied. A new CAB interconnection scheme was developed being more efficient than already reported scheme. In the proposed CAB interconnection scheme in this thesis, we have reduced redundancy of the architecture i.e. reducing the number of unused CABs during implementation of an analog Signal Processing Function. By using this new technique less area is required to implement the CABs.

4-Transistor Transconductor was found to be a better candidate as routing switch. Full implementation of OTA-based FPAA has been done. A 6_{th} order and 12^{th} order Band-pass filter has been realized by using OTA-based FPAA, designed in this thesis.

In this thesis, three multiplier architectures were explored theoretically and simulated in Cadence Virtuoso Analog Environment. A cross-coupled OTA-based multiplier was proposed in this thesis. The proposed OTA multiplier is most attractive for low power and highly linear MOS multiplier structure.

Several important performance metrics i.e. input range, linearity, power consumption, noise etc. have been analyzed, for the three multiplier structures. The experimental results have shown that proposed OTA multiplier consumes comparable power with the existing structures, while maintaining good linearity. The total supply current can be further reduced by some design considerations.

Briefly in this thesis a methodology for design and optimization of analog circuits was proposed and used for implementation of an OTA-based FPAA. Further a new interconnection scheme was proposed and implemented for CAB interconnections. The implemented FPAA was used to implement two continuous-time Butterworth filters. We also proposed and implemented a new multiplier using cross-coupled OTA architecture.

FPAA design and implementation has recently taken gain and still there is a lot of scope for further work in this domain. Efficient FPAA architecture with respect to the area, programmability and tuning range of analog modules, diversity of available functions and availability of wide range of specifications are suggested for future research. As technology scales down design of OTA CAB modules, which will be able to work at less levels of power supply, will be of interest and is suggested as another subject for future research. Also modification and improvement of the multiplier, proposed in this thesis, is another research which can be followed as a continuation of this work.