Chapter 3

Analog Design Flow

3.1. Introduction

The time required to do circuit design and the quality of the results are strongly dependant on the skill of the designer performing the task. Many design /simulate /update schematic iterations are needed to obtain a design that meets the necessary performance specifications at all required operating and process corners. Redesign of analog building blocks is a time consuming process while scaling an analog module in CMOS technology. So automatic sizing while taking care of second order effects is of great importance. In this thesis a method for automatic sizing and optimization of a CMOS Operational Transconductance Amplifier (OTA), used in analog FPAA (Field Programmable Analog Array) is presented. The optimization determines the optimal component values and transistor dimensions for CMOS OTA in order to minimize the dissipated power. The presented methodology uses geometric programming (GP) and simulation-based optimization in a time-efficient manner. The CMOS OTA is sized using MATLAB Optimization toolbox applying convex optimization and Cadence Analog Circuit Optimizer to include second order effects. Since the design uses GP method the globally optimum solution is obtained. The results are verified by detailed analog simulation using Cadence Analog Design Environment (ADE). The widely tunable and highly programmable OTA is designed in 0.35um CMOS technology, which can be used for low power applications.

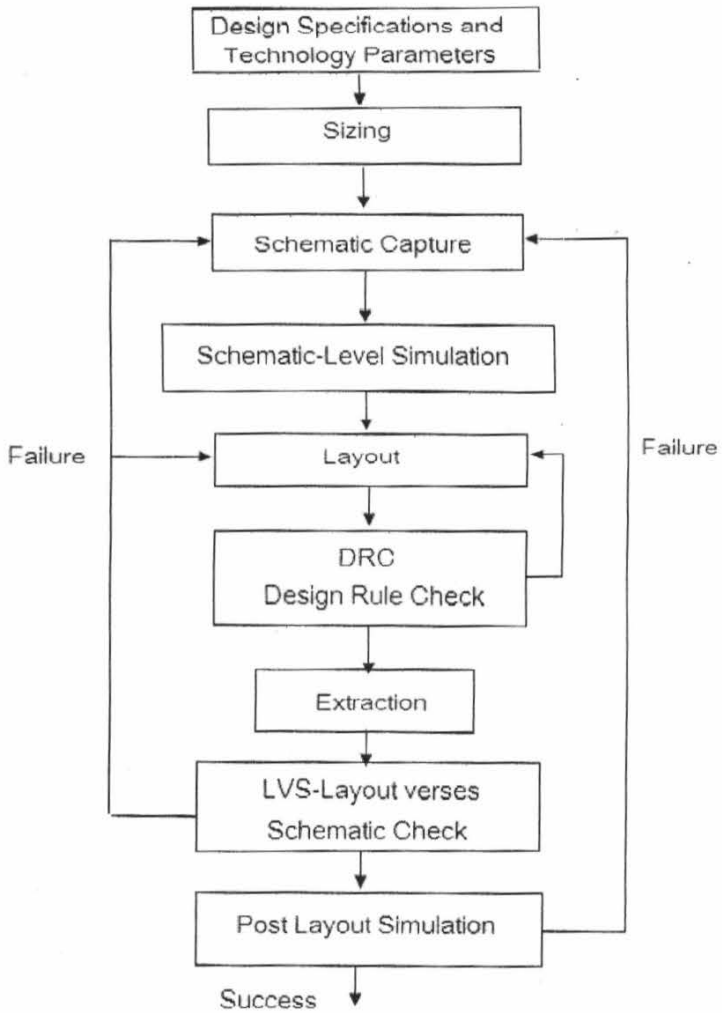

Fig. 3.1 Main Analog Design Flow

3.2. Analog Design Flow

Figure 3.1 shows main Analog Design Flow [34, 35].

Fabrication technology -

Fast analog integration in deep sub-micron CMOS technologies has become a very important issue. Since the technology roadmap predicts a fast scaling-down of the

transistor's minimum channel lengths to 0.03μm in Year 2014, the need for fast redesigns for different technologies of existing analog building blocks becomes crucial in the IC industry. Circuit designers must have a working knowledge of chip fabrication to create effective designs and in order to optimize the circuits with respect to various manufacturing parameters. Also, the circuit designer must have a clear understanding of the roles of various masks used in the fabrication process, and how the masks are used to define various features of the devices on-chip. As fabrication technology scales down, it becomes more challengeable to analog designer to design.

Design Specifications -

The top-down design flow for a transistor-level circuit layout always starts with a set of design specifications. The design specifications allow considerable freedom to the circuit designer. It gives the choice to select a specific circuit topology, individual placement of the devices, the locations of input and output pins, and the overall aspect ratio (width-to-height ratio) of the final design. In a large-scale design, the initial design specifications may also evolve during the design process to accommodate other specs or limitations [34].

Sizing –

Analog components are an important part of integrated systems. Either in terms of elements and area in mixed-signal systems, or as vital parts in digital systems, for instance power-on reset, pad driving, or clock generation. Despite their importance, design automation for analog circuits still lags behind that of digital circuits. As a

consequence, analog components often are a bottleneck in the design flow. Analog synthesis is complicated because it does not only consist of topology and layout synthesis but also of component sizing. Additionally, it has to incorporate physical effects like process variations, variations of operating conditions, matching constraints, or noise. It becomes even more complicated, as more and more mixed-signal systems and systems-on-chips are designed with customized analog components. For each building block a set of sizing rules will be given. These rules result from constraints guaranteeing the dedicated function and its robustness e.g. towards mismatch or channel length modulation. These constraints refer to transistor geometry parameters (width, length, area) and electrical transistor quantities (e.g. transistor drain/source voltage) [36].

In analog circuit design automatically sizing is not possible. Sizing may start completely from scratch, without any initial device sizing information on the schematic while respecting all design constraints. Sizing begins with annotating the schematic database with constraints, which includes defining critical device relationships (e.g. matching), identifying independent variables and providing the target design specifications (e.g., Total Harmonic Distortion [THD]). Numerous simulations, including process and operating corner simulations, can be setup to measure the target specifications of the circuit. After sizing a circuit, designers can view trade-off curves (e.g., between two goals such as power and settling time).

Schematic Capture –

The traditional method for capturing transistor-level or gate-level design is via the schematic editor. Schematic editors provide simple, intuitive means to draw, to place and

to connect individual components that make up the design. The resulting schematic drawing must accurately describe the main electrical properties of all components and their interconnections. Also included in the schematic is the power supply and ground connections, as well as all "pins" for the input and output signals of circuit. This information is crucial for generating the corresponding netlist, which is used in later stages of the design. The generation of a complete circuit schematic is therefore the first important step of the transistor-level design flow. Usually, some properties of the components (e.g. transistor dimensions) and/or the interconnections between the devices are subsequently modified as a result of iterative optimization steps. These later modifications and improvements on the circuit structure must also be accurately reflected in the most current version of the corresponding schematic [34].

Schematic-level Simulation -

After the transistor-level description of a circuit is completed, the electrical performance and the functionality of the circuit must be verified using a Simulation tool. The detailed transistor-level simulation of the design will be the first in-depth validation of its operation. Hence, it is extremely important to complete this step before proceeding with the subsequent design optimization steps. Based on simulation results, the designer usually modifies some of the device properties (such as transistor width-to-length ratio) in order to optimize the performance. The initial simulation phase also serves to detect some of the design errors that may have been created during the schematic entry step [34].

Layout -

The creation of the mask layout is one of the most important steps in the full-custom design flow, where the designer describes the detailed geometries and the relative positioning of each mask layer to be used in actual fabrication, using a Layout Editor. Physical layout design is very tightly linked to overall circuit performance (area, speed and power dissipation) since the physical structure determines the transconductances of the transistors, the parasitic capacitances and resistances, and obviously, the silicon area, which is used to realize a certain function. It is extremely important that the layout design must not violate any of the Layout Design Rules, in order to ensure a high probability of defect-free fabrication of all features described in the mask layout.

DRC – Design Rule Check -

The created mask layout must conform to a complex set of design rules, in order to ensure a lower probability of fabrication defects. A tool built into the Layout Editor, called "Design Rule Checker", is used to detect any design rule violations during and after the mask layout design. The detected errors are displayed on the layout editor window as error markers, and the corresponding rule is also displayed in a separate window. The designer must perform DRC (in a large design, DRC is usually performed frequently - before the entire design is completed) and make sure that all layout errors are eventually removed from the mask layout, before the final design is saved [34].

Extraction –

Circuit extraction is performed after the mask layout design is completed, in order to create a detailed net-list (or circuit description) for the simulation tool. The circuit extractor is capable of identifying the individual transistors and their interconnections (on various layers), as well as the parasitic resistances and capacitances that are inevitably present between these layers. Thus, the "extracted net-list" can provide a very accurate estimation of the actual device dimensions and device parasitics that ultimately determine the circuit performance. The extracted net-list file and parameters are subsequently used in Layout-versus-Schematic comparison and in detailed transistor-level simulations (post-layout simulation) [34].

LVS – Layout versus Schematic Check -

After the mask layout design of the circuit is completed, the design should be checked against the schematic circuit description created earlier. The design called "Layout-versus-Schematic (LVS) Check" will compare the original network with the one extracted from the mask layout (excluding parasitic elements), and prove that the two networks are indeed equivalent. The LVS step provides an additional level of confidence for the integrity of the design, and ensures that the mask layout is a correct realization of the intended circuit topology. However a successful LVS will not guarantee that the extracted circuit will actually satisfy the performance requirements. Any error that may show up during LVS (such as unintended connections between transistors, or missing connections / devices, etc.) should be corrected in the mask layout before proceeding to post-layout simulation [34].

Post – Layout Simulation -

The electrical performance of a full-custom design can be best analyzed by performing a post-layout simulation on the extracted circuit net-list. At this point, the designer should have a complete mask layout of the intended circuit/system, and should have passed the DRC and LVS steps with no violations. If the results of post-layout simulation are not satisfactory, the designer should modify some of the transistor dimensions and/or the circuit topology, in order to achieve the desired circuit performance under "realistic" conditions, i.e., taking into account all of the circuit parasitics. This may require multiple iterations on the design, until the post-layout simulation results satisfy the original design requirements. A satisfactory result in post-layout simulation is still no guarantee for a completely successful product; the actual performance of the chip can only be verified by testing the fabricated prototype. Even though the parasitic extraction step is used to identify the realistic circuit conditions to a large degree from the actual mask layout, most of the extraction routines and the simulation models used in modern design tools have inevitable modeling and numerical limitations [34].

3.3 Target Technology

Complete design of whole FPAA has been done in 0.35um Mixed-Mode CMOS process from TSMC. The reference work has used 2um CMOS process but one of our goals in this research has been to first scale that design (not as per digital scaling rules) and second optimizes it for low power consumption and high linearity.