CHAPTER IV

ANALYSIS OF PROPOSED XOR/XNOR CIRCUITS

The XOR/XNOR is the basic building block of various circuits like adders, comparators, multipliers, parity generator/checkers, code converters and error controlling coders – to mention a few. Hence it is used widely in many VLSI systems as a part of the critical path that determines the altogether performance of the system. The performance of the complex logic is decided by the performance of individual XOR/XNOR blocks that are part and parcel of them. Careful design and analysis, therefore, is required for XOR/XNOR circuits to produce a full rail-to-rail swing, dissipate less power, and have less delay in the critical path and component economy leading to smaller. In this chapter, an anlayses like rail to rail swing, sizing of transistors, self checking, code disjoint, propagation delay, power dissipation and Monte Carlo simulations of proposed circuits are discussed.

4.1 Two input differential XOR/XNOR circuits: Fig.3.1 and Fig.3.2

The four versions of proposed two input differential XOR/XNOR circuit-1 and circuit-2 exhibit full rail to rail swing.

4.1.1 Rail to rail analysis of Fig.3.1(a)

The proposed two input differential XOR/XNOR circuit version-1 which is shown as Fig.3.1(a) circuit exhibit full rail to rail swing. The analysis of Fig 3.1(a) is as follows.

(i) For AB=00 case

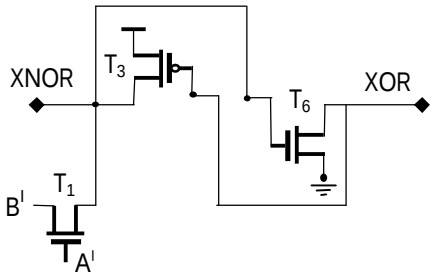

Fig.4.1 Equivalent circuit of Fig.3.1(a) for inputs A=logic 0, B= logic 0

The input values are A=logic 0, B= logic 0 and Abar =logic 1. Since the gate terminal of transistor T_1 is connected to logic 1 i.e V_{dd}, T_1 is Switched ON and B^1 value, i.e logic high is passing so transistors T_6 and T_3 are also switched ON. The transistors T_2, T_4, T_5 are switched OFF. The equivalent circuit is shown in Fig.4.1.

So at $V_{XNOR}= V_{dd} – V_{tn}$

$V_{gs6}=V_{XNOR}= V_{dd} – V_{tn}$

$V_{ds6}= 0$

So transistor T_6 is in triode region.

Then $V_{gs3} = -V_{dd}$

$V_{ds3} = V_{XNOR} - V_{dd} = -V_{tn}$

So transistor T_3 is also in triode region. It's equivalent resistance is

$$R_P = \frac{V_{ds3}}{I_{ds3}} = \frac{V_{ds3}}{\left(\mu_P \frac{\varepsilon_{ox}}{t_{ox}}\right)\left(\frac{W}{L}\right)\left[\left(V_{gs3} - V_{tp}\right)V_{ds3} - \frac{V^2_{ds3}}{2}\right]} \quad (4.1)$$

After substituting $R_P = \frac{L.t_{ox}}{\mu_P \varepsilon_{ox} W\left(-V_{dd} - V_{tp} + \frac{V_{tn}}{2}\right)}$ (4.2)

This R_P is small. So $V_{XNOR} = V_{dd}$ – drop across R_P

Drop across R_P is negligible, so $V_{XNOR} = V_{dd}$.

Therefore V_{XNOR} is gaining its full rail swing.

For W_1/L_1 = 360nm/90nm, W_3/L_3 = 450nm/90nm, t_{ox} = 2.05nm, C_{ox} = 16.84e-3 F/m^2, V_{tn} = 0.3 V, V_{tp} = -0.365 V, μ_p = 117 μA/V^2 , V_{dd} = 0.9 V, then R_p = 186.591 μΩ.

(ii) For AB=10 case

For inputs A=logic 1, B= logic 0, the equivalent circuit is shown in Fig.4.2.

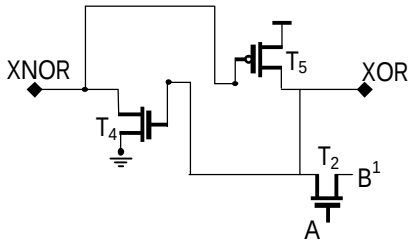

Fig.4.2 Equivalent circuit of Fig.3.1 (a) for inputs A=logic 1, B= logic 0

Similar to the above analysis, $V_{XOR} = V_{dd}$ is achieving through the combination of transistors T_4 and T_5.

(iii) For AB=01 and AB=11 cases

For the cases of A=logic 0, B= logic 1 and A=logic 1, B=logic 1 , the values of V_{XOR} and V_{XNOR} are strong logics. The equivalent circuits are shown in Fig.4.3 and Fig.4.4.

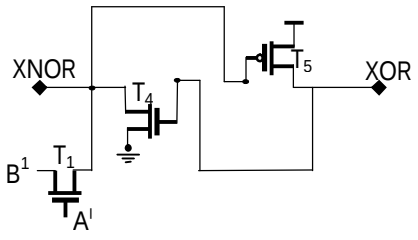

Fig.4.3 Equivalent circuit of Fig.3.1(a) for inputs A=logic 0, B= logic 1

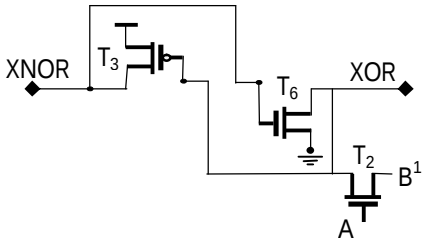

Fig.4.4 Equivalent circuit of Fig.3.1(a) for inputs A= logic 1, B=logic 1

4.1.2 Rail to rail analysis of Fig.3.1(b)

The proposed circuit of two input differential XOR/XNOR circuit version-2 (Fig.3.1(b)) exhibit full rail to rail swing. The analysis of Fig 3.1(b) is as follows.

(i) For AB=10 case

For inputs A=logic 1, B= logic 0, the equivalent circuit is shown in Fig.4.5.

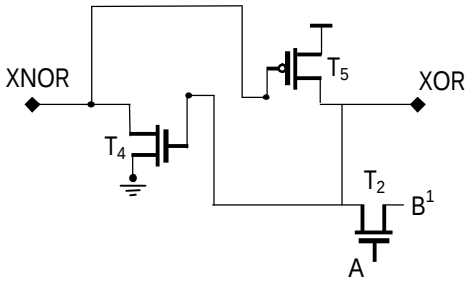

Fig.4.5 Equivalent circuit of Fig.3.1 (b) for inputs A=logic 1, B= logic 0

So at $V_{XOR}= V_{dd} - V_{tn}$

$V_{gs4}=V_{XOR}= V_{dd} - V_{tn}$

$V_{ds4}= 0$

So transistor T_4 is in triode region.

Then $V_{gs5} = -V_{dd}$

$V_{ds5} = V_{XOR} - V_{dd} = - V_{tn}$

So the transistor T_5 is also in triode region. Its equivalent resistance is

$$R_P = \frac{V_{ds5}}{I_{ds5}} = \frac{V_{ds5}}{\left(u_p \frac{\varepsilon_{ox}}{t_{ox}}\right)\left(\frac{W}{L}\right)\left[\left(V_{gs5} - V_{tp}\right)V_{ds5} - \frac{V^2_{ds5}}{2}\right]} \quad (4.3)$$

After substituting $R_P = \dfrac{L.t_{ox}}{\mu_P \varepsilon_{ox} W\left(-V_{dd} - V_{tp} + \dfrac{V_{tn}}{2}\right)}$ (4.4)

This R_P is small.

So $V_{XOR}= V_{dd}$ – drop across R_P

Drop across R_P is negligible, so $V_{XOR}= V_{dd}$.

Therefore V_{XOR} is gaining its full rail swing.

For W_2/L_2 = 360nm/90nm, W_5/L_5 = 450nm/90nm, t_{ox} = 2.05nm, C_{ox} = 16.84e-3 F/m^2, V_{tn} = 0.3 V, V_{tp} = -0.365 V, μ_p = 117 μA/V^2 , V_{dd} = 0.9 V, then R_p = 186.591 μΩ.

(ii) For AB=01 case

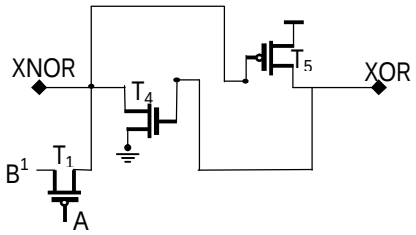

Fig.4.6 Equivalent circuit of Fig.3.1(b) for inputs A=logic 0, B= logic 1

For inputs A= logic 0, B= logic 1, the equivalent circuit is shown in Fig.4.6. Similar to the above analysis, V_{XnOR} = 0 is achieving through the combination of transistors T_4 and T_5.

(iii) For AB=00 and AB=11 cases

For the cases of A=logic 0, B= logic 0 and A=logic 1, B=logic 1, the values of V_{XOR} and V_{XNOR} are strong logics. The equivalent circuits are shown in Fig.4.7 and Fig.4.8.

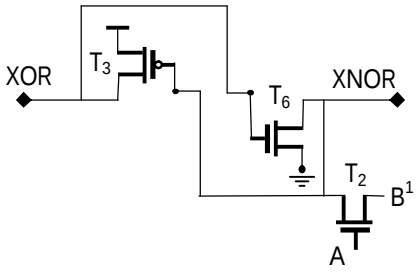

Fig.4.7 Equivalent circuit of Fig.3.1(b) for inputs A=logic 1, B=logic 1

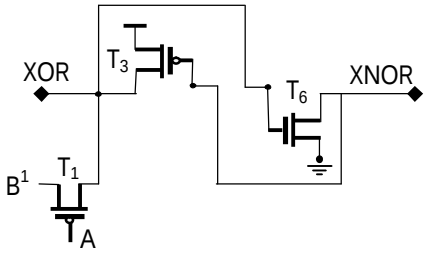

Fig.4.8 Equivalent circuit of Fig.3.1(b) for inputs A=logic 0, B= logic 0

4.1.3 Rail to rail analysis of Fig.3.1(c)

The proposed circuit of two input XOR/XNOR circuit version-3 which is shown in Fig.3.1(c) exhibit full rail to rail swing. The analysis for Fig 3.1(c) is as follows.

(i) For AB=01 case

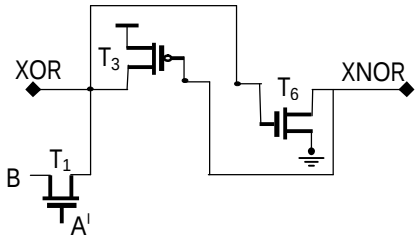

Fig.4.9 Equivalent circuit of Fig.3.1(c) for inputs A=logic 0, B= logic 1

The equivalent circuit of Fig.3.1(c) for inputs A=logic 0, B= logic 1 and Abar =logic 1 is shown in Fig.4.9. Since the gate terminal of transistor T_1 is connected to logic 1 i.e V_{dd} , T_1 is Switched ON and B value, i.e logic high is passing so transistors T_6 and T_3 are also switched ON. The transistors T_2, T_4, T_5 are switched OFF.

So at $V_{XOR} = V_{dd} - V_{tn}$

$V_{gs6} = V_{XOR} = V_{dd} - V_{tn}$

$V_{ds6} = 0$

So the transistor T_6 is in triode region.

Then $V_{gs3} = -V_{dd}$

$V_{ds3} = V_{XOR} - V_{dd} = -V_{tn}$

So the transistor T_3 is also in triode region. Its equivalent resistance is

$$R_P = \frac{V_{ds3}}{I_{ds3}} = \frac{V_{ds3}}{\left(u_p \frac{\varepsilon_{ox}}{t_{ox}}\right)\left(\frac{W}{L}\right)\left[\left(V_{gs3} - V_{tp}\right)V_{ds3} - \frac{V^2_{ds3}}{2}\right]} \quad (4.5)$$

After substituting $R_P = \frac{L.t_{ox}}{\mu_P \varepsilon_{ox} W\left(-V_{dd} - V_{tp} + \frac{V_{tn}}{2}\right)}$ (4.6)

This R_P is small.

So V_{XOR}= V_{dd} – drop across R_P

Drop across R_P is negligible, so V_{XOR}= V_{dd}.

Therefore V_{XOR} is gaining its full rail swing.

For W_1/L_1 = 360nm/90nm, W_3/L_3 = 450nm/90nm, t_{ox} = 2.05nm, C_{ox} = 16.84e-3 F/m^2, V_{tn} = 0.3 V, V_{tp} = -0.365 V, μ_p = 117 μA/V^2 , V_{dd} = 0.9 V, then R_p = 186.591 μΩ.

(ii) For AB=11 case

Similarly for inputs A=logic 1, B= logic 1, the equivalent circuit is shown in Fig.4.10.

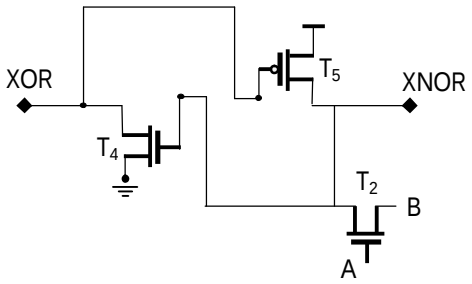

Fig.4.10 Equivalent circuit of Fig.3.1(c) for inputs A=logic 1, B= logic 1

Similar to the above analysis, $V_{XNOR} = V_{dd}$ is achieving through the combination of transistors T_4 and T_5.

(i) For AB=00 and AB=10 cases

For the cases of A=1, B=0 and A=0, B=0 , the values of V_{XOR} and V_{XNOR} are strong logics. Equivalent circuits are shown in Fig.4.11 and Fig.4.12.

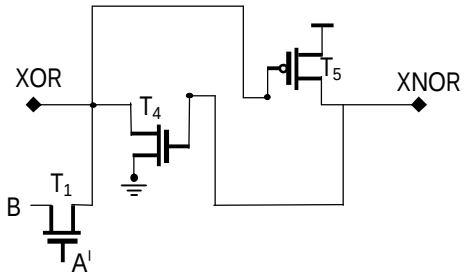

Fig.4.11 Equivalent circuit of Fig.3.1(c) for inputs A=logic 0, B= logic 0

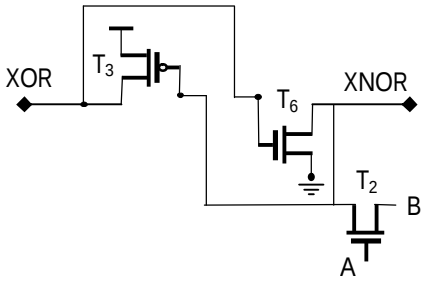

Fig.4.12 Equivalent circuit of Fig.3.1(c) for inputs A=logic 1, B=logic 0

4.1.4 Rail to rail analysis of Fig.3.1(d)

The proposed circuit two input differential XOR/XNOR circuit version-4 which is shown in Fig.3.1(d) exhibits full rail to rail swing. The analysis of Fig 3.1(d) is as follows.

(i) For AB=11 case

For inputs A=logic 1, B= logic 1, the equivalent circuit is shown in Fig.4.13.

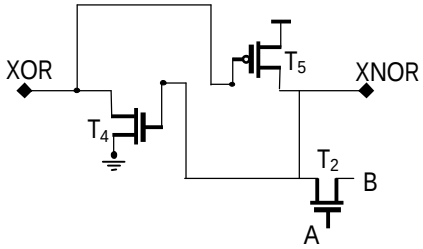

Fig.4.13 Equivalent circuit of Fig.3.1 (d) for inputs A=logic 1, B= logic 1

So at $V_{XNOR}= V_{dd} – V_{tn}$

$V_{gs4}=V_{XNOR}= V_{dd} – V_{tn}$

$V_{ds4}= 0$

So the transistor T_4 is in triode region.

Then $V_{gs5} = –V_{dd}$

$V_{ds5} = V_{XNOR} –V_{dd} = – V_{tn}$

So the transistor T_5 is also in triode region. Its equivalent resistance is

$$R_P = \frac{V_{ds5}}{I_{ds5}} = \frac{V_{ds5}}{\left(u_p \frac{\varepsilon_{ox}}{t_{ox}}\right)\left(\frac{W}{L}\right)\left[\left(V_{gs5} - V_{tp}\right)V_{ds5} - \frac{V^2_{ds5}}{2}\right]} \quad (4.7)$$

After substituting $R_P = \frac{L.t_{ox}}{\mu_P \varepsilon_{ox} W\left(-V_{dd} - V_{tp} + \frac{V_{tn}}{2}\right)}$ (4.8)

This R_P is small.

So $V_{XNOR}= V_{dd}$ – drop across R_P

Drop across R_P is negligible, so $V_{XNOR}= V_{dd}$.

Therefore V_{XNOR} is gaining its full rail swing.

For W_2/L_2 = 360nm/90nm, W_5/L_5 = 450nm/90nm, t_{ox} = 2.05nm, C_{ox} = 16.84e-3 F/m^2, V_{tn} = 0.3 V, V_{tp} = -0.365 V, μ_p = 117 μA/V^2, V_{dd} = 0.9 V, then R_p = 186.591 μΩ.

(ii) For AB=00 case

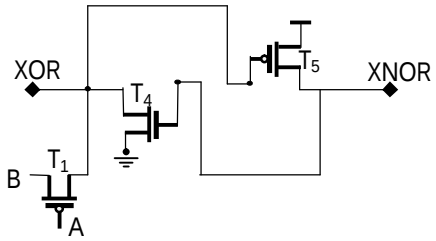

Fig.4.14 Equivalent circuit of Fig.3.1(d) for inputs A=logic 0, B= logic 0

For input pattern of 00, the equivalent circuit is shown in Fig.4.14. Similar to the above analysis, V_{XOR} =0 is achieving through the combination of transistors T_4 and T_5.

(iii) For AB=10 and AB=01 cases

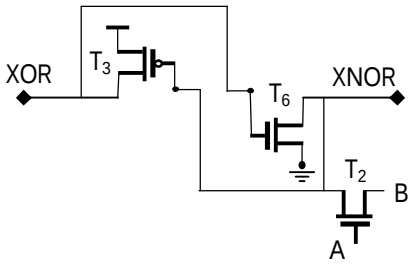

Fig.4.15 Equivalent circuit of Fig.3.1(d) for inputs A=logic 1, B=logic 0

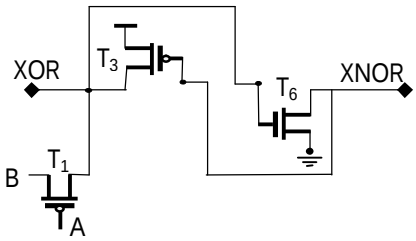

Fig.4.16 Equivalent circuit of Fig.3.1(d) for inputs A=logic 0, B= logic 1

For the cases of A=1, B=0 and A=0, B=1, the values of V_{XOR} and V_{XNOR} are strong logics without loops also. The equivalent circuits are shown in Fig.4.15 and Fig.4.16 respectively.

4.1.5 Rail to rail analysis of Fig.3.2(a) to Fig.3.2(d)

The proposed two input differential XOR/XNOR structure-2 circuits all four versions (Fig.3.2(a) to Fig.3.2(d)) are producing full logic swing for all input combinations because of usage of transmission gate switch as this transmission gate is not having any threshold loss problem.

4.1.6 Sizing of transistors: Fig.3.1(a) and Fig.3.1(c)

The proposed circuits, however, function satisfactorily only when appropriate transistor sizing is maintained in order to take care of the contention in the transition or state-change. To this extent it is a ratioed-logic.

From (J. M. Rabaey et al, 2003), we can arrive at appropriate sizing for T_1 and T_3 by solving (4.9):

$$\mu_n C_{OX}\left(\frac{W}{L}\right)_1\left[(V_{dd}-V_{tn})V_{dsatn}-\frac{V_{dsatn}^2}{2}\right]= -\mu_p C_{OX}\left(\frac{W}{L}\right)_3\left[(-V_{dd}-V_{tp})V_{dsatp}-\frac{V_{dsatp}^2}{2}\right] \quad (4.9)$$

Likewise to arrive at appropriate sizing for T_2 and T_5 we solve (4.10):

$$\mu_n C_{OX}\left(\frac{W}{L}\right)_2\left[(V_{dd}-V_{tn})V_{dsatn}-\frac{V_{dsatn}^2}{2}\right]= -\mu_p C_{OX}\left(\frac{W}{L}\right)_5\left[(-V_{dd}-V_{tp})V_{dsatp}-\frac{V_{dsatp}^2}{2}\right] \quad (4.10)$$

To get the size of T_4 and T_6 , the relation used is $(W/L)_p = 2.5 * (W/L)_n$

since $\mu_n \simeq 2 * \mu_p$

For 90nm, obtained aspect ratios of transistors are $W_1/L_1 = W_2/L_2 = 360nm/90nm$, $W_3/L_3 = W_5/L_5 = 450nm/90nm$, $W_4/L_4 = W_6/L_6 = 180nm/90nm$.

4.1.7 Sizing of transistors: Fig.3.1(b) and Fig. 3.1(d)

The proposed circuits, however, function satisfactorily only when appropriate transistor sizing is maintained in order to take care of the contention in the transition or state-change. To this extent it is a ratioed-logic.

From (J. M. Rabaey et al, 2003), we can arrive at appropriate sizing for T_1 and T_3 by solving (4.11):

$$-\mu_p C_{OX}\left(\frac{W}{L}\right)_1\left[(V_{dd}-V_{tp})V_{dsatp}-\frac{V_{dsatp}^2}{2}\right]= -\mu_p C_{OX}\left(\frac{W}{L}\right)_3\left[(-V_{dd}-V_{tp})V_{dsatp}-\frac{V_{dsatp}^2}{2}\right] \quad (4.11)$$

Likewise to arrive at appropriate sizing for T_2 and T_5 we solve (4.12):

$$\mu_n C_{OX}\left(\frac{W}{L}\right)_2\left[(V_{dd}-V_{tn})V_{dsatn}-\frac{V_{dsatn}^2}{2}\right]= -\mu_p C_{OX}\left(\frac{W}{L}\right)_5\left[(-V_{dd}-V_{tp})V_{dsatp}-\frac{V_{dsatp}^2}{2}\right] \quad (4.12)$$

To get the size of T_4 and T_6 , the relation used is $(W/L)_p = 2.5 * (W/L)_n$

since $\mu_n \simeq 2 * \mu_p$

For 90nm, obtained aspect ratios of transistors are $W_1/L_1 = 250nm/90nm$, $W_2/L_2 = 360nm/90nm$, $W_3/L_3 = W_5/L_5 = 450nm/90nm$, $W_4/L_4 = W_6/L_6 = 180nm/90nm$.

4.1.8 Sizing of transistors: Fig.3.2(a) to Fig. 3.2(d)

To get the size of transistors in the inverter latch, the relation used is $(W/L)_p = 2 * (W/L)_n$ since $\mu_n \simeq 2 * \mu_p$ and for transmission gates TG_1 and TG_2, the minimum sizes of nMOS and pMOS transistors are used.

4.2 Three input differential XOR/XNOR circuits: Fig.3.3 to Fig.3.5

4.2.1 Rail to rail analysis of Fig.3.3

This proposed three input XOR/XNOR circuit-1 which is shown in Fig.3.3 is giving full output for all the input patterns. Actually, two patterns of 000 and 111 are suffering with threshold loss problem, but that problem is avoided by using back back inverter latch connection. That analysis is as follows.

(i) For ABC=111 case

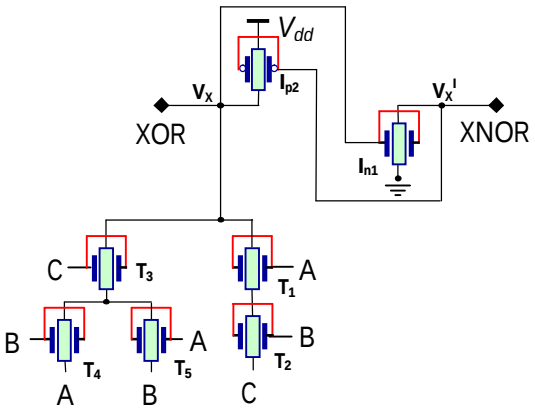

Fig.4.17 Equivalent circuit of Fig.3.3 for inputs A=logic 1, B= logic 1, C= logic 1

Since the input values are A = logic 1, B= logic 1, C= logic 1, the logic 1 is passed to XOR output but due to threshold loss problem only ($V_{dd} - V_{th,n}$) is passed and it is restored by a combination of the transistors I_{n1} and $I_{p2.}$ The resistance of the FinFET transistor I_{p2} can be written as

$$R_P = \frac{V_{dsp2}}{I_{dsp2}} = \frac{L_g . t_{ox}}{\mu_P \, \varepsilon_{ox} \, W_{fin} \left(-V_{dd} - V_{th,p} + \frac{V_{th,n}}{2} \right)} \qquad (4.13)$$

From the above equation, the resistance R_P is small. So

$V_X = V_{dd}$ – drop across R_P

Therefore V_X is gaining its full rail swing.

(ii) For ABC=000 case

Its equivalent circuit is shown in Fig.4.18. Since the input values are A = logic 0, B= logic 0, C= logic 0, A^I = logic 1, B^I = logic1 and C^I = logic 1, the logic 1 is passed to XNOR output but due to threshold loss problem only ($V_{dd} - V_{th,n}$) is passed and it is restored by combination of the transistors I_{n2} and $I_{p1.}$

So the resistance of the FinFET transistor I_{p1} can be written as

$$R_P = \frac{V_{dsp1}}{I_{dsp1}} = \frac{L_g . t_{ox}}{\mu_P \varepsilon_{ox} W_{fin} \left(-V_{dd} - V_{th,p} + \frac{V_{th,n}}{2} \right)} \quad (4.14)$$

From the above equation, the resistance R_P is small. So

$V_X^1 = V_{dd}$ – drop across R_P

Therefore, V_X^1 is gaining its full rail swing.

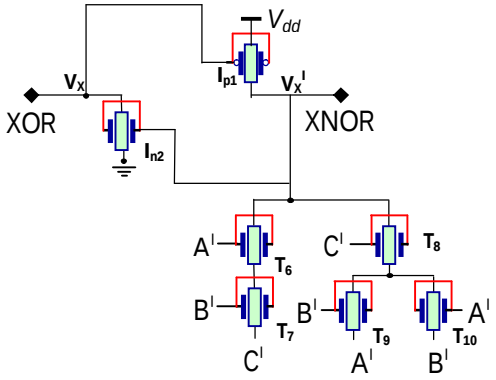

Fig.4.18 Equivalent circuit of Fig.3.3 for inputs A=logic 0, B= logic 0, C= logic 0

4.2.2 Rail to rail analysis of Fig.3.4

The proposed three input XOR/XNOR circuit-2 which is shown in Fig.3.4 is giving full swing for all input patterns. Actually patterns of 001, 111, 101 and 011 are suffering with the threshold loss problem, but that problem is avoided by using back to back inverter latch connection**.** That rail to rail analysis of Fig.3.4 is given below.

(i) For ABC=001 case

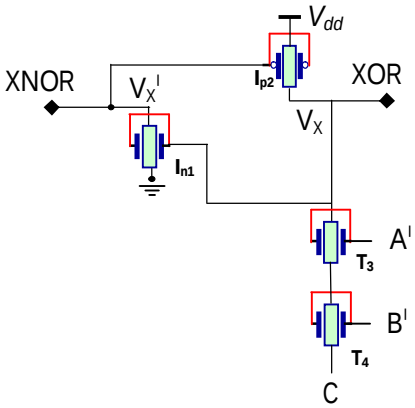

Fig.4.19 Equivalent circuit of Fig.3.4 for inputs A=logic 0, B= logic 0, C= logic 1

The input values are A = logic 0, B= logic 0, A^I = logic 1, B^I = logic1, since the gate terminal of transistors T_3 and T_4 are connected to logic 1 i.e V_{dd} so T_3 and T_4 switched ON and input C value, i.e. logic high is passing through transistors T_3 and T_4 to node V_X. The transistors I_{n1} and I_{p2} are switched ON. So, the resistance of the FinFET transistor I_{p2} can be written as:

$$R_P = \frac{V_{dsp2}}{I_{dsp2}} = \frac{L_g . t_{ox}}{\mu_P \, \varepsilon_{ox} \, W_{fin} \left(-V_{dd} - V_{th,p} + \frac{V_{th,n}}{2} \right)} \qquad (4.15)$$

From the above equation, the resistance R_P is small.

So $V_X = V_{dd} - \text{drop across } R_P$

Therefore, V_X is gaining its full rail swing.

(ii) For ABC=111 case

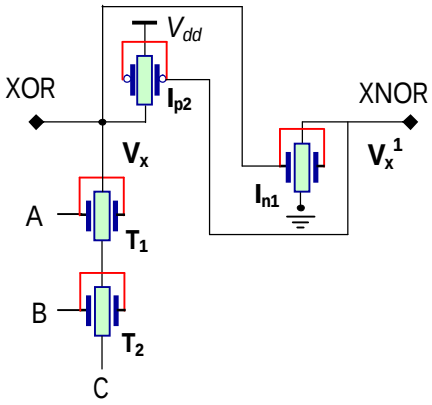

Fig.4.20 Equivalent circuit of Fig.3.4 for inputs A=logic 1, B= logic 1, C= logic 1

Its equivalent circuit is shown in Fig.4.20. Similar to the above analysis, $V_x = V_{dd}$ is achieved through the combination of FinFETs I_{p2} and I_{n1}.

(iii) For ABC=101 case

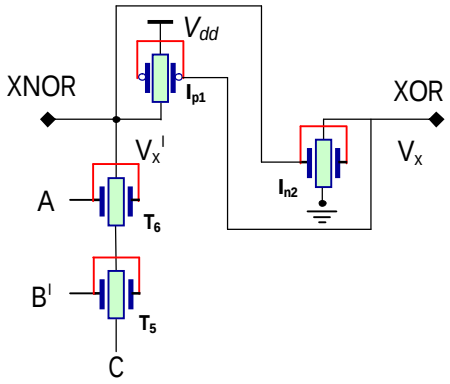

Fig.4.21 Equivalent circuit of Fig.3.4 for inputs A=logic 1, B= logic 0, C= logic 1

Its equivalent circuit is shown in Fig.4.21 for input pattern of 101 case. Similar to the above analysis, $V_x{}' = V_{dd}$ is achieved through the combination of transistors I_{p1} and I_{n2}.

(iv) For ABC=011 case

Similar to the above analysis, $V_X{}^I = V_{dd}$ is achieved through the combination of transistors I_{n2} and I_{p1}. Its equivalent circuit is shown in Fig.4.21 for input pattern of 101 case.

For another four cases of input patterns 000, 010, 100 and 110 of inputs, Vx and Vx^1 are strong values without considering the loop also.

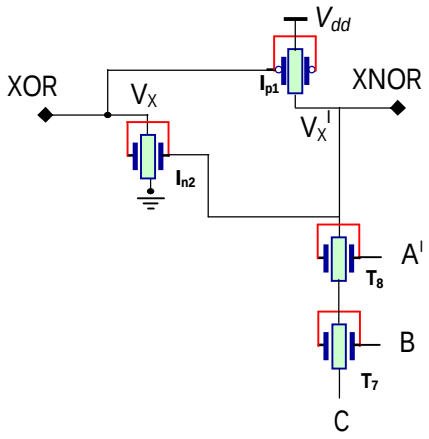

Fig.4.22 Equivalent circuit of Fig.3.4 for inputs A=logic 0, B= logic 1, C= logic 1

4.2.3 Rail to rail analysis of Fig.3.5

The proposed three input XOR/XNOR circuit-3 which is shown in Fig.3.5 is giving full swing for all input patterns. Actually patterns of 001, 110, 101 and 010 are suffering with the threshold loss problem, but that problem is avoided by using back to back inverter latch connection**.** That rail to rail analysis of Fig.3.5 is given below.

(i) For ABC=001 case

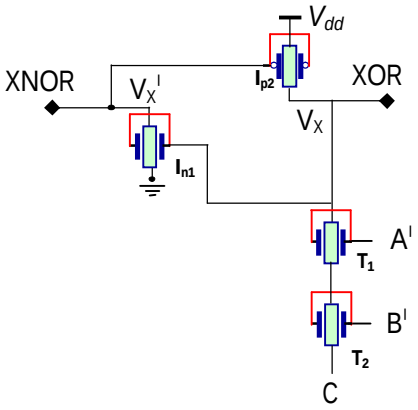

Fig.4.23 Equivalent circuit of Fig.3.5 for inputs A=logic 0, B= logic 0, C= logic 1

The input values are A = logic 0, B= logic 0, A^I = logic 1, B^I = logic1, Since the gate terminal of transistors T_1 and T_2 are connected to logic 1 i.e V_{dd}, T_1 and T_2 are Switched ON and input C value, i.e. logic high is passing through transistors T_1 and T_2 to node V_{XOR}. The transistors I_{n1} and I_{p2} are switched ON. Its equivalent circuit is shown in Fig.4.23. So the resistance of the FinFET transistor I_{p2} can be written as

$$R_P = \frac{V_{dsp2}}{I_{dsp2}} = \frac{L_g . t_{ox}}{\mu_P \varepsilon_{ox} W_{fin} \left(-V_{dd} - V_{th,p} + \frac{V_{th,n}}{2} \right)} \quad (4.16)$$

From the above equation, the resistance R_P is small. So

$V_X = V_{dd} - \text{drop across } R_P$

Therefore V_X is gaining its full rail swing.

(ii) For ABC=110 case

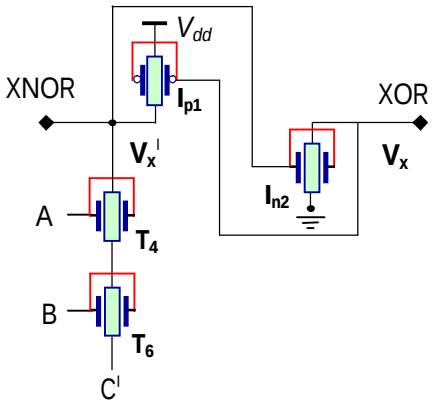

Fig.4.24 Equivalent circuit of Fig.3.5 for inputs A=logic 1, B= logic 1, C= logic 0

Its equivalent circuit is shown in Fig.4.24 for the input of 110. Similar to the above analysis, $V_x' = V_{dd}$ is achieved through the combination of FinFETs I_{p1} and I_{n2}.

(iii) For ABC=101 case

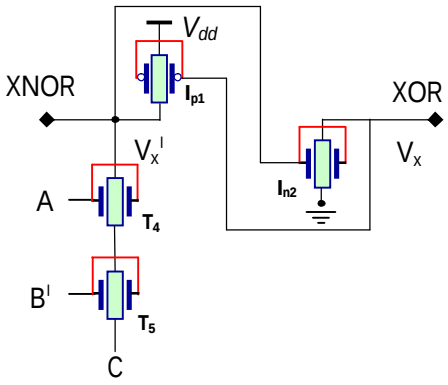

Fig.4.25 Equivalent circuit of Fig.3.5 for inputs A=logic 1, B= logic 0, C= logic 1

Its equivalent circuit is shown in Fig.4.25 for the input of 101. Similar to the above analysis, $V_x' = V_{dd}$ is achieved through the combination of transistors I_{p1} and I_{n2}.

(iv) For ABC=010 case

Its equivalent circuit is shown in Fig.4.26 for the input of 010. Similar to the above analysis, $V_X = V_{dd}$ is achieved through the combination of transistors I_{n1} and I_{p2}.

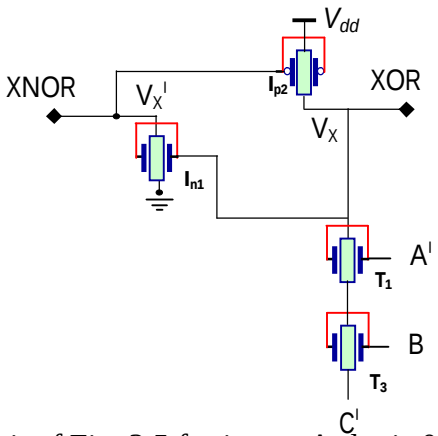

Fig.4.26 Equivalent circuit of Fig. 3.5 for inputs A=logic 0, B= logic 1, C= logic 0

For other four patterns 000, 011, 100 and 111 of inputs, Vx and Vx^1 are strong values without considering the loop also.

4.2.4 Sizing of the transistors

The size of transistors of Fig.3.5 arrived at appropriate sizing for T_1, T_2 and I_{p2} by solving (4.17):

$$\mu_n C_{ox}\left(\frac{W_{fin}}{L_g}\right)_{1-2}\left[\left(V_{dd}-V_{th,n}\right)V_{dsatn}-\frac{V_{dsatn}^2}{2}\right]= -\mu_p C_{ox}\left(\frac{W_{fin}}{L_g}\right)_{p2}\left[\left(-V_{dd}-V_{th,p}\right)V_{dsatp}-\frac{V_{dsatp}^2}{2}\right] \quad (4.17)$$

Thus the appropriate sizing for T_1, T_3 and I_{p2} by solving

$$\mu_n C_{ox}\left(\frac{W_{fin}}{L_g}\right)_{1-3}\left[\left(V_{dd}-V_{th,n}\right)V_{dsatn}-\frac{V_{dsatn}^2}{2}\right]=$$

(4.18):
$$-\mu_p C_{ox}\left(\frac{W_{fin}}{L_g}\right)_{p2}\left[\left(-V_{dd}-V_{th,p}\right)V_{dsatp}-\frac{V_{dsatp}^2}{2}\right] \quad (4.18)$$

Similarly the appropriate sizing for T_4, T_5 and I_{p1} by solving (4.19):

$$\mu_n C_{ox}\left(\frac{W_{fin}}{L_g}\right)_{4-5}\left[\left(V_{dd}-V_{th,n}\right)V_{dsatn}-\frac{V_{dsatn}^2}{2}\right]= -\mu_p C_{ox}\left(\frac{W_{fin}}{L_g}\right)_{p1}\left[\left(-V_{dd}-V_{th,p}\right)V_{dsatp}-\frac{V_{dsatp}^2}{2}\right] \quad (4.19)$$

Likewise the appropriate sizing for T_4, T_6 and I_{p1} by solving (4.20):

$$\mu_n C_{ox}\left(\frac{W_{fin}}{L_g}\right)_{4-6}\left[\left(V_{dd}-V_{th,n}\right)V_{dsatn}-\frac{V_{dsatn}^2}{2}\right]=$$
$$-\mu_p C_{ox}\left(\frac{W_{fin}}{L_g}\right)_{p1}\left[\left(-V_{dd}-V_{th,p}\right)V_{dsatp}-\frac{V_{dsatp}^2}{2}\right] \quad (4.20)$$

For sizing of transistors the relations similar to above equations have followed for Fig.3.3 and Fig.3.4 also.

Similar to the above analysis, the full rail to rail swing and sizing of transistors can be observed for the proposed circuits of 4-bit input, multi-input and 8-bit input XOR/XNOR structures of Fig.3.6, Fig.3.7 and Fig.3.8 respectively.

The proposed direct three input XOR circuit-1 (Fig.3.9) is based on the TGL, so for all combinations of input it produced full swing. The proposed direct three input XOR circuit-2 (Fig.3.10) and circuit-3 (Fig.3.11) are also produced full swing since extra inverter is used at the output node as these circuits are implemented with PTL. Fig.3.12 and Fig.3.13 of two input XNOR circuits are designed in a structure such that they will produce full swing for all the combinations. And all these circuits are ratio-less designs so for all these minimum sized transistors are used.

4.3 Self-checking XOR/XNOR Circuit: Fig.3.13

The proposed self-checking XOR/XNOR circuit of Fig.3.13 is satisfying the code disjoint, fault secure and self checking properties. To examine these properties, the analysis is taken w.r.to stuck-at faults, stuck-on faults and stuck-open faults by considering valid and invalid inputs into consideration.

4.3.1 Analysis of logical Stuck-At faults

Table 4.1 shows the outputs of the proposed circuit by choosing the logical stuck-at faults into consideration. Both Stuck-at 0 and stuck-at 1 faults are considered in single

Table 4.1 Codes Disjoint & Fault Secure Properties for Logical Stuck-At Faults

I/P A	**I/P A^1**	**I/P B**	**I/P B^1**	**O/P XOR**	**O/P XNOR**	**Detection of Multiple Fault(MF), Single Fault(SF)**
Stuck-at 0	Stuck-at 0	Stuck-at 0	Stuck-at 0	1	1	Detected MF
Stuck-at 0	Stuck-at 0	0	1	1	1	Detected SF
Stuck-at 0	Stuck-at 0	1	0	1	1	Detected SF
Stuck-at 0	Stuck-at 0	1	Stuck-at 1	1	1	Detected MF
0	1	Stuck-at 0	Stuck-at 0	1	1	Detected SF

0	1	0	1	0	1	No Fault
0	1	1	0	1	0	No Fault
0	1	Stuck-at 1	Stuck-at 1	0	0	Detected SF
1	0	Stuck-at 0	Stuck-at 0	1	1	Detected SF
1	0	0	1	1	0	No Fault
1	0	1	0	0	1	No Fault
1	0	Stuck-at 1	Stuck-at 1	0	0	Detected SF
Stuck-at 1	Stuck-at 1	Stuck-at 0	Stuck-at 0	1	1	Detected MF
Stuck-at 1	Stuck-at 1	0	1	0	0	Detected SF
Stuck-at 1	Stuck-at 1	1	0	0	0	Detected SF
Stuck-at 1	Stuck-at 1	Stuck-at 1	Stuck-at 1	0	0	Detected MF

and multiple number. Here both struck-at 0 and struck-at 1 faults are examined. From Table 4.1 it can be inferred that for faulty inputs, outputs generated are faulty. From the Table 4.1 the proposed circuit in Fig.3.13 is concluded as fault secure and code disjoint for both single and multiple faults.

4.3.2 Analysis of Stuck-ON faults

Fig.3.13 is studied for both struck-on and struck-open conditions of possible single faults. Table 4.2 demonstrates that the circuit depicted in Fig.3.13 satisfied fault secure and self testing properties for all struck-on transistor anomalies.

Table 4.2 Fault Secure and Self-Testing Properties for Stuck-ON Faults

Stuck-ON @ Transistor	**I/P Vector (A,B) detecting the Stuck-ON Fault**
P_1	(0,ϕ)
P_2	(ϕ,1)
P_3	(1,ϕ)
P_4	(ϕ,0)
P_5	(1,ϕ)
P_6	(ϕ,1)
P_7	(1,ϕ)
P_8	(ϕ,1)
N_1	(0,ϕ)
N_2	(ϕ,0)
N_3	(1,ϕ)
N_4	(ϕ,1)
N_5	(0,ϕ)
N_6	(ϕ,1)
N_7	(1,ϕ)
N_8	(ϕ,0)

Note: ϕ: logic 0 or 1 indefinitely

4.3.3 Analysis of Stuck-OPEN faults

Table 4.3 demonstrates that the transistor P_1 stuck-open results the output fluctuating for the input pattern of '1 1'. So the proposed Fig.3.13 is concluded as fault secure and self testing as it detects struck open fault at transistor P_1.

Table 4.3 Transistor P_1 Stuck-Open

Inputs		**Outputs without Fault**		**Outputs with Fault**		**Conclusion**
A	**B**	**XOR**	**XNOR**	**XOR**	**XNOR**	
0	0	0	1	0	1	Both outputs are Valid
0	1	1	0	1	0	Both outputs are Valid
1	0	1	0	1	0	Both outputs are Valid
1	1	0	1	0	X	XNOR is not Valid

Table 4.4 displays the fault secure and self-testing properties of the proposed circuit for stuck-open faults in a single transistor. From Table 4.4, it can be examined that any single fault can be detected out by any valid input code word.

Hence, from the above analysis, it can be concluded that the proposed circuit is totally self checking for all single stuck-at 0, stuck-at 1, stuck-open and stuck-on faults.

Table 4.4 Transistors with Stuck-Open Condition and Fault Detected Cases

Transistor	**Inputs**		**Outputs without Fault**		**Outputs with Fault**		**Conclusion**
	A	**B**	**XOR**	**XNOR**	**XOR**	**XNOR**	
P_1	1	1	0	1	0	X	XNOR is not Valid
P_2	0	0	0	1	0	X	
P_3	0	0	0	1	0	X	
P_4	1	1	0	1	0	X	
P_5	1	0	1	0	X	0	XOR is not Valid
P_6	0	1	1	0	X	0	
P_7	0	1	1	0	X	0	
P_8	1	0	1	0	X	0	
N_1	1	0	1	0	1	X	XNOR is not Valid
N_2	0	1	1	0	1	X	
N_3	0	1	1	0	1	X	
N_4	1	0	1	0	1	X	
N_5	1	1	0	1	X	1	XOR is not Valid
N_6	0	0	0	1	X	1	
N_7	0	0	0	1	X	1	
N_8	1	1	0	1	X	1	

Note: X- logic 0 or 1 indefinitely

4.3.4 Sizing of transistors

The aspect ratios of the n-FinFET and p-FinFET transistors in Fig.3.13 are chosen by using the relation

$(W/L)_p = 2 * (W/L)_n$ since $\mu_n \simeq 2 * \mu_p$

4.4 Sub-threshold operated DCVSL XOR/XNOR circuits: Fig.3.17 to Fig.3.18

The MOS transistor will operate in sub-threshold region when Vgs < Vt. The current is modeled as (Alexander Fish Arkadiy and Morgenshtein, 2005)

$$I_{ds} = I_{d0} . W/L. e^{(qVgs / KT)} \quad (4.21)$$

Where $I_{d0} = I_0 [e^{(qVgs / nKT)} -1]$, I_0 is reverse current, n- sub-threshold slope factor and it is between 1 to 2, q is charge of electron, K is Boltzman constant and T is temperature in degrees or kelvin.

Here the transistor widths (W) and Vgs are varied in simulator to get the operation in sub-threshold operation.

4.5 Ternary XOR and XNOR gates using CNTFET: Fig.3.19 to Fig.3.26

The threshold voltage of a CNTFET is expressed by (4.21) (M. H. Mouiyeri et al, 2013)

$$V_{th} \simeq E_{bg}/2e \simeq 0.436/D_{cnt} \text{ (nm)} \quad (4.22)$$

Where E_{bg} -- band-gap,

e -- unit electron charge

D_{cnt} -- diameter of the nanotubes

m, n -- chirality values

It can be concluded from (1) that the threshold voltage (V_{th}) of a CNTFET is inversely proportional to the diameter (D_{cnt}) of its nanotubes, which is computed by (4.22) (M. H. Mouiyeri et al, 2013)

$$D_{cnt} = 0.0783 \sqrt{m^2 + n^2 + mn} \quad (4.23)$$

where m, n – chirality values

By using equations (4.21) and (4.22), the chiralities, diameters and threshold voltages of proposed circuits are calculated. That analysis is given below.

4.5.1 STXOR (Fig.3.18) and STXNOR (Fig.3.20)

The supply voltage used is +0.9V. To get logic 0 (0 V), logic 1 (+0.45 V) and logic 2 (+0.9 V), the required threshold voltages for p- CNTs are –0.289 V, –0.428 V and –0.559 V and the threshold voltages for n-CNTs 0.289 V, 0.428 V and 0.559 V.

Hence, the chirality vectors of the CNTFETs chosen as (19, 0), (13, 0) and (10, 0) so their diameters according to (2) are 1.487nm, 1.018nm and 0.783nm respectively. And (19, 0) chirality values are used for p-CNTFETs C1 to C4 and n-CNTFETs C11 to C14. The chiralities (10, 0) are chosen for p-CNTFETs C5 to C8 and n-CNTFETs C15 to C18. The chirality (13, 0) is used for CNTs C9 and C10.

4.5.2 PTXOR (Fig. 3.19) and PTXNOR (Fig. 3.21)

The supply voltage used is +0.9V. To get logic 0 (0 V) and logic 2 (+0.9 V) as in the output it has only two logic levels of logic 0 and logic 2, the required threshold voltages of n-CNTFETs are 0.559V and p-CNTFETs are – 0.289 V. So the chirality values chosen for n-CNTFETs are (10, 0) and for p-CNTs are (19, 0) hence these results 0.783 nm and 1.487 nm diameters respectively.

4.5.3 NTXOR (Fig. 3.19) and NTXNOR (Fig. 3.21)

For the supply voltage of +0.9V, to get logic 0 (0 V) and logic 2 (+0.9 V) as in the output it has only two logic levels of logic 0 and logic 2, chiralities (10,0) and (19,0) are selected for p-CNTs and n-CNTs. Therefore, the obtained threshold voltages are – 0.559 V and 0.289 V for p and n-CNTs respectively. And corresponding diameters are 0.783 nm and 1.487 nm.

4.5.4 Pseudo STXOR (Fig. 3.22) and STXNOR (Fig. 3.24)

The supply voltage used is +0.9V. To get logic 0 (0 V), logic 1 (+0.45 V) and logic 2 (+0.9 V), the selected chirality of the CNT C1 is (7, 0) and (13, 0) is for C2, (19, 0) is for CNTs C3 to C6 and (11, 0) is for CNTs C7 to C10. So their diameters are computed as 0.548 nm for C1, 1.017 nm for C2, 1.487 nm for C3 to C6 and 0.861 nm for C7 to C10. Hence the threshold voltages of C1 and C2 are calculated as –0.795 V, and –0.428 V respectively, and Vth is 0.289V for C3 to C6 and 0.506V for C7 to C10 similarly.

4.5.5 Pseudo PTXOR (Fig. 3.23) and PTXNOR (Fig. 3.25)

For the supply voltage of +0.9V, to get logic 0 (0 V) and logic 2 (+0.9 V) as in the output it has only two logic levels of logic 0 and logic 2, for both PTXOR and PTXNOR, the chiralities selected for n-CNTs C2 to C5 are (10, 0) and the chirality for P-CNT C1 is (7, 0). So, the diameters are calculated as 0.783 nm and 0.548 nm for n-CNTs and p-CNT respectively, results 0.559 V is the threshold voltages of n-CNTFETs and –0.795 V is the threshold voltage of p-CNTFET.

4.5.6 Pseudo NTXOR (Fig. 3.23) and NTXNOR (Fig. 3.25)

For the supply voltage of +0.9V, to get logic 0 (0 V) and logic 2 (+0.9 V) as in the output it has only two logic levels of logic 0 and logic 2, for both NTXOR and NTXNOR, the chiralities selected for n-CNTs C2 to C5 are (20, 0) and the chirality for P-CNT C1 is (7, 0). So, the diameters are calculated as 1.566 nm and 0.548 nm for n-CNTs and p-CNT respectively, results 0.278 V is the threshold voltages of n-CNTFETs and –0.795 V is the threshold voltage of p-CNTFET.

4.6 Performance

The computational ability defines the performance of the system. And it is expressed in terms of propagation delay. The propagation delay of a circuit defines how fastly it gives response to a change at its inputs. It represents the delay faced by a signal when passing through a circuit. It is measured between the 50% transition points of the input and output waveforms with the assumption of switching threshold is typically in the middle of the logic swing, as shown in below figure (J.M. Rabaey et al,2003). Two definitions of the propagation delay are necessary because a circuit displays different response times for rising or falling input waveforms. The propagation delay t_{pLH} defines the response time of the gate for a low to high (or positive) output transition, while t_{pHL} refers to a high to low (or negative) transition. The propagation delay t_p is defined as the average of the two (J.M. Rabaey et al,2003), and it is shown in Fig.4.27.

$$t_p = \frac{t_{pLH} + t_{pHL}}{2} \tag{4.24}$$

The delay depends on circuit technology, topology, pattern of inputs and supply voltage. In the proposed circuits, for getting more speed the circuit topology is taken as pass transistor logic as it is better in the performance and designed with different technologies like MOSFET, FinFET and CNTFET transistors for better performance.

For all different input combinations, the delay is calculated based on above definition using Cadence Virtuoso tool from the simulated results. And among all the worst case propagation delay is considered for specifying the propagation dealy of the circuit. These propagation delay values for the existed circuits and proposed circuits are given in the next chapter.

Delay of a circuit depending on the supply voltage as follows from (J.M. Rabaey et al,2003),

$$\tau = KC_L \frac{V_{dd}}{(V_{dd} - V_{th})^2} \quad (4.25)$$

where τ is the circuit delay, K is the gain factor, C_L is the load capacitance, V_{dd} is the supply voltage, and V_{th} is the threshold voltage. The above equation (4.24) shows that reducing supply voltage will have a negative effect on the speed of the circuit. To show this we have simulated the proposed circuits for a range of different voltages. The simulated propagation delay values for the existed circuits and proposed circuits are given in the next chapter.

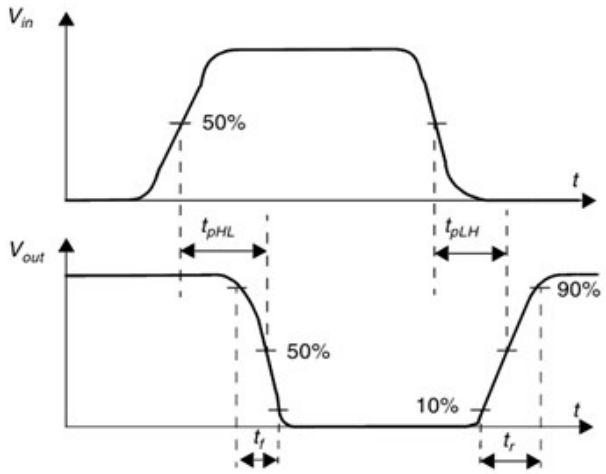

Fig.4.27 Propagation Delay calculation (J.M. Rabaey et al, 2003).

Delay of any circuit can be calculated by converting the ON transistors in the critical path in its terms of resistance and capacitance according to Elmore delay (J.M. Rabaey et al, 2003). Hence, in order to improve the speed of the design, we have to see to it that the critical path consists of less number of transistors and with minimum capacitance. So to get higher performance, circuits which are having less number of transistors in the critical path are designed.

4.7 Power Consumption

The power consumption of a design determines how much energy is consumed per operation, and how much heat that circuit dissipates. The power dissipation is an important property of a design that affects feasibility, cost and reliability.

Total power consumption of a CMOS circuit can be given as in the below equation (J.M. Rabaey et al, 2003)

$$P_{avg} = P_{switching} + P_{short\text{-}circuit} + P_{static} = \frac{1}{2} \alpha C_L V_{dd}^2 f + I_{sc} V_{dd} + I_{leakage} V_{dd} \quad (4.26)$$

Where $P_{switching}$ refers to the dynamic component of power, C_L is the load capacitance,

f is the clock frequency, and α is the switching activity. The equation of the switching power depends on the square of the supply voltage (V_{dd}). $P_{short\text{-}circuit}$ is due to the short circuit current I_{sc} which arises due to the direct path between the supply rails during output transitions. P_{static} is due to the leakage current $I_{leakage}$ which is a summation of bias current and sub threshold currents.

The dominant source of power dissipation is the switching power dissipation. As the switching power is proportional to the square of the operating voltage, reduction in voltage offers the most effective means to minimize power consumption. With scaling down of the supply voltage the effect of static power consumption increases with MOSFET technology. Static power is primarily determined by the technology used. To reduce both switching and static powers, the proposed circuits used FinFET technology, since FinFET technology is advantageous than MOSFET technology at lower supply voltages which discussed in chapter 1 in sections 1.4 and 1.5. And we have designed circuits with requirement of less count of total transistors and the number of transistors operating at a time in the circuit is less in number. So total dynamic and static power consumptions are reduced.

The short-circuit power consumption, is avoided by avoiding the static paths in the proposed designs and these depend on the rise and fall timings of inputs and outputs. The proposed circuits have equal input and output edge timings so the minimum short-circuit current flows and results minimum short-circuit power consumption. We have measured the total power consumption in simulation using Cadence Virtuoso tool and the values are given in the next chapter.

4.8 Monte Carlo Analysis

Device mismatches, the small random variations in the characteristics of identically designed devices, occur during the manufacturing of integrated circuits. These mismatches result in behavioral variations of analog and digital integrated circuits. Except for very small circuits, it is difficult to analytically predict the behavior of a circuit due to the combination of the mismatch errors of individual devices. The impact of these random parameter variations on circuit behavior can be studied with Monte Carlo simulation by analyzing a large set of circuit instantiations with randomly varied devices. (H. Hung et al, 2006). The definition of Monte Carlo is "Monte Carlo methods are a broad class of computational algorithms that rely on repeated random sampling to obtain numerical results". Simplifying the definition, Monte Carlo algorithms are used for introducing random variations within the given

limits to explore the corner cases of any problem. The problems fed to Monte Carlo algorithms are spanned over a wide variety of applications including Risk Analysis, Finances, Statistics, Physics, and Electronic Designs (K.R. Lakshmikumar et al, 1986).

In VLSI circuit design during simulation, we run the design through various PVT (Process, Voltage and Temperature) corners with an aim that the circuit should be able to reliably operate at all the extreme conditions. These PVT variations can be generalized as:

(i)Temperature from as low as -40° to as high as 125°C,

(ii)Voltage ±10% variation from its nominal value

(iii)Process – This is generally two letter convention where the first letter is the behavior of NMOS and the second letter is of PMOS. TT, SS, FF, SF and FS are the corners generally used. Letter T stands for Typical (Nominal V_{th}), F for Fast (Low V_{th}) and S for Slow (High V_{th}). Running the design over different PVT corners cover the environmental variations (voltage and temperature) as well as manufacturing variations (process). It aids in introducing the randomness into the transistors by changing its V_{th} in different directions such that all the transistors are different at a time, depicting the real silicon behavior.

The Spectre simulator tool from Cadence systems can support this Monte Carlo simulation for transient, DC, AC and corner alnalyses by taking random noises into consideration. It generates a user specified number of modified netlists with randomly varied device characteristics. Each circuit device is modified according to a mismatch model for the device type. A user supplied parameters file controls the magnitude of variation for each device type and the tool automatically adjusts the parameter distributions of different device types and sizes. All netlists are simulated and their results are aggregated. These results reflect the tolerance of a circuit to device mismatch errors.

Transient, Noise and DC Monte Carlo analyses of all the proposed circuits are performed. Noise Montecarlo analysis was performed by varying the temperature from -60° to +130° and DC supply voltage from +0.8V to +1.8V. The transient Monte Carlo response is simulated for 200 random samples. The plots of histograms for two outputs are showing the number of output samples is appearing at what values of outputs. The robustness of the proposed circuits from these results is given in the next chapter.