CHAPTER I

INTRODUCTION

1.1 General

1.1.1 Digital circuits

In the past few years, most of the people are enthralled by the digital or binary logic. The very thought that a two-valued number system, can possibly be the foundation for the most potent and sophisticated computers seems astounding, to say the least. However, it is so, and the how and the why of these take some explanation. Everything in the digital world is based along the binary number scheme. Numerically, this requires just two symbols: 0 and 1. Logically, we can apply these symbols or we can equalize them with other symbols according to the demands of the moment. Therefore, when handling with digital logic, we can define that symbol '0' = Low = False =No and symbol '1' = High = True =Yes.

Applying this two-valued logic system, every statement or status must be either 'true' or 'false': it cannot be partially true and partially untrue.While this approach may appear limited, it has really resulted in quite nicely, and can be spread out to make very complex relationships and interactions among any number of individual conditions. Data integrity in this discrete representation is much better than that of analog form representation because here data loss involves an arbitrary alteration of the condition of a device, not a drift in value. That is lots less likely, and there are ways to compensate for it.

A few decades ago, humans only used to perform some complex things which now computers do with an apparent ease. Things that require human thought are done by connecting chips made of silicon. This can best be seen with the help of Boolean logic, a logic, originally made by George Boole in the mid 1800s that allows quite a few unexpected things to be mapped into bits and bytes. The powerful thing about Boolean logic is that, once you get the flow of things, it is outrageously simple. It helps in turning 1's and 0's into meaningful information.

A logic gate is nothing but an arrangement of electrically controlled switches, commonly called as transistors. Each logic gate is used to represent a function of a Boolean logic. A digital circuit of simple to complex is realized using these logic gates.

1.1.2 Logic gates

A logic gate is a placement of controlled switches used to calculate operations using Boolean logic in digital circuits. They are primarily carried out electronically, but can likewise be constructed using electromagnetic relays, electronic diodes, fluids, optical or even mechanical elements.

Cardinal characteristics of the logic gates are:

- the capability to connect to single or two input wires
- the capability to connect to one output wire
- the capability to obtain a value from a connected input wire
- the capability to carry a value to a connected output wire
- the capability to compute correct output value, given current input value(s).

The four types of basic logic gates are AND, OR, XOR and NOT gates. With these four, any conceivable Boolean equation can be put through. Nevertheless, for convenience, the derived types NAND, NOR and XNOR are also practiced, which often use fewer circuit elements for a given equation than an implementation based solely on AND, OR, XOR and NOT would do.

1.1.3 Exclusive OR logic gates

The Exclusive OR logic gate is one of the logic gates that perform an exclusive or operation; i.e, a true output results if one, and only one, of the inputs to the gate is true. A false output results if both the inputs are false and both are true. XOR represents the inequality function, i.e., the output is high if the inputs are unalike otherwise the output is low. A way to think XOR is 'one or the other, but not both'. XOR can also be seen as addition modulo-2 and it can also called as arithmetic gate. Because of this, XOR gates are utilized to perform binary addition in computers. A basic digital adder is the half adder, which adds two bits, that comprises of an XOR gate for sum and an AND gate for carry.

The algebraic expressions $A.B^1+A^1.B$ and $(A+B).(A^1+B^1)$ either used to represent the XOR gate with inputs A and B and the operation of exclusive OR is summarized in the below truth table named as Table 1.1. XNOR is complementary to XOR.

Applications of Exclusive OR logic gates are:

The Exclusive OR circuit is the basic building block of various circuits mainly arithmetic circuits like adders, multipliers, compressors, comparators, pseudo random number generators, parity generators or checkers, code converters, correlation &

sequence detectors, error detecting and error correcting codes, phase detector circuit in PLL and encryption processor. Hence it is used widely in many VLSI systems as a section of the critical path that determines the altogether performance of the system. So enhancing the performance of the XOR gate is important in reducing the propagation delay and power consumption.

Table 1.1 Two input Exclusive OR Truth Table

A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

1.2 Basic Exclusive OR Logic Gates

The XOR gate circuit can be constructed by using AND, OR and NOT gates. Then this approach needs two AND gates, one OR gate and two NOT gates, totally five gates of three different types. Alternatively, it can be constructed by using four NAND or five NOR gates in the forms as indicated in Fig.1.1 and Fig.1.2.

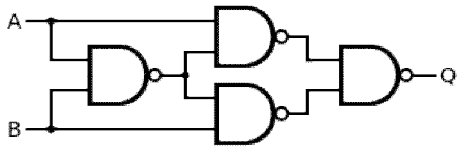


Fig.1.1 Two input Exclusive OR using NAND gates (M. M. Mano, 1979)

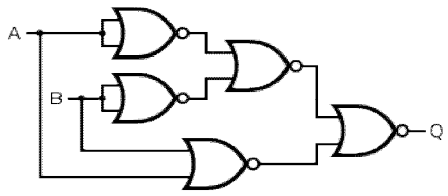


Fig.1.2 Two input Exclusive OR using NOR gates (M. M. Mano, 1979)

But such kind of arrangements occupy much space of the room, hence direct designs of XOR logics is preferable. Exclusive OR logic gates with more than two inputs are generally used. For example, in adders and parity generators as well as checkers three input exclusive OR logic gates are used predominantly. For the implementation of modulo-2 adder, it is more usual to regard subsequent inputs as being employed through a cascade of binary exclusive OR operations: the first two signals are run into an XOR gate, then the output of that gate is run into a second XOR gate together with the third signal, and so on for any remaining signals. So that circuits results an output of 1 when the number of 1s is odd at inputs otherwise it results output of 0. This

traditional implementation experiences a significant delay because of cascading number of gates to obtain the desired exclusive OR function as the gate delay will be added to the overall propagation delay of the circuit. Hence, high performance designs and direct designs are preferable. Some of the high performance designs and direct designs of three input exclusive OR logic gates are discussed in the next chapters.

1.3 CMOS Logics to Implement XOR/XNOR Gates

The growth of the semiconductor industry is forcing the designers to shift for the smaller silicon area, higher speed, longer battery life and dependability (H.E Neil Weste et al, 1993). The semiconductor industry has found an explosive growth in multimedia based applications in the last decade, as experienced with laptops, cell phones, sensors, smart card and many other applications. In most of these applications, exclusive OR logic gate comprises a portion of the critical path which significantly affects the worst-case delay and the overall performance of the system. The XOR and XNOR gates are the substantial pieces of different digital systems and are highly utilized in VLSI systems such as arithmetic and logic circuits (S.C. Yuan et al, 2007, R.F. Mirzaee et al, 2010, K. Navi et al, 2008a, K. Navi et al, 2008b,K. Navi et al, 2009), crypto processors (H.W.Kim et al, 2004), test pattern generators (X. Zhang et al, 2008), parity checkers, comparators (M.M. Mano, 1979, J.M. Rabaey et al, 2003) and so forth. Therefore, improving the functioning of the XOR gate contributes to an overall improvement in the system performance.

1.3.1 Static Complementary Logic

In literature, so many circuit styles are existing to construct a given logic function. The more typical design metrics used to examine a gate area, speed, power and energy. Add on to these metrics, robustness to noise and reliability are also really important considerations (J.M. Rabaey et al, 2003). The most common design style in modern VLSI design is the Static CMOS logic style. The primary advantages of this style are robustness, good performance and low power consumption.

In static circuits, the output of the gate is connected to either V_{dd} or V_{ss} via a low resistance path and the outputs of gate take at all times the value of the Boolean function implemented by the circuit. This style basically consists of two networks named pull up network (PUN) and pull down network (PDN). The function of PUN is to make a connection between V_{dd} and output to give output as logic 1. Similarly, the PDN makes a connection between V_{ss} and output to give output as logic 0. Both the

networks are connected such that either PUN or PDN networks are conducting at any point of time i.e. in steady state.

To implement logic gates this complementary static CMOS logic, it provides the advantages of robustness and simplicity in designing approach. It induces a trouble of needing 2N number of transistors for N fan-in. This can ensue in a significantly large area and more propagation delay as fan-in increases. In fact, the unloaded intrinsic delay of the gate is, at worst, a quadratic function of the fan in.

Hence the static CMOS logic style has, though, been greatly robust and scalable with technology, it needs 2N number of transistors to construct an N input gate. Also, the load capacitance is important, since each gate steers both pMOS and nMOS devices per each fan out. Thus, it leads to the development of alternative CMOS logics which are faster and simpler.

1.3.2 Pass Transistor Logic

Pass Transistor Logic (PTL) (R. Zimmermann et al, 1997) is the most popularly and extensively used alternative to complementary static CMOS, which reduces the number of transistors needed to implement logic by considering the main inputs to drive gate terminals as well as source drain terminals.

In this approach a small number of transistors are needed to implement the given logic. For instance, the construction of an AND gate using PTL requires four transistors while a complementary static CMOS implementation would need six transistors. Resultant of lower capacitance is the additional advantage with the reduced number of devices. But in this PTL, an NMOS transistor is strong at passing a '0', but is poor at hauling a node to V_{dd}. The output charges up to (V_{dd}-V_{tn}) when the NMOS pass transistor hauls a node high. Actually, the position is exacerbated by the fact that the devices undergo body effect, because a sufficient source-to-body voltage is present when pulling high. Similarly a PMOS pass transistor faces the problem for pulling node to '0'. Due to the reduced voltage swing, the pass transistors need low switching energy to charge up a node. This PTL consumes static power, even though it exhibits lower switching power. And the reduced voltage level may be insufficient to operate the next stage circuits. To handle this problem, the suggested solutions are level restoration, multiple threshold transistors and transmission gate logic.

1.3.3 Transmission Gate Logic

Transmission Gate Logic (TGL) is generally used solution to handle the threshold voltage loss problem with the PTL. TG consists of the parallel combination of nMOS

and pMOS devices so that it will get the best flavors of both devices. The best approach is to use the nMOS device to pull down and the pMOS device to pull up since the nMOS device gives a strong '0' and a weak '1' and the pMOS device gives strong '1' and weak '0'. Though the transmission gate requires two transistors and more control signals, it enables rail to rail swing.

1.3.4 Differential CMOS Logic

Circuit design techniques have largely overlooked differential cascode logic circuits in favor of traditional CMOS styles. This is mainly because the high activity of DCVS gates causes them to compare unfavorably with respect to conventional CMOS implementations from a power perspective (K.M. Chu et al,1987). The need to route differential signals, and the high clock load of clocked DCVS styles are known disadvantages. However, this sort of logic has potential advantages as compared to standard CMOS NAND (NOR) implementations. High complexity, high fan-in gates are possible. Complex gates can be implemented with less number of transistors. Certain clocked DCVS families have very low propagation delay for large complex gates. Clocked DCVS styles often integrate both the sequential and combinatorial portions into a single complex gate. This style of logic is hence suitable for high-speed VLSI. Both true and complementary outputs are available. This makes the completion of gate evaluation easy to detect. It is this reason which makes DCVS gates the logic family of choice for implementing self-timed circuits. In common with dynamic logic, gate input loading is very light and consists of few NMOS transistors. The high power of DCVS gates is a definite hindrance toward their greater acceptance. The power consumed by a DCVS gate can be subdivided into the power consumed because of outputs switching and the power consumed because of switching at the gate internal nodes. As the gate complexity increases, the number of internal nodes switched in the nMOS evaluation tree increases. Hence power dissipation due to switching in internal nodes is a dominant factor of the total gate power.

Over the years, various XOR/XNOR designs reported (Masaru Uya et al, 1983, I.J.Sanwo et al, 1988, H.E Neil Weste et al, 1993, W.Jyh-Ming et al, 1994, S.C. Fang et al, 1996, K.H. Cheng et al, 1999, Y. Tsujihashi et al, 1999, P.Couteaux et al, 2000, D. Radhakrishnan et al, 2001, A.M. Shams et al, 2002, S. Geol et al, 2006, S.S Mishra et al, 2009, S.Bonsels et al, 2009, M. H.Moaiyeria et al, 2010,R. Kumar et al, 2011, Jin-Uk Shin et al, 2012, N. Ahmad et al, 2013, S. Musala et al, 2013) based on Complimentary Pass Transistor Logic (CPL), Pass Transistor Logic (PTL), Double

Pass Transistor Logic (DPL) and Transmission Gate (TG) logic to enhance the performance of time synchronized applications like wave-pipelined systems. Family of Pass Transistor Logic (PTL) had been a popular choice due to identical logic depth to this end. However, this logic style has its limitation due to data-dependent output level and input loading.

1.4 Problems with CMOS Scaling

In the advanced integrated circuit technology, the big challenges are producing MOSFETs with channel lengths much lower than a micrometer and its fabrication. In recent times, if the size of the MOSFET is reduced to a few tens of nanometers, it made some operational problems (N. Z Haron et al, 2008). Some of the problems are given below:

- Higher sub threshold conduction

As the size of MOSFET shrinks, the voltage that can be given to the gate must be decreased to maintain reliability. To sustain the performance, the threshold voltage of the MOSFET has to be decreased as well. Since threshold voltage is decreased, the transistor cannot be shifted from complete turn-off to complete turn-on. With the availability of limited voltage swing, the design of the circuit has weakened between strong current in the ON state and low current in the OFF state. Now sub-threshold leakage, including sub-threshold conduction, gate-oxide leakage and reverse-biased junction leakage can consume more than half of the total power consumption of modern designs.

- Increased gate-oxide leakage

The thin gate oxide layer, which functions as an insulator between the gate and the channel, should be manufactured as lean as possible to rise the conductivity of the channel and performance when the transistor is in ON state and to lessen sub-threshold leakage when the transistor is in OFF state. Oxide thickness (t_{ox}) has been scaling with each technology generation. We have reached the point where t_{ox} is so small. The direct tunneling occurs if t_{ox} < 2nm. Gate leakage is function of t_{ox} and V_G. For reliable device operation, the maximum electric field across a device gate oxide should be limited to 7MV/cm (R. Jacob Baker etc, 2003). This translates into $0.7V/10A^0$ of gate oxide.

- Gate oxide tunneling

This direct gate tunneling current could be the dominant source of device leakage, leading to faulty circuit operation and the increase in standby power in the MOSFET.

In the ultra thin oxide MOSFETs, the application of the gate voltage has a big role in the type of leakage current. Reduction of gate oxide thickness results in an increase in the field across the oxide. The high electric field coupled with low oxide thickness results in tunneling of electrons from substrate to gate and also from gate to substrate through the gate oxide, resulting in the gate oxide tunneling current. Typically, the conduction band offset between Si and SiO_2 is 3.2eV and the valence band offset is 3.7eV, and holes have a much lower tunneling probability in oxide than electrons. As a result, the leakage current limit will be reached first for n-type MOSFETs. Due to the small oxide thickness, which results in a small width of the potential barrier, the electrons at the strongly inverted surface can tunnel into or through the SiO_2 layer and hence give rise to the gate current. One of the most important effects that limit scaling is the tunneling of carriers through the energy barriers in the device. This tunneling results in leakage current, which increases power dissipation and decreases logic operating margins. Oxide tunneling between gate and channel is the most prominent and well known of these leakage currents. In n-FETs leakage current is due to the tunneling of electrons from the channel to the gate. In p-FETs the tunneling current is due to hole tunneling from channel to gate for very thin oxides (<1.5 nm) and low voltages, but at higher bias it is more often due to tunneling of electrons from the valence band of the gate into the conduction band of the body. This asymmetry exists because the valence-band barrier height is ~5 eV, while the conduction-band barrier is only ~3 eV.

- Increased junction leakage

Junction design is more complex in the smaller devices so it contributes to problems of shallower junctions, higher doping levels, halo doping and so forth all to decrease drain-induced barrier lowering. Source and drain junctions are normally reverse-biased so they will leak current. Typically very small but may increase with scaling since doping levels are very high in future technologies i.e breakdown voltage decreases as doping increases. nMOS leakage is 3 to 10 times PMOS leakage (electrons vs. holes). Below 20 A^0, the leakage increases by 10 times for every $2A^0$ in gate thickness reduction. For 90 nm, 1V, $t_{ox} < 20\ A^0$, the gate leakage current density J for pMOS transistor is $1x10^{-7}$ A/ μm^2 and for nMOS transistor is $3x10^{-7}$ A/ μm^2.

- DIBL

The threshold voltage V_T becomes a function of V_{ds}. As V_{ds} increases, depletion region increases. So gate voltage needed to create channel is now less. Hence V_T

decreases with increase in V_{ds}. This effect is named as Drain Induced Barrier Lowering.

- V_T roll-off

As the length of the channel is decreased, the depletion region of source and drain starts coming closer and it will make the threshold voltage as a function of the channel length. This is called V_T roll-off.

- Lower Output Resistance

The sensitivity of the MOSFET current to the drain voltage increases due to growing proximity of drain and gate of devices are made smaller. But required is a high output impedance to produce good gain.

- Lower Transconductance

As the size of the MOSFET is reduced, the dopant impurity levels and the fields in the channel increase. So carrier mobility is reduced due to these changes, and hence the transconductance. Both transconductance and current are limited due to velocity saturation of carriers. This velocity saturation happened due to rise in the electric field in the channel as channel lengths are reduced without proportional reduction in drain voltage.

1.5 FinFET Transistor

The growing need of energy efficient circuits that work at low voltages with low power consumption has led to an idea of low voltage circuits. MOS circuits are found to be the perfect solution to fit into this idea. But as the threshold voltage cannot be scaled down proportionally with respect to the supply voltage of the MOS circuits, the MOS circuits face difficulties in the sub-threshold region of operation. Several methods were proposed to make the operation of MOS circuits possible at sub-threshold region. One among such methods is voltage-boost logic where the internal voltage of some nodes is boosted to a voltage level higher than the supply voltage. And another is having different other technologies like FinFET, TFET, HTFET etc. When compared to the single gate MOSFET, the FinFET provides different advantages for reducing the sub-threshold and gate dielectric leakage currents simultaneously. It has lesser gate leakage, well built gate control and ability of minimizing short channel effects. Due to these surpassing characteristics FinFET device shows advantages in terms of performance, power, sizing of transistors and speed in sub-micron or sub-threshold regions. The FinFET presents the double gate silicon-on-insulator device, so that it helps to avoid the short channel effects and to

mitigate drain-induced barrier lowering. A narrow channel placed between source and drain is named as “Fin”. It is isolated from its gate by a thin insulating layer on both sides of the channel. FinFETs with a thick oxide on top of the fin are called double-gate FinFETs. In total, it has a superb channel control and these are also offered approximately double the on-current compared to the MOSFETs, because of the dual gates, yet without rising channel doping. This is one of the major advantages, providing carrier mobility and results in a low gate leakage simultaneously. All drawbacks should be overcome by the implementation of these types of FinFET devices and also it is suitable for exploring nano scale device technologies. To design a low power, efficient complex circuit, it is more flexible and easy to use FinFETs with independent gates (D. Bhattacharya et al, 2014). Fig.1.3 shows the top view and the symbol of the double gate FinFET structure. FinFET provide lesser flicker noise and higher drive currents at low supply voltages (V_{dd}) and it is suitable for analog and digital applications (H. Lui et al, 2013).

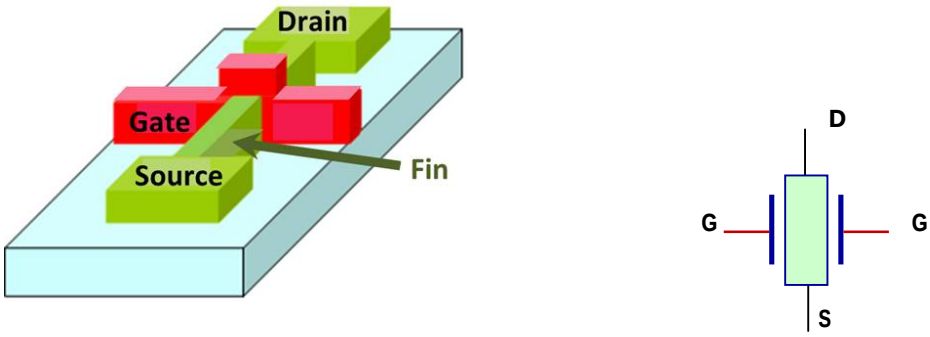


Fig.1.3 Double gate FinFET Structure: Top view and its symbol (D. Bhattacharya et al, 2014)

1.6 CNTFET Transistor

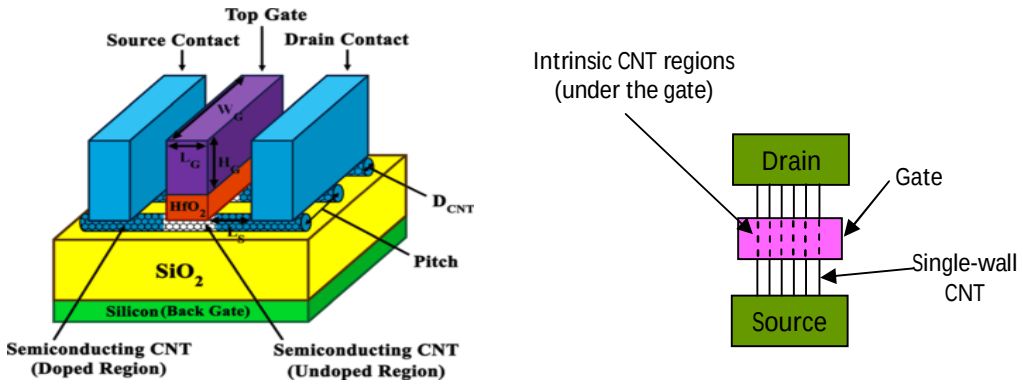
By the inevitable scaling down of the aspect ratios of the MOSFET more deeper in nano scale, the CMOS technology encounters many severely critical problems such as high leakage currents, short channel effects, high power density, large parametric variations and reduced gate control and decrease its suitability in the near future very low power, high speed, more functioning and high packing density applications. Some devices beyond CMOS devices such as carbon nanotube field effect transistor (CNTFET) (M.H. Moaiyeri et al, 2013), quantum-dot cellular automata (Y.B.Kim et al, 2010) and single electron technology (Y.B. Kim et al, 2010) brought out to overcome the above said problems. These nano devices benefit from ballistic transport attributes under low supply voltages, low power consumption and very small sizes

that make them very suitable for ultra high performance, ultra low power and ultra high density chip design. However, by getting into consideration of these nanotechnologies, CNTFET can be more desirable because of its equivalence to MOSFET in respect of its inherent electronic characteristics. CNTFET typically has the benefit of a very high carrier velocity, much higher performance operation, higher transconductance and lower power consumption in contrast with the MOS transistors.

A thin sheet of graphite is rolled to form Carbon nanotubes (CNTs). These CNTs can be categorized into (i) single-walled CNTs (SWCNTs) (ii) multi-walled CNTs (MWCNTs). SWCNTs consist a single cylinder and MWCNTs consist more than one cylinder. The chiral number of a CNT is (n,m), is also called as a chirality vector of the CNT. If (n–m) is not the integer multiples of 3 then the SWCNT acts as a semiconductor, otherwise it acts as a conductor (M.H.Moaiyeri et al, 2013). Semiconductor single wall CNTs can be applied as the channel of the CNTFET device. Moreover, P and N-type CNTFETs have the same mobility and as a result, same drive currents, unlike the MOSFET devices. This exclusive attribute of the CNTFET device is extremely momentous for unscrambling the sizing and design procedures of CNTFET-based complex circuits. The other big advantage of the CNTFET is providing equivalent I-V characteristics of well-tempered MOSFET devices. Fig.1.4 shows the schematic diagram of CNTFET. Similar to the traditional silicon device, the CNTFET also has four terminals. As shown in Fig.1.4, undoped semiconducting nanotubes are placed under the gate as channel region, while heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance in the ON-state. As the gate potential increases, the device is electrostatically turned ON or OFF via the gate.

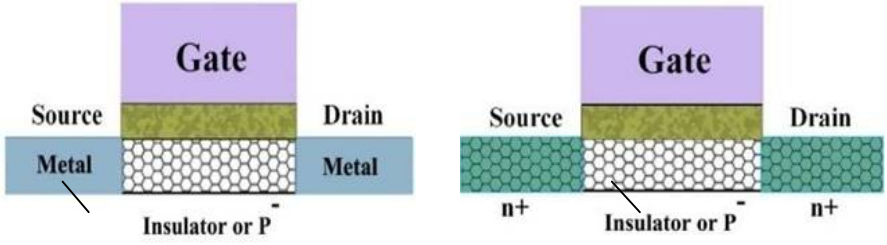
The working principle of CNTFET is similar to that of the conventional silicon device. This three or four terminal device comprises of a semiconducting nanotube, acting as conducting channel, bridging the source and drain contacts. The device is turned ON or OFF electrostatically via the gate. According to the mechanism of device operation, CNTFET can be categorized as two ways: Schottky Barrier (SB) CNTFET (SB-CNTFET) (Fig1.5(a)) and MOSFET-like FET (Fig1.5(b)) (M.H. Moaiyeri et al, 2013). The conductivity of SB-CNTFET is governed by the majority carriers tunneling through the Schottky Barriers at the end contacts. The ON-current and thereby device performance of the SB-CNTFET is determined by the contact

resistance due to the presence of tunneling barriers at both or one of the source and drain contacts.



(a) Cross sectional view (b) Top view

Fig.1.4 Schematic diagram of a CNTFET device (M.H. Moaiyeri et al, 2013)



(a) (b)

Fig.1.5 (a)SB-CNTFET (b) MOS-CNTFET (M.H. Moaiyeri et al, 2013)

The Schottky Barriers at source/drain contacts are due to the Fermi-level alignment at the metal-semiconductor interface. Both the height and the width of the SBs, and therefore the conductivity, are modulated by the gate electrostatically. SB-CNTFET shows the ambipolar transport behavior. So both the device polarity (n-type FET or p-type FET) and the device bias point can be adjusted by choosing the appropriate work function of source/drain contacts. On the other hand, MOSFET like CNTFET exhibits unipolar behavior by suppressing either electron (pFET) or hole (nFET) transport with heavily doped source/drain. The non-tunneling potential barrier in the channel region, and there by the conductivity, is modulated by the gate-source bias.

1.7 Motivation of the Present Work

One of the important issues in electronic circuits like memories is soft errors and multiple numbers of different techniques are used to reduce their effects. One of the extensively used techniques is error correction code (ECC) to secure memories from soft errors. These ECCs influence the propagation delay, area, and power consumption of the circuit. The extra encoding and decoding delays are added in the circuit since data need to be encoded while writing into the memory and decoded while reading

from it. The effect on delay, area and power occurs from the circuits of encoder and decoder and also from the extra check bits that the ECC appends to each block of data. Most commonly used ECCs is, a Single error correction (SEC) codes to protect memories because of simple encoding and decoding circuitry and less number of extra check bits. SEC codes can correct single bit error and detect double bit errors per block. These codes are used for both correction and detection in memory protection. So these SEC codes are called as SEC-DED (Single error correction - double error detection) codes.

Most crucial aspects of these circuits are reducing the delays of encoding and decoding logics. A low encoding and decoding delay SEC and/or SEC-DED code is proposed (P.Reviriego et al, 2013). This code can be used to protect memory for any data block size with low delay and less area. Low delay SEC-DED code encoder and decoder block diagrams are shown in Fig.1.6.

It contains an array of XOR gates, which are connected as cascading of two input XOR gates. Because of cascading, stage delay is added in that encoder and decoder so that resultant delay will be increased. So to avoid that cascaded stage delay, a direct single circuit can be used. So in this thesis different structures of two input, three input and a direct structure for different multi input XOR/XNOR logic circuit, self checking XOR/XNOR, sub threshold operated XOR/XNOR circuits are proposed that results low delay SEC-DED hamming code having much more less delay with reduced number of transistors. Another advantage of the use of the proposed circuits is differential hamming outputs are available at the same time, so that it is useful for self-checking of circuit working itself. So that it makes ECC more efficient.

Along with these ECC codes, XOR/XNOR gates are important components in applications such as adders, multipliers, MACs, parity generators, error detection and correction coders, digital signal processors (DSP) architectures and microprocessors etc. In most of these systems XOR/XNOR circuits in the critical path that affects the overall speed of the system. So enhancing the performance of the XOR/XNOR cell is a significant goal. The efficiency of the XOR/XNOR gate determines the efficiency of the systems. Various structures have evolved trying to improve the performance of the XOR/XNOR cells in terms of area, power and speed. Low power design with high speed of operation, fault secure and less area are more essential for designing of XOR/XNOR circuits. And other applications of XOR/XNOR gates are given in Fig.1.7.

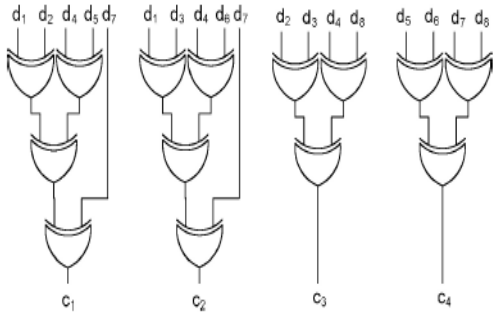


Fig.1.6(a)Low Delay SEC-DED Hamming Encoder (P.Reviriego et al, 2013)

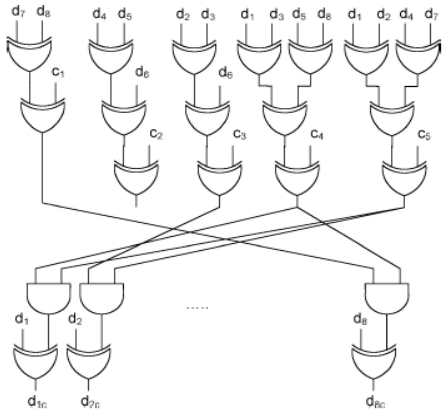
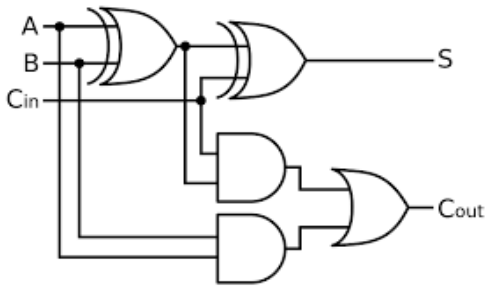
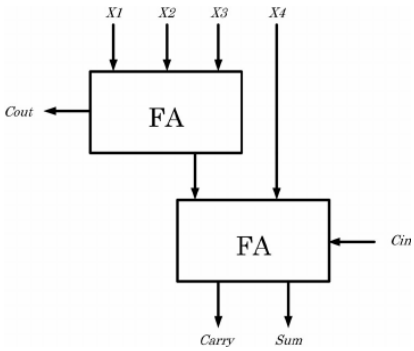


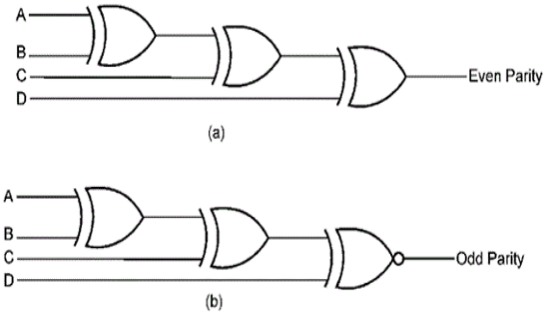
Fig.1.6(b) Low Delay SEC-DED Hamming Decoder (P.Reviriego et al, 2013)



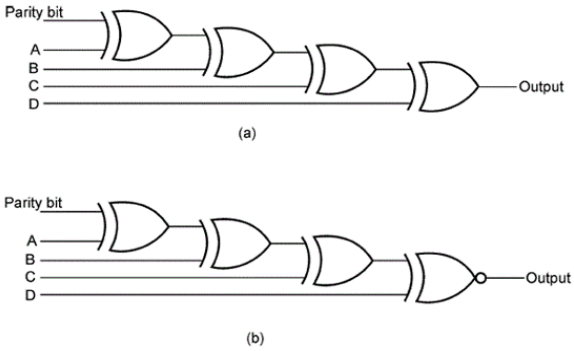
(i) Full Adder



(ii) Compressor



(iii)Even and Odd parity generator



(iv)Even and Odd parity checker

Fig.1.7 Applications of XOR and XNOR gates (S.C. Yuan et al, 2007, R.F. Mirzaee et al, 2010, K. Navi et al, 2008a, K. Navi et al, 2008b, K. Navi et al, 2009, J.M. Rabaey et al, 2003, M. M. Mano, 1979)

1.8 Objectives and Scope of the Present Work

With the ever growing demand for portable applications like mobile phones, laptops, palmtops etc. designers striving for the smaller silicon area, high speed, less power dissipation, longer battery life, more reliability. The XOR/XNOR is the basic building block of various error controlling coders and many arithmetic circuits like adders, multipliers, comparators, parity generator/checkers and code converters etc.

So the objectives of the present work are designing new XOR/XNOR gates with

- Rail to Rail Swing
- High Performance/low power
- Better Power Delay Product (PDP)
- More Reliability
- At low voltages
- Less number of transistors

By combining the above said objectives, those are grouped into four different categories of objectives. Those are:

- full rail to rail swing, high performance and better power delay product XOR/XNOR circuits.
- fault secure, full rail to rail swing, high performance and better power delay product XOR/XNOR circuits.
- low voltage, low power, full rail to rail swing and better power delay product XOR/XNOR circuits.
- Multi-valued logic, full rail to rail swing and better power delay product XOR/XNOR circuits.

1.9 Description of the Research Work

In the part of this thesis, the work done is

- full rail to rail swing, high performance and better power delay product XOR/XNOR circuits:
    - (i) Two input differential XOR/XNOR circuits
    - (ii) Three input differential XOR/XNOR circuits
    - (iii) Four input and eight input differential XOR/XNOR circuits
    - (iv) General structure for Multi input (‘n’ input, where n>3) differential XOR/XNOR cells
    - (v) Direct Three input XOR circuits

(vi) Two input XOR and XNOR circuits

- fault secure, full rail to rail swing, high performance and better power delay product XOR/XNOR circuit:
  (i) Self-checking XOR/XNOR circuits
- low voltage, low power, full rail to rail swing and better power delay product XOR/XNOR circuits:
  (i) Sub-threshold voltage operated DCVSL XOR/XNOR Circuits.
- multi valued logic, full rail to rail swing and better power delay product XOR/XNOR circuits:
  (i) Ternary XOR/XNOR circuits

1.10 Organization of Thesis

The thesis organization is structured as follows:

Chapter 2 consists of existed two input, direct three input, two input differential, self checking XOR logic designs. In this chapter all these logic structures of different exclusive OR and exclusive NOR cells are studied, analyzed and compared.

Chapter 3 presents the proposed two input differential, three input differential, four input and eight input differential, multi input differential XOR/XNOR structure, two input XNOR cells and direct three input XOR logic circuits, self checking XOR logic designs, sub-threshold operated circuits and ternary XOR and XNOR logic gates. This chapter begins with the proposed design structures, then operations and truthtables have been discussed.

Chapter 4 presents the mathematical analysis of proposed two input differential, three input differential, multi input differential XOR/XNOR structure, two input XNOR cells and direct three input XOR logic circuits, self-checking XOR logic designs, sub-threshold operated circuits and ternary XOR and XNOR logic gates. This chapter begins with the transistor aspect ratios analysis, full swing analysis, power and delay analyses then Monte Carlo noise analysis of the proposed designs have been discussed.

Chapter 5 presents the simulation results, comparison of the proposed designs with the existing designs in various terms and a conclusion has been drawn.

Chapter 6 presents conclusions and future scope. Finally, references and list of publications/communication related to my work were added.