CHAPTER VI

CONCLUSION AND FUTURE SCOPE

In this thesis,

(i) Various two input and three input XOR and XNOR cells are reviewed from the past to the most recent published research work.

(ii) Proposed eight circuits of two new structures for two input XOR/XNOR circuits and compared with existing circuits with respect to parameters like propagation delay, power consumption and noise margin.

(iii) Proposed three circuits for three input differential XOR/XNOR circuits and compared with existing circuits with respect to all parameters.

(iv) Proposed four input differential XOR/XNOR circuit and compared with existing circuits with respect to all parameters.

(v) Proposed general structure for multi input XOR/XNOR circuits, where that structure can be used for minimum of fan-in four to any number.

(vi) Proposed three new direct three input XOR circuits and compared with existing circuits in terms of power and delay and concluded as proposed one is better than the others.

(vii) Proposed two new two input XNOR circuits and compared with existing circuits and discussed about advantages.

(viii) New Self-Checking XOR/XNOR circuits proposed for reliable circuits and discussed about all features.

(ix) Proposed two new structures for Sub threshold voltage operated DCVSL XOR/XNOR Circuits to work at low/ ultra-low voltages.

(x) Proposed twelve new Ternary XOR and XNOR circuits for multi-valued logic.

(xi) The comparison of XOR/XNOR cells with each other in terms of power, delay, number of transistors and power delay product is done.

Table 6.1 shows the summary of the proposed circuits including its objectives. Based on this work it can be concluded that depending on the application-requirement, one can choose the best amongst the circuits represented in all the above stated as they have different output swing levels, power dissipation, speed and number of inputs/outputs.

6.1 Conclusions

Chapter 1 constructs the introductory overview of the importance of XOR/XNOR gates in digital circuits and the designing of XOR/XNOR circuits in VLSI systems. The applications of XOR circuits are described. The evolution of FinFET and CNTFET transistors by overriding the challenges of MOSFET transistors is covered in this chapter.

In chapter 2, various 2-input and 3-input XOR and XNOR cells existed from the past to the most recent published research work are reviewed. The advantages and disadvantages of circuits are discussed. The problems from the existed circuits are identified.

In Chapter 3, all the proposed circuits are presented with four different categories of objectives. Under the objective of full rail to rail Swing, high performance and better PDP XOR/XNOR Circuits, two new two input XOR/XNOR structures, three new three input XOR/XNOR structures and a general structure for multi input with n (n>3) inputs, two XNOR circuits for two input and three direct three input XOR circuits are proposed, explained their operations and thus compared in terms of power, delay, number of transistors, noise margin and output logic swing. The proposed circuits have exhibited a full-swing voltage output in 90 nm CMOS process for low voltages with less delay and more noise margin. All proposed circuits have better driving capability with strong output signal in all input combinations, good performance and high noise margin especially in low supply voltage. Hence, these are proven the best alternative to low-power and low-voltage applications with requirement of small size, high speed, high noise margin and better power delay product.

The proposed self checking XOR/XNOR circuit with the objectives of fault secure, self testing, totally self testing and code disjoint properties are explained in this chapter. This design is simple and symmetrical. The static logic is used to derive the structure. The proposed circuit has displayed the fault secure and self-testing properties. Hence, it is called as a totally self-checking circuit. This circuit possesses less delay since it has minimum number of two transistors in its critical path. The output swings of both outputs are strong. The simulation results have displayed that the proposed design takes less delay as well as power consumption with satisfying totally self-checking property.

Then sub threshold operated circuits are presented with the objectives of low voltage and low power operation. In the proposed structures voltage boosting blocks are used.

These are acting as negative voltage generators. It generates a negative voltage approximately equal to the applied V_{dd} thus providing the required gate-source voltage to the transistors in the logic gate to make them to conduct at voltages lower than their

Table 6.1 Summary of the proposed circuits

S.No	Proposed Circuits	Technology Used	No. of proposed structures	Objectives
1	Two input Differential XOR/XNOR	Both MOSFET and FinFET versions	2	Rail to Rail Swing, High Performance, Less number of transistors, better PDP
2	Three input Differential XOR/XNOR		3	
3	Multi input XOR/XNOR		1	
4	Direct three input XOR/XNOR		3	
5	Two input XNOR		2	
6	Self Checking XOR/XNOR		1	Fault secure, self testing, code disjoint, more reliable, Rail to Rail Swing, High Performance, Less number of transistors, better PDP
7	Subthreshold voltage operated DCVSL XOR/XNOR		2	low voltages, low power , Sub-threshold voltage operation, Rail to Rail Swing, better PDP
8	Ternary XOR and XNOR	CNTFET version	12	Multi Valued Logic, low power, Rail to Rail Swing, better PDP

threshold voltage. And finally, ternary XOR and XNOR circuits with static and pseudo logics, their operations are described. To overcome the challenges of binary logic this three valued logic Ternary is used. To design ternary logic circuits, multi

threshold devices are required. Having multi threshold CNTFET is easier and more effective than MOSFET or FinFET, these ternary circuits are designed with CNTFET devices. My contribution in this work is design of the circuit structures and analysis of threshold voltages calculation to get outputs according to their function.

In Chapter 4, the mathematical analysis for rail to rail analysis of the proposed pass transistor logic based circuits is explained for all input combinations. Then, the aspect ratio calculation of transistor is given followed by propagation delay, power consumption and Monte carlo noise analyses discussions. For self checking circuits the Stuck-at, Stuck-ON and Stuck-OPEN faults are analyzed. For ternary circuits the chiralities are decided based on the requirement of threshold voltage.

In Chapter 5, the simulation results for newly proposed circuits are given. All the circuits are simulated with various technologies of Cadence Spectre180nm, 90nm CMOS technology, 20nm FinFET technology and 32nm CNTFET technology. Transient results, propagation delay, power dissipation and noise analysis of all the proposed circuits are given and compared with all conventional circuits. Based on these simulation results it can be concluded that depending on the application requirement one can choose the better amongst the circuits represented in all above stated as they have different output swing levels, power dissipation, speed and number of inputs/outputs. An application of SEC-DED Hamming code is implemented with all proposed circuits and existing circuits. The SEC-DED Hamming code with proposed circuits has given better results in terms of delay, power, PDP, noise margin and number of transistors.

6.2 Scope for Future Work

Further work can be done by implementing the other error detection and correction codes like Reed solman and Goley codes with proposed circuits to get high performance, low power and fault secure codes. The proposed circuits can be extended to work at ultra low voltages by using TFET and HTFET. This work can be extended to get fault tolerant systems of reliable communications. Faster and reliable arithmetic circuits like adders, multipliers, MAC and ALU can be implemented with proposed circuits. A library model for XOR/XNOR circuit can be made.