

REFERENCES

- A. Beg, A. Beg, and A. Elchouemi, "XOR gates for low-energy and near- V_{th} operation" IEEE International Conference on Electronics, Circuits, and Systems (ICECS), (2015), 49-52.
- A. De and S. Ghosh, "Threshold voltage defined multi-input complex gates" IEEE International Symposium on Hardware Oriented Security and Trust (HOST), (2017), 164 – 164.
- A. K. Pandey, R.A.Mishra and R.K.Nagaria, "Leakage Power Analysis of Domino XOR Gate," ISRN Electronics, (2013), 1, 1-7.
- A. K. Pandey, R.A.Mishra and R.K.Nagaria, "Performance Analysis of NOVEL Domino XNOR Gate in Sub 45nm CMOS Technology," WSEAS Transactions on Circuits and Systems, (2013), 12 (2), 48-56.
- A. K. Nishad and R. Chandel, "Analysis of Low Power High Performance XOR Gate Using GDI Technique" International Conference on Computational Intelligence and Communication Networks, India, (2011), 187-191.
- A. M. Shams, T. K. Darwish and M. A. Bayoumi: "Performance analysis of low power 1-bit CMOS full adder cells," IEEE Transactions on VLSI systems, (2002), 10 (1), 20-29.
- A. P.Chandrakasan, S. Sheng and R.W. Brodersen, "Low power CMOS Digital Design," IEEE Journal of Solid State Circuits, (1992), 27 (4), 473-484.
- A. Raychowdhury, K. Roy, "Carbon-nanotube-based voltage-mode multiple-valued logic design," IEEE Trans. Nanotechnol., (2005), 4 (2), 168–179.
- A. Srinivasulu, "Modified Optical OR and AND Gates," journal of Semiconductor Physics, quantum electronics and Optoelectronics, (2002), 5 (4), 428-430.
- A. Srinivasulu and K. Sivadasan, "Optical Exclusive-OR Gate", Journal of Microwaves, Optoelectronics and Electromagnetic Applications, (2003), 3 (1), 20-25.
- A. Srinivasulu and M. Rajesh, "ULPD and CPTL pull-up stages for differential cascode voltage switch logic," Journal of Engineering, (2013), 1-5.

- A. Srinivasulu and K.B. Kebede, "Optical Co-Incidence Gate," *African Journal of Science and Technology*, (2002), 3 (2), 114-117.
- A. Wang and A. Chandrakasan, "A 180 mV FFT processor using sub-threshold circuit techniques," in *Proc. IEEE ISSCC*, (2004), 292-295.
- B. Hamdi, K. Chiraz and T. Rached, "Pass Transistor Based Self-Checking Full Adder," *International Journal of Computer Theory and Engineering*, (2011a), 3(5).
- B. Hamdi, K. Chiraz, F. Aymen and T. Rached, "Four Transistors Self-Checking Differential XOR," *International Symposium on signals, circuits and systems*, (2011b).
- B. Hamdi, K. Chiraz and T. Rached, "A novel differential XOR-based self checking Adder," *International Journal of Electronics*, (2012), 99(9), 1239-1261.
- B. Hamdi, T. Rached and F. Aymen, "Mixed CMOS/PTL Logic Style Design for Fast Self-Checking Adders," *International Journal of Advancements in Computing Technology (IJACT)*, (2014), 6(2).
- C. Piguet, J.-M. Masgonty, S. Cserveny, and E. Dijkstra, "Low power low-voltage digital CMOS cell design," in *Proc. PATMOS'94*, Barcelona, Spain, (1994), 132-139.
- C. Yu, W.P. Wang and B.D. Liu, "A 3-input XOR/XNOR for Low-Voltage Low-Power Applications", in *proceedings of 2000 IEEE Asia-Pacific Conference on Circuits and Systems*,(2000), 505-508.
- D. A. Anderson and G. Metze, "Design of totally self checking check circuits for m-out-of-n codes," *IEEE Transactions on Computers*, (1973) 22 (3), 263-269.
- D. Bhattacharya and K. J. Niraj, "FinFETs: From Devices to Architectures", *Journal of Advances in Electronics*, (2014).
- D. Radhakrishnan, "Low voltage low power CMOS full adder," *IEEE Proc.-Circuits, Devices and Systems*, (2001), 148(1), 19-24.
- D. Wang, M. Yang, W. Cheng, X. Guan, Z. Zhu and Y. Yang, "Novel low power full adder cells in 180nm CMOS technology," *4th IEEE Conference on Industrial Electronics and Applications*, China, (2009), 430 - 433.
- E. Dubrova, "Multiple-valued logic in VLSI: challenges and opportunities," *Proc.*

- NORCHIP Conf., Oslo, Norway, (1999), 340–350.
- F. Aymen, H. Belgacem and K. Chiraz, “A New Efficient SelfChecking Hsiao SECDED Memory Error Correcting Code,” International Conference on Microelectronics, Hammamet, Tunisia, (2011), 1-5.
- G. E. P. Box and M.E.A Muller, “Note on the Generation of Random Normal Deviates”, The Annals of Mathematical Statistics, (1958), 29(2), 610-611.
- G. Cho, Y. Kim, F. Lombardi, M. Choi, “Performance evaluation of CNFET-based logic gates,” Proc. IEEE Int. Instrumentation and Measurement Technology Conf., Singapore, (2009), 909–912.
- H. E. Neil Weste and Kamran Eshraghian, “Principles of CMOS VLSI Design, A System Perspective, Pearson Edition Asia, 2nd Ed,” (2004), 304-305.
- H. Hung and V. Adzic, "Monte Carlo Simulation of Device Variations and Mismatch in Analog Integrated Circuits" Proceedings of the National Conference On Undergraduate Research (NCUR), The University of North Carolina at Asheville, (2006)
- H. Lui, S. Datta and V. Narayanan, “Steep switching tunnel FET: A promise to extend the energy efficient road map for post CMOS digital and analog/RF applications,” International Symposium on Low power electronics and design, (2013), 4-6.
- H. T. Bui, A. K. Al-Sheraidah and Y. Wang, “New 4-transistor XOR and XNOR designs,” Proceedings of Second IEEE Asia Pacific Conference on ASICs, South Korea ,(2000), 25 – 28.
- H. W. Kim and S. Lee, ‘Design and Implementation of a Private and Public Key Crypto Processor and its Application to a Security System’, *IEEE Transactions on Consumer Electronics*, (2004), 50(1), 214–224.
- I. J. Sanwo, M. B. Suthar, “3-input Exclusive-OR gate circuit “, patent no:US4749887 A, (1988).
- J. B. Kim, S.J. Hong and J. Kim, “New Circuits for XOR and XNOR functions,” International Journal of Electronics, (2010), 82 (2), 131-144.
- J. Deng and H. S. Philip Wong, “A Compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application – part i: model of

- the intrinsic channel region,” *IEEE Trans. Electron Devices*, (2007), 54 (12), 3186–3194.
- J. Deng and H. S. Philip Wong, “A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application – part ii: full device model and circuit performance benchmarking,” *IEEE Trans. Electron Devices*, (2007), 54 (12), 3195–3205.
- J. H. Lou and J. B. Kuo, “A 1.5V full-swing bootstrapped CMOS capacitive-load driver circuit suitable for low-voltage CMOS VLSI,” *IEEE J. Solid-State Circuits*, (1997), 32 (1), 119-121.
- J. H. Lou and J. B. Kuo, “A 1.5V CMOS all-N-logic true-single-phase bootstrapped dynamic-logic circuit suitable for low supply voltage and high-speed pipelined system operation,” *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, (1999), 46 (5), 628-631.
- J. M. Wang and S.C Fang, “New Efficient Designs for XOR and XNOR Functions on the Transistor Level,” *IEEE Journal of Solid-State Circuits*, (1994), 29 (7), 780-786.
- J. M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital Integrated Circuits: A Design Perspective, 2nd Edition, Prentice Hall India”, (2003).
- J. W. Kim, J.S. Kim and B.S. Kong, “Low voltage CMOS differential logic style with supply voltage approaching device threshold voltage”, *IEEE Transactions on Circuits and Systems*,(2012), 59(3), 173-177.
- J. W. Kim and B. S. Kong, “Low-voltage bootstrapped CMOS drivers with efficient bootstrapping,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, (2008), 55 (6), 556-560.
- J. U. Shin, L.Y. Kwong and G. Shrivastav, “High-speed static XOR circuit “, patent no: US 8324932 B2, (2012).
- K. Hedayati, “Reduced parallel EXCLUSIVE or and EXCLUSIVE NOR gate”, patent no:US4749886 A, (1988).
- K. Navi, O. Kavehei, M. Rouholamini, A. Sahafi, S. Mehrabi, and N. Dadkhahi, “Low-Power and High-Performance 1-Bit CMOS Full-Adder Cell”, *Journal of Computers*, (2008a), (3), 48–54.

- K. Navi, R. F. Mirzaee, M.H. Moaiyeri, B. Mazloom Nezhad, O. Hashemipour, and K. Shams, "Ultra High Speed Full Adders", *IEICE Electronics Express*, (2008b), 5, 744–749.
- K. Navi, M.H. Moaiyeri, R.F. Mirzaee, O. Hashemipour, and B. M. Nezhad, "Two Novel Low-Power Full Adders based on Majority-Not Gates", *Elsevier, Microelectronics Journal*, (2009), (40), 126–130.
- K. H. Cheng and V. C. Hsieh, "High Efficient 3-input XOR for Low-Voltage Low-Power High-Speed Applications," *AP -ASIC '99, IEEE*, (1999), 166-169.
- K. M. Chu and D. L. Pulfrey, "A comparison of CMOS circuit techniques: Differential Cascode Voltage Switch Logic Versus Conventional Logic", *IEEE J. Solid-State Circuits*,(1987), 22(4), 528 - 532.
- K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," *IEEE Journal of Solid-State Circuits* , (1986), 21(6),1057–1066.
- K. R. Kumar, P. M. Reddy, M. Sadanandam, A. S. Kumar and M. Raju, "Design of 2T XOR gate based full adder using GDI technique," *International Conference on Innovative Mechanisms for Industry Applications (ICIMIA)*, Bangalore, India, (2017), 10-13.
- L. G. Heller, W. Griffin, J. Davis, and N. Thoma, "Cascode voltage switch logic: A differential CMOS logic family," in *Proc. IEEE ISSCC Dig. Tech papers*, (1984), 16-17.
- M. Uya, "Complementary channel type MOS transistor exclusive OR/NOR logic gate circuit", patent no:US4417161 A, (1983).
- M. A. Akbar and J.A. Lee, "Self-Checking Carry Select Adder with Fault Localization ," *Euromicro Conference on Digital System Design*, (2013), 863-869.
- M. A. Akbar and J.A. Lee, "Self-Checking Carry-Select Adder Design Based on Two-Rail Encoding," *IEEE Transactions on Circuits and Systems I: Regular Papers*, (2014), 61(7), 2212-2214.
- M. A. Elgamel, S. Goel, and M. A. Bayoumi: "Noise tolerant low voltage XOR-XNOR for fast arithmetic," *Great Lake Sym. VLSI*, Washington DC, (2003), 285-288.

- M. C. Parris, "Layout area efficient, high speed, dynamic multi-input exclusive or (XOR) and exclusive NOR (XNOR) logic gate circuit designs for integrated circuit devices", patent no:US7298171 B2, (2007).
- M. H. Moaiyeria, R. F. Mirzaee, K. Navi, T. Nikoubin and O. Kavehei, "Novel direct designs for 3-input XOR function for low power and high speed applications," *International Journal Electronics*, (2010), 647-662.
- M. H. Moaiyeri, R.F. Mirzaee, A. Doostaregan, K. Navi and O. Hashemipour, "A universal method for designing low-power carbon nanotube FET-based multiple-valued logic circuits," *IET Computers & Digital Techniques*, (2013), 7(4), 167–181.
- M. H Moaiyeri, A. Doostaregan, K. Navi, , "Design of energy-efficient and robust ternary circuits for nanotechnology," *IET Circuits Devices Syst.*, (2011), 5 (4), 285–296.
- M. J. M. Pelgrom, A.C.J. Duinmaijer, A.P.G. Welbers, "Matching Properties of MOS Transistors," *IEEE Journal of Solid-State Circuits*, (1989), 24(5), 1433-1440.
- M. M. Mano, "Digital logic and Computer Design," 2nd edition, Prentice Hall India, (1979).
- M. S. Daliri, K. Navi, R. F. Mirzaee, S. S. Daliri and N. Bagherzadeh, "A new approach for designing compressors with new hardware-friendly mathematical method for multi-input XOR gates," *journal of IET Circuits, Devices & Systems*, (2017), 11(1), 46-57.
- N. Ahamd and R. Hasan, "Topology of 2 input sub- nano watt XOR gate in 65 nm CMOS technology," *Proc. IEEE International Conference on Semiconductor Electronics*, (2012), 597-599.
- N. Ahmad and R. Hasan, "A 0.8V 0.23nW 1.5nS Full Swing Pass Transistor XOR gate in 130nm CMOS," *Active and Passive Electronic Components*, (2013).
- N. Pandey, K. Gupta, G. Bhatia and B. Choudhary, "MOS current mode logic exclusive-OR gate using multi-threshold triple-tail cells," *Microelectronics Journal*, (2016), 57, 13-20.
- N. Ohkubo, M. Suzuki, T. Shinbo, T.Yamanaka, A. Shimizu, K. Sasaki, Y. Nakagome, "A 4.4 ns CMOS 54-b multiplier using pass-transistor

- multiplexer,” *IEEE J. Solid-State Circuits*, (1995), 30, 251–257.
- N. Yadav, S. Khandelwal and S. Akashe, “Design and analysis of FINFET pass transistor based XOR and XNOR circuits at 45 nm technology,” *International Conference on Control, Computing, Communication and Materials (ICCCCM)*, (2013), 1-5.
- N. Z. Haron and S. Hamdioui, "Why is CMOS scaling coming to an END?", 3rd International Design and Test Workshop, Tunisia,(2008)
- P. Couteaux, R. Marbot, “Exclusive-or logic gate with four two-by-two complementary inputs and two complementary outputs, and frequency multiplier incorporating said gate”, patent no: US6137309 A, (2000).
- P. Lee, C.H. Hsu, and Y.H. Hung, “Novel 10-T full adders realized by GDI structure,” in the proceedings of *IEEE International Symposium on Integrated Circuits (ISIC-2007)*, (2007), 115-118.
- P. Reviriego, S. Pontarelli, J. A. Maestro and M. Ottavi.”A Method To Construct Low Delay Single Error Correction Codes For Protecting Data Bits Only,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, (2013), 32 (3), 479-483.
- P. R. Kinget, “Device Mismatch and Tradeoffs in the Design of Analog Circuits,” *IEEE Journal of SolidState Circuits*, (1990), 40(6), 1212-1215.
- P. Srivastava, A. K. Dwivedi and A. Islam, “Power - and variability-aware design of FinFET-based XOR circuit at nanoscale regime,” *IEEE International Conference on Advanced Communications, Control and Computing Technologies*, Ramanthapuram, India, (2014), 440 – 444.
- R. Jacob Baker, Harry W. Li, David E. Boyce, “Circuit Design, Layout, and Simulation by –CMOS” Prentice-Hall of India Private Ltd. (2003).
- R. Kumar and V. K. Pandey, “A New 5-Transistor XOR-XNOR circuit based on the pass transistor logic,” *Proc. IEEE World Congress on Information and Communication Technologies*, (2011), 667 – 671.
- R. Zimmermann and W. Fichtner, “Low-Power Logic Styles: CMOS versus Pass-Transistor Logic,” *IEEE Journal of Solid-State Circuits* , (1997), 32 (7), 1079-1090.

- R. Zimmermann and R. Gupta, "Low-Power Logic Styles : CMOS vs CPL," Proceedings of the 22nd European Solid-State Circuits Conference, Switzerland, (1996), 112-115.
- R. F. Mirzaee, M. H. Moaiyeri, and K. Navi, "High Speed NP-CMOS and Multi-Output Dynamic Full Adder Cells", International Journal of Electrical, Computer and Systems Engineering, (2010), 4(4), 304–310.
- R. H. Krambeck, C. M. Lee and H. F. S. Law, "High-speed compact circuits with CMOS," IEEE J. Solid-State Circuits, (1982), 17 (3), 614-619.
- R. Rogenmoser, H. Kaeslin, and N. Felber, "The impact of transistor sizing on power efficiency in submicron CMOS circuits," in Proc. 22nd European Solid-State Circuits Conf., Neuchatel, Switzerland, (1996), 124–127.
- S. Bonsels, M. Padeffke, T. Werner, A. Woerner, "Topology for a n-way XOR/XNOR circuit", patent no: US 7557614 B1, (2009).
- S. Geol, M.E. Elgamel, M.A. Bayouni, and Y.Hanafy: "Design Methodologies for high-performance Noise-tolerant XOR-XNOR Circuits," IEEE Trans. Circuits and Sys. - I, (2006), 53(4).
- S. Goel, A. Kumar, M.A. Bayoumi, "Design of Robust, Energy-Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS Logic Style," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (2006), 14(12), 1309 - 1321.
- S. Goel, M.A. Elgamel and M.A. Bayoumi, "Novel design methodology for high-performance XOR-XNOR circuit design," 16th Symposium on Integrated Circuits and Systems Design, Brazil, (2003), 71-76.
- S. C. Fang, J.M. Wang and W. S. Fang, "A new direct design for 3 input XOR function on the transistor level," IEEE J. Solid State Circuits, (1996), 43(4), 343-348.
- S.C. Yuan, "4-2 Compressor of Fast Booth Multiplier for High-Speed RISC Processor", International Journal of Electronics, (2007), 94(9), 869–875.
- S. Lin, Y. B. Kim, and F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits," IEEE Transactions on Nanotechnology, (2011), 10(2), 217–225.

- S. L. Murotiya and A. Gupta, "Design of High Speed Ternary Full Adder and Three-Input XOR Circuits Using CNTFETs," 28th International Conference on VLSI Design, (2015), 292-297.
- S. Musala and B.R. Reddy, "Implementation of a Full Adder Circuit with New Full Swing Ex-OR/Ex-NOR Gate," Proc. IEEE Conference-Prime Asia, (2013), 29-33.
- S. R. Chowdhury, A. Banerjee, A. Roy and H. Saha, "A high Speed 8 Transistor Full Adder Design," International Journal of Electronics and Communication Engineering, (2008), 2 (10), 2240-2250.
- S. S. Mishra, S. Wairya, K. Nagaria and S. Tiwari, "New Design Methodologies for High Speed Low Power XOR-XNOR Circuits," World Academy of Science, Engineering and Technology, (2009), 196-202.
- S. S. Mishra, A.K. Kumar and R.K. Nagaria, "A comparative performance analysis of various CMOS design techniques for XOR and XNOR circuits," International Journal on emerging technologies, (2010), 1(1), 1-10.
- T. V. Rao and A. Sinivasulu, "Modified level restorers using current sink and current source inverter structures for BBL-PT full adder", Radio engineering, (2012), 21(4), 1279-1286.
- T. V. Rao and A. Sinivasulu, "16-BIT RCA Implementation Using Current Sink Restorer Structure," International Journal of Design, Analysis and Tools for Integrated Circuits and Systems, (2013), 4 (1), 9-14.
- T. Nagateja, T. V. Rao and A. Srinivasulu, "Low Voltage, High Speed FinFET Based 1-BIT BBL-PT Full Adders," in proc. IEEE International Conference on Communication and Signal Processing, India, (2015), 1247-1251.
- U. Ko, P. T. Balsara, and W. Lee: "Low-power design techniques for high-performance CMOS adders," IEEE Trans. Very Large Scale Integr. Syst., (1995), 327-333.
- V. Lavanya, S. S. Kumar and L. Bhagyarakshmi, "RF harvesting and its applications in low power devices," IEEE International Conference on Advanced Computing, Chennai, India, (2015).
- W. J. Ming, F. Sung-Chuan, and F. Wu-Shiung: "New efficient designs for XOR and

- XNOR functions on the transistor level,” IEEE Journal of Solid- State Circuits, (1994), 780-786.
- U. Ko, P. T. Balsara and W. Lee, “Low-power design techniques for high-performance CMOS adders,” IEEE Trans. Very Large Scale Integr. Syst., (1995), 3, 327-333.
- X. Lin, Y. Wang and M. Pedram, “Stack sizing analysis and optimization for FinFET logic cells and circuits operating in the sub/near-threshold regime,” in Proc. IEEE 15th International Symposium on Quality Electronic Design, (2014), 341-348.
- X. Zhang, C.I.H. Chen, and A. Chakravarthy, “Structure Design and Optimization of 2-D LFSR Based Multi Sequence Test Generator in Built-In Self-Test”, IEEE Transactions on Instrumentation and Measurement, (2008), 57(3), 651–663.
- Y. B. Kim, “Challenges for nanoscale MOSFETs and emerging nanoelectronics” Transactions on Electrical and Electronic Materials, (2010), 11(3), 93-105.
- Y. Tsujihashi, “Three-input exclusive NOR circuit”, patent no:US5936427 A, (1999).