CHAPTER VI

CONCLUSION AND FUTURE WORK

6.1 CONCLUSION

In Chapter 5 the hardware implementation of the efficient architecture for real-valued FFT with a modified complex multiplier was used. The standard multiplier incorporation and the other multipliers are replaced with the module of modified shift and add/subtract based on the Canonical Signed - Digit (CSD) on with the resource sharing scheme for efficient power and hardware reduction. The usage of additional operations can be reduced by the change of number system representation. The complete architecture is coded in Verilog HDL and synthesized and simulated using Xilinx ISE 14.1. The area report and RTL schematic are generated. The power report is generated by the XPower Analyzer. If the operating frequency is increased from minimum to maximum of its frequency in a dynamic and the total power steady increase was found. The proposed implementation in chapter 4 occupied 58.3% fewer slices and increased the operating frequency of 12.58%. The look-up table occupied with the proposed design is compared, and the path delay of our modified complex multiplier is compared with other existing architectures, the proposed architecture shows that less area and power reduction.

During the process of the communication process, the speech signals are usually affected by noises. For suppressing the noise signal that is combined with the speech signal Wiener filter is adapted. In noise suppression, the Weiner filter plays an important role and enhancement by estimating the relationship between the power spectrums of the speech signal noise affected and the noise signal. The chapter 5 deals with the denoising system based on the FPGA for speech signal enhancement in digital hearing aid using Wiener filter and Real-valued FFT/IFFT is proposed. The power consumption and hardware requirement of the system can be reduced by the proposed modified Wiener filter and the processor of Real-valued FFT/IFFT. Using the Given Rotation method the Matrix inversion and reduces the computational complexity of the system. The system of noise degradation was coded in Verilog, synthesized and simulated in Xilinx ISE 14.5 and efficient SNR values are obtained.
6.2 FUTURE WORK

To receive a better signal nowadays the researchers are more involved in the noise reduction in the speech signal and implementation in the real time to reduce the hardware complexity requirement and reduce delay.

The efficient hardware architecture for the algorithm of spectral subtraction can be applied to the enhancement of speech. In the applications of the audio de-noising, Spectral subtraction algorithm is widely used. The environmental noise from speech can be estimated adaptively. To make the noise free the samples of noise from the input speech are subtracted after the noise estimation. The noise estimation-subtraction block and the phase block can be used.

The parallel architecture for the computation of one-dimensional discrete Mellin transform (DMT) can be used in real-time hardware implementation. The DMT is a useful technique in recognition of pattern, speech processing, signal detection and image registration due to its property of scale invariant, in real time applications for the hardware implementation VLSI architecture of this transformation is better. For one-dimensional DMT is based on ROM and MAC (Multiply and Accumulator).

For most real-valued applications, the decimation-in-time (DIT) fast Fourier transforms (FFT) have a better advantage over the decimation-in-frequency (DIF) FFT, like processing of speech, image, video processing, and analysis of time-series. The output reordering is not necessary. The design can be register-based storage, which involves significantly less area at the cost of a little higher latency. The address generation for folded in-place DIT RFFT computation with register-based storage is challenging, at different locations both the operation of read and write can be performed in the same clock cycle.

For the discrete Fourier transform (DFT) computation of real-valued signals, two-parallel pipelined architecture of fast Fourier transform (FFT) can be used. For signal processing and the applications of wireless communication, the architectures are optimized with less number of registers. To avoid storing the redundant values the clock to registers is disabled and hence the registers storing those redundant values are removed.