CHAPTER 4

IMPROVEMENT OF SOLID-STATE CIRCUIT BREAKER OPERATION IN COMMUTATION CIRCUIT

4.1 INTRODUCTION

Power quality (PQ) has developed into a major important issue for electricity users at every level of usage (Benachaiba 2009). Measuring the PQ fluctuations, analysis of power disturbances characteristics and finding solutions for the PQ problems is resulted due to the increased interest for PQ. Any power problem that will cause deviations of different parameters like voltage, current or frequency and will result in collapse or incorrect operation of customer equipments can be described as a power quality problem (Paisan Boonchiam 2006). Most of the problems that engross, overvoltage, low voltages, sags, swells impulses, transients, surges and disruptions of voltages are the widespread focus of PQ surveys (Omar et al 2010). One of the PQ problems, challenging today’s power systems is the frequently occurring voltage sag (Woo-Cheol Lee 2007).

Voltage sag is defined by IEEE as a drop between 0.1 and 0.9 Pu in rms voltage or current at the power frequency ranging for various periods of 0.5 cycles to 1 min (Tarek I. El-Shennawy 2010). In low voltage distribution systems, short period increase in current ultimately causes voltage sags. In a very short interval of period, the voltage sag event will decrease the amplitude of the effective load voltage from 0.9 to 0.1 of the nominal load voltage (H. Nasiraghdam 2007). Some other distinctiveness of voltage sags like interval, sag deepness and early point on gesticulate is dissimilar for different voltage sag measures. In-phase, pre-fault and optimized energy are three types of
methods commonly employed to perform voltage sag compensation (Jazayeri 2009). Some financial losses may also occur due to severe voltage sags if the equipment gets tripped and halts the process (Patne Nita.R 2008)

Depending on the different causes, the voltage sags that occur are either symmetrical or unsymmetrical. The sag is understood to be regular, if all the period voltages are equal and the phase rapport is 120. If not, the sag is thought to be unsymmetrical (Luis Guasch et al 2004). The current peaks produced by unsymmetrical voltage sags are high as those produced by symmetrical voltage sags. (i) Traditional Solutions (ii) Uninterruptible Power Supplies (UPS) (iii) Electronic Voltage Regulator are the three different types of voltage sag reducing devices. Voltage sags can be due to remote defects, alterations in loading conditions and charging of capacitor or transformer can create voltage sags. Since of the fact that voltage sags can make worse perceptive components similar to motor drives, computers, programmable logic controller etc., it is considered as a serious problem. Starting large loads and remote fault clearing done by utility equipment are the common causes of sags (Deswal 2008).

### 4.1.1 Thyristor Commutation techniques

Line commutation: The process of opening, or turning-off, a conducting thyristor is called commutation. In a line commutated converter circuit where the input voltage is alternating. A overturn voltage appears crosswise the thyristor straight away after the onward current go from side to side the zero value. This reverse voltage accelerates the turn-off process, by sweeping out the excess carriers from pn-junction $J_1$ and $J_3$. 
Turn-off time in $t_q$ is the minimum value of time interval between the instant value when the on-state current has decreased to zero and the instantaneous value when the thyristor is capable of withstanding forward conducting voltage without turning on. $t_q$ depends on the certain peak value of on-state current value and the instantaneous on-state current value and the instantaneous on-state voltage value.

Reverse recovered charge $Q_{rr}$ is the amount of charge that has to be recovered during only the turn-off process. Its price is determined from the over area enclosed by path of the reverse recovery current. The value of $Q_{rr}$ depends on the rate rise of fall of on-state current with the peak value of on-state current before turn-off. $Q_{rr}$ causes equivalent energy loss within the device.

Forced commutation: In forced commutation, exterior elements $L$ and $C$ which do not carry the load instantaneous current continuously, are used to turn-off a conducting thyristor. It may be recall that a conducting thyristor can be turned off by dropping its anode current decrease the holding current value and then applying a reverse voltage magnitude across the device to enable it to recover its forward blocking capability. There are more than a few technique of turning-off of a thyristor. All these methods be different from one to an additional in the mode in which commutation is achieved. Forced commutation can be attain in the following two ways:

Voltage commutation: In this method, a conducting thyristor is commutated by the application of a gate pulse of large reverse voltage. This reverse voltage is usually functional by switching a before charged capacitor. The sudden application of reverse voltage across the conducting thyristor reduces the anode current to zero rapidly. Then the being there of reverse voltage across the SCR help in the completion of its turn-off process.
Current commutation: In this scheme, an external pulse of current greater than the load current is passed in the reversed direction through the conducting SCR. When the current pulse attains a value equal to the load current, net pulse current through thyristor becomes zero and the device is turn-off. The current pulse is usually generated an initially charged capacitor.

An important feature of current commutation is the connection of diode in anti-parallel with the main thyristors so that voltages drop across the diode reverse biases the main SCR. Since this voltage drop is of the order of 1 volt, the commutation time in current commutation is more as compared to that in voltage commutation.

In both voltage and current commutation schemes, commutation is initiated by gating an auxiliary SCR.

The fault clearing performance of the capacitor based commutation circuit takes more time. Because, the discharging time of the capacitor is high it will increase the fault duration. If the fault duration is increased it will affect the fault clearing performance of SCB. To avoid this problem, in this paper a modified commutation circuit based SCB is proposed. In the proposed commutation circuit, a digital switch circuit is added instead of commutation capacitor. The details of the formulated problem and proposed methodology are described 4.2.

4.2 PROBLEM FORMULATION IN SCB

In SCB application, the nonlinear load supply quality is improved during nonlinear voltage distortion. In the voltage distortion time, the natural line goes to break down and the varistor connected local line goes to break up. In the breaking operation, the voltage of both power grids is collapsed for insufficient circuit facility. This voltage collapse problems cause power
interruption in the circuit. In (Christoph Meyer 2006), the voltage collapse was avoided by SCB based thyristor commutation circuit. The commutation circuit consists of auxiliary thyristor and commutation capacitor. One main problem that occurs in commutation circuit is the discharging time of the commutation capacitor is high. So, the SCB performance is affected and the time taken to solve this problem is high. Hence, to improve the performance of SCB, a modified commutation circuit based SCB will be proposed in the work.

4.2.1 Proposed Different Topologies for Active Current Limitation

The proposed commutation circuit will consist of digital switch and current comparator with the commutation capacitor. Then using the current comparator, the fault current will be calculated by comparing with normal current. When the time of fault occurs, the fault current will be reduced by opening the digital switch. If the digital switch is opened, then an open circuit will be formed in the commutation circuit and it will take less time to make an open circuit when compared with the performance of capacitor-enabled SCB.
Figure 4.1 Basic single phase forced commutation circuit

The different topologies of the forced commutation circuits are used to limit the active current that equal to zero. Then only the varistor circuit breaker is enabled to limit the distortion voltage. Here, the varistor is needed to prevent the voltage exceeding the breakdown voltage of the device. The different topologies are existed in and the existed topologies are topology, topology B and topology C. Figure 4.1 shows the basic single phase SCB commutation circuit with solid-state circuit breaker. The different topologies are modified by adding proposed circuit with commutation capacitor. The different topologies of the proposed commutation circuit based SCB are described in the following section.

4.3 TOPOLOGY A WITH DIGITAL SWITCH AND COMPARATOR

The proposed force commutation circuit of the topology A is described in Figure 4.2. (a,b)In the proposed SCB commutation circuit, during the normal operation time the current flows through the main thyristor. If a fault occurs, then the auxiliary thyristor of the current carrying main thyristor is fired. Thus, the fault current commutates instantaneously to the auxiliary pathway and reach one input of the current comparator. The other input of the current comparator is reference current. Then these two inputs are compared and the change of current is calculated. If the change of current is greater than zero, then utilize digital switch, make the open circuit and the limit the change of current. In this way, the proposed force commutation circuit is operated and the varistor has limited the voltage distortion. The diagram of the proposed digital switch based force commutation circuit is shown.
Figure 4.2 (a) Topology A with Digital switch and Comparator Circuit

Figure 4.2 (b) Single phase equivalent circuit for Topology A

The Figure 4.3 shows the circuit diagram of current comparator and digital switch used in the proposed force commutation circuit. The voltage across the digital switch, reference current, fault current and change of current are denoted as $V(t), I_R, I_F$ and $\Delta I$ respectively. The change of current is the
difference between the reference current and fault current. The digital switch state is changed based on the change of current values. The operating time of the digital switch is very less when compared to the commutation capacitor.

\[ V_{\text{switch}} = V_G \left( 1 - \cos \left( \frac{t_{\text{hold}}}{\sqrt{L_{\text{total}}}} \right) \right) + \left( I_G \cdot L_{\text{total}} + V_G \right) \cdot \sin \left( \frac{t_{\text{hold}}}{\sqrt{L_{\text{total}}}} \right) \]  (4.1)

where, \( V_{\text{switch}} \) is the voltage across the digital switch,

\( V_G \) is the grid voltage,

\( t_{\text{hold}} \) is the hold off time,

\( L_{\text{total}} \) is the sum of the inductance of the circuit.

The turn off process of the commutation circuit is calculated as a function of voltage across the digital switch. The turn off process is derived as follow.
\[ L_{\text{total}} + \frac{d^2 V(t)_{\text{switch}}}{dt^2} + V(t)_{\text{switch}} + V_G = 0 \]  

(4.2)

4.3.1 Topology B with Digital Switch and Comparator

The force commutation circuit of the topology B is described in Figure 4.4 (a,b). The difference in this commutation circuit is that an extra thyristor bridge circuit is added to reduce one digital switch. The operation of the thyristor bridge based force commutation circuit is the same as the standard force commutation circuit. The voltage across the varistor is determined by using the following formula

\[ V_{\text{Var}} = V_{ph} - V_{\text{Charge}} \]  

(4.3)

where,  

- \( V_{\text{Var}} \) is the voltage across the varistor,
- \( V_{ph} \) is the phase voltage,
- \( V_{\text{Charge}} \) is the varistor charging voltage.

Figure 4.4 (a) Topology B with Digital switch and Comparator Circuit
Figure 4.4 (b) Single phase equivalent circuit for Topology B

The force commutation circuit of the topology C is described in Figure 4.5. (a,b) In this commutation circuit, an extra gate commutated turn-off thyristor (GCT) bridge and commutating pulse transformer are added. The GCT is a high power semiconductor device used for turn off the commutation circuit. In normal operation the on state behavior of GCT is no relevance so the GCT is operated under in symmetric. The inductance rating of the commutating pulse transformer is very low that is integrated with digital switch thyristor circuit. In commutating pulse transformer, the voltage at the primary winding is responsible for the commutation time of the current to the auxiliary path. The fast commutation time is allowing a fast turn-off of the main thyristor, but it also increases the required hold-off time significantly due to reverse recovery effects. The complete commutation time is determined by using the following formula
\[ t_c = t_0 F\left(\frac{di}{dt}\right) + \left(\frac{dt}{di}\right) I_{\text{max}} \]  

(4.4)

where \( t_c \) is the complete commutation time,

\( t_0 \) is the initial commutation time,

\( F\left(\frac{di}{dt}\right) \) is the slew rate function,

\( I_{\text{max}} \) is the maximum commutation current.

### 4.3.2 Topology C with GCT and Digital Switch Comparator

In topology C, during normal operation the current flows through the thyristor and the inductance. If any failure is detected in the system, then the auxiliary circuits (GCT and thyristors) are fired. The current comparator compares the reference current and fault current; then depending on the change of current, the digital switch is operated. The digital switch limits the duration of fault current when compared with the commutation capacitor. The leakage inductance value is used to avoid the positive voltage of the commutation circuit. The positive voltage is caused by the on-state voltage of the GCT across the thyristors during the hold-off time.
Figure 4.5 (a) Topology C with Digital Switch and Comparator Circuit
4.4 RESULTS AND DISCUSSION

The proposed digital switch aided commutation circuit based SCB was implemented in MATLAB simulation platform. The output performance of the proposed commutation circuit based SCB was compared with existing commutation circuit based SCB (Christoph Meyer 2006). Here, the voltage distortion in PQ problem was selected for testing the performance of the proposed circuit. The voltage distortion clearance time of the proposed commutation circuit is less than that of the existing commutation circuit. So the fault duration of the proposed commutation circuit is low so the device is protected quickly. The matlab based simulink model of the proposed current comparator, varistor, digital switch based proposed commutation circuit topology A, B and C are shown in Figures 4.6, 4.7, 4.8, 4.9 and 4.10.
Figure 4.6 Proposed Current Comparator Model

Figure 4.7 Varistor Circuit Model
Figure 4.8 Simulink Model of Topology A with Digital Switch Circuit

Figure 4.9 Simulink Model of Topology B with Digital Switch Circuit
The PQ problem mitigation performances of the proposed commutation circuit and existing commutation circuit are shown as follow. The different tested topologies are topology A, B and C. Figure 4.11(a) and 4.11(b) are the proposed and existing commutation circuit based SCB voltage distortion clearing performance of topology A circuit, While the Figure 4.12(a) and 4.12(b) are the proposed and existing commutation circuit based SCB voltage distortion cleared performance of topology B circuit. Then the Figure 4.13(a) and 4.13(b) are the proposed and existing commutation circuit based SCB voltage distortion cleared performance of topology C with GCT circuit.
Figure 4.11 (a) Existing Topology A Circuit Based PQ problem clearing Performance

Figure 4.11(b) Proposed Topology A Circuit Based PQ problem clearing Performance
Figure 4.12 (a) Existing Topology B Circuit Based PQ problem clearing Performance

Figure 4.12(b) Proposed Topology B Circuit Based PQ problem Clearing Performance.
Figure 4.13(a) Existing Topology C with GCT Circuit Based PQ problem clearing Performance

Figure 4.13(b) Proposed Topology C with GCT Circuit Based PQ problem clearing Performance

From the above performances, the PQ problem is encircled and the zoomed view displayed at the end of the graph. In the zoomed view, the PQ
problem (voltage distortion) occurred in the proposed and the existing circuits are shown. Then the time taken to clear the PQ problem by proposed digital switch based commutation circuit and the existing capacitor based commutation circuit are compared. The time comparison for PQ problem Table 4.1 is shown as follow

**Table 4.1 PQ Problem Clearing Time in Proposed and Existing Circuit**

<table>
<thead>
<tr>
<th>Different Topologies</th>
<th>PQ Problem Clearing Time in Proposed Circuit (m sec)</th>
<th>PQ Problem Clearing Time in Existed Circuit (m sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topology A</td>
<td>427.841971</td>
<td>450.0783</td>
</tr>
<tr>
<td>Topology B</td>
<td>320.080382</td>
<td>342.257473</td>
</tr>
<tr>
<td>Topology C with GCT</td>
<td>304.112553</td>
<td>330.495709</td>
</tr>
</tbody>
</table>

![Performance Analysis](image1)

**Figure 4.14 Performance PQ Problem of Different Topologies Solved Time**
shown in Figure 4.14 performance comparison, the performance of topology A is less as compared to the topology B and topology C with GCT. The proposed digital switch based topology A, B and C circuits PQ clearing performances are improved by 5.2%, 6.9% and 8.7% respectively compared with existing circuit. The PQ problem clearing performance of proposed topology C with GCT is achieved in remarkable range. But the existing capacitor based commutation circuits are taking more time to solve the PQ problem. So the proposed digital commutation circuit performance is improved by existing capacitor commutation circuit. Hence the proposed digital commutation circuit has improved the performance of SCB for clearing the circuit failure problem.

4.5 CONCLUSION

The proposed technique of modified digital switch aided commutation circuit based SCB was simulated and the output performances were evaluated. The evaluated output performance of the proposed circuit was analyzed with the existing capacitor based commutation circuit. The output performance of the digital switch based commutation circuit was tested by considering a voltage distortion PQ problem. Then the voltage distortion clearing time of the different topologies A, B and C of the proposed circuit were analyzed. The proposed circuit based SCB voltage distortion clearing time performance was lesser compared with existing capacitor commutation circuit based SCB. The comparative results assured that the PQ enhanced the capability of the proposed commutation digital switch circuit based SCB over the existing commutation capacitor circuit based SCB. In the future work, other PQ issues can be considered for further evaluation of the proposed commutation digital switch circuit.