Appendix 3

Technical Specification of AT91SAM9263

The AT91SAM9263 32-bit microcontroller, based on the ARM926EJ-S processor, is architecture on a 9-layer matrix, allowing a maximum internal bandwidth of nine 32-bit buses. It also features two independent external memory buses, EBI0 and EBI1, capable of interfacing with a wide range of memory devices and an IDE hard disk. Two external buses prevent bottlenecks, thus guaranteeing maximum performance. The AT91SAM9263 embeds an LCD Controller supported by a Two D Graphics Controller and a 2-channel DMA Controller, and one Image Sensor Interface. It also integrates several standard peripherals, such as USART, SPI, TWI, Timer Counters, PWM Generators, Multimedia Card interface and one CAN Controller. When coupled with an external GPS engine, the AT91SAM9263 provides the ideal solution for navigation systems.

The main features of AT91SAM9263

• Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  – DSP Instruction Extensions
  – 16 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer
  – 220 MIPS at 200 MHz
  – Memory Management Unit
  – Embedded ICE, Debug Communication Channel Support

• Bus Matrix
  – Nine 32 bit layer Matrix, Allowing a Total of 28.8Gbps of On-chip Bus Bandwidth
– Boot Mode Select Option, Remap Command

• Embedded Memories
  – One 128 Kbyte Internal ROM, Single-cycle Access at Maximum Bus Matrix Speed
  – One 80 Kbyte Internal SRAM, Single-cycle Access at Maximum Processor or Bus Matrix Speed
  – One 16 Kbyte Internal SRAM, Single-cycle Access at Maximum Bus Matrix Speed

• Dual External Bus Interface (EBI0 and EBI1)
  – EBI0 Supports SDRAM, Static Memory, ECC-enabled NAND Flash
  – EBI1 Supports SDRAM, Static Memory and ECC-enabled NAND Flash

• DMA Controller (DMAC)
  – Acts as one Bus Matrix Master
  – Embeds 2 Unidirectional Channels with Programmable Priority, Address Generation, Channel Buffering and Control

• Twenty Peripheral DMA Controller Channels (PDC)

• LCD Controller
  – Supports Passive or Active Displays
  – Up to 24 bits per Pixel in TFT Mode, Up to 16 bits per Pixel in STN Colour Mode
  – Up to 16M Colours in TFT Mode, Resolution Up to 2048x2048, and Supports Virtual Screen Buffers

• Two D Graphics Accelerator
  – Line Draw, Block Transfer, Clipping, Commands Queuing

• Image Sensor Interface
  – ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
– 12-bit Data Interface for Support of High Sensibility Sensors

– SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format

**USB 2.0 Full Speed (12 Mega bits per second) Host Double Port**

– Dual On-chip Transceivers

– Integrated FIFOs and Dedicated DMA Channels

**USB 2.0 Full Speed (12 Mega bits per second) Device Port**

– On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM

**Ethernet MAC 10/100 Base-T**

– Media Independent Interface or Reduced Media Independent Interface

– 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit

**Fully-featured System Controller, including**

– Reset Controller, Shutdown Controller

– Twenty 32-bit Battery Backup Registers for a Total of 80 Bytes

– Clock Generator and Power Management Controller

– Advanced Interrupt Controller and Debug Unit

– Periodic Interval Timer, Watchdog Timer and Double Real-time Timer

Reset Controller (RSTC)

– Based on Two Power-on Reset Cells, Reset Source Identification and Reset Output Control

**Shutdown Controller (SHDWC)**

– Programmable Shutdown Pin Control and Wake-up Circuitry

**Clock Generator (CKGR)**

– 32768Hz Low-power Oscillator on Battery Backup Power Supply, Providing a
Permanent Slow Clock
– 3 to 20 MHz On-chip Oscillator and Two Up to 240 MHz PLLs

• Power Management Controller (PMC)
  – Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  – Four Programmable External Clock Signals

• Advanced Interrupt Controller (AIC)
  – Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  – Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected

• Debug Unit (DBGU)
  – 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
  – Mode for General Purpose Two-wire UART Serial Communication

• Periodic Interval Timer (PIT)
  – 20-bit Interval Timer plus 12-bit Interval Counter

• Watchdog Timer (WDT)
  – Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock

• Two Real-time Timers (RTT)
  – 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler

• Five 32-bit Parallel Input/output Controllers (PIOA, PIOB, PIOC, PIOD and PIOE)
  – 160 Programmable I/O Lines Multiplexed with Up to Two Peripheral I/Os
– Input Change Interrupt Capability on Each I/O Line
– Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output

• One Part 2.0A and Part 2.0B-compliant CAN Controller
  – 16 Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter

• Two Multimedia Card Interface (MCI)
  – SD Card/SDIO and Multi Media Card™ Compliant
  – Automatic Protocol Control and Fast Automatic Data Transfers with PDC
  – Two SD Card Slots Support on each Controller

• Two Synchronous Serial Controllers (SSC)
  – Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  – High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer

• One AC97 Controller (AC97C)
  – 6-channel Single AC97 Analog Front End Interface, Slot Assigner

• Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  – Individual Baud Rate Generator, Infrared Modulation/Demodulation,
    Manchester Encoding/Decoding
  – Support Smart Card, Hardware Handshaking, RS485 Support

• Two Master/Slave Serial Peripheral Interface (SPI)
  – 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects

• One Three-channel 16-bit Timer/Counters (TC)
  – Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  – Double PWM Generation, Capture/Waveform Mode, Up/Down Capability

• One Four-channel 16-bit PWM Controller (PWMC)
• One Two-wire Interface (TWI)
  – Master Mode Support, All Two-wire Atmel® EEPROMs Supported IEEE® 1149.1
  
  JTAG Boundary Scan on All Digital Pins

• Required Power Supplies
  – 1.08V to 1.32V for VDDCORE and VDDBU
  – 3.0V to 3.6V for VDDOSC and VDDPLL
  – 2.7V to 3.6V for VDDIOP0 (Peripheral I/Os)
  – 1.65V to 3.6V for VDDIOP1 (Peripheral I/Os)
  – Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM0/VDDIOM1 (Memory I/Os)
Figure A.3 AT91SAM9263 Block Diagram
Hardware Used:

i. LPC 2148

ii. Wireless Sensor Node

iii. LPC 2378 Board

iv. AT91SAM9263 Board

Figure A.4 A Snapshot of The Hardware Used In This Work
Sensor Nodes In cluster 1

Sensor Nodes In cluster 2

Sensor Nodes In cluster 3

Base Station

Figure A.5  A Framework – Wireless Sensor Networks