Appendix A: Detailed Explanation of PQ Event Generation Setup

The block diagram representation of the PQ event generation set up has been shown in Figure 2.17 of Chapter 2. The following blocks are explained in details hereafter

1. Digital to analog data conversion (DAC)(Block B of Figure 2.17)
2. Analog data processing stage(Block 2 of Figure 2.17)
3. Driver Stage (Block 3 of Figure 2.17)
4. Pulse Generator(Block 6 of Figure 2.17)

A.1 Digital to analog data conversion (DAC)

The schematic of the DAC module is shown in Figure A.1. The output current \(I_O\) is calculated using the following expression.

\[
I_O = K \left( \frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right) \quad (A.1)
\]

Where

\[
K \approx \frac{V_{REF}}{R} \quad (A.2)
\]

and \(A_1-A_8= \text{"1" if bits are high, otherwise '0' if bits are low.}\) The above equations as available in the datasheet are utilized to produce the desired analog voltage waveform as explained here. \(V_{REF}\) as shown in Figure A.1 is chosen to be 12V and the resistance R is selected as 4.7kΩ. In this case constant in equation A.1 is found out as \(K \approx \frac{V_{REF}}{R} = 12 \text{V} / 4.7k\Omega = 2.55\)
mA. Assuming all bit to be high in the digital data is $I_0 = K \times \frac{255}{256} = 2.54$ mA from equation A.1. In the module the load resistance $R_L$ is 2.2kΩ. Thus for all bits high (255) in digital data, the maximum output voltage is $-2.54 \times 2.2 = -5.588$ V. Therefore the analog output voltage swings between 0 and -5.59 V for 0-255 of digital input signal.

### A.2 Analog data processing stage

The analog data processing stage is shown in Figure A.2. In this circuit operational amplifier A1 (Op AmpA1) acts as a buffer that provides the impedance matching between the output of the DAC and the adder stage. Op AmpA3 is for adder and adjusts the zero level of the output signal. Op AmpA2 acts as constant voltage source to the other input of the adder for the required amplitude scaling operations. The output from Op AmpA2 can be adjusted by varying the potentiometer (VR1) for required scaling, i.e. zero level adjustment.

![Figure A.2: Analog Data Processing Stage](image)

### A.3 Driver Stage

Figure A.3 represents the driver stage circuit. Op AmpD in conjunction with transistors $Q_{D1}$ and $Q_{D2}$ operates in non-inverting mode in the driver stage. $Q_{D1}$ and $Q_{D2}$ are in the emitter follower mode so that high current drive can be given to step up transformer (4) (as shown in Figure 2.17 of Chapter 2). $R_{D1}$ and $R_{D2}$ control the gain of the driver stage so that the maximum input to transformer (4) is 10 V peak to peak for all wave shapes. $R_{D3}$ and $R_{D4}$ act as potential divider to the input of driver stage to limit the output to aforesaid
value. The gain stage comprising of $Q_{D2}$ and $R_{D1}$, along with the potential divider stage $R_{D3}$ and $R_{D4}$ at the input are so adjusted that the maximum output is $10V_p$.

The transformer (4) is a step up transformer having primary rating $10V_p$ and secondary rating $650V_p$. The power rating of the transformer is kept limited to 25 VA so that the secondary current of the transformer is $50mA$. High current output is not required because the generated voltage will be utilized by the developed PQ monitoring module for assessment purpose and not for true loading. The transformer is specially manufactured so that saturation does not take place in the core. As a result, the output follows the input waveshape for the PQ events as generated in the laboratory.

A.4 Pulse Generator

Figure A.4 represents the circuit that generates pulse. In this circuit transistor $Q_{P1}$ generates a sharp pulse at the input of a step up pulse transformer (5)(as shown in Figure 2.17 of Chapter 2). Transistor $Q_{P1}$ gets it pulse input from one port pin of microcontroller module as and when required. Capacitor $C_{P1}$ and resistor $R_{P1}$ as high pass filter to drive $Q_{P1}$. The secondary of transformer (5) is in series secondary circuit of transformer (4) so that the transient can be created at the output of PQ event Generator module. The peak of transient pulse is about $100V$. 

Figure A.3: Driver Stage
Appendix B: Description of the PQ event monitoring module

The schematic of the PQ event monitoring module is shown in Fig. B.1. This schematic is explained in the subsequent paragraphs.

The main component of the data acquisition system is the PIC24F series microcontroller that is clocked by an 8 MHz crystal oscillator which is internally multiplied by 2 to generate instruction cycle of duration 0.0625 μs. It has got 44 K words of program memory and 8 K of data memory. It is chosen for this application because of its low-power consumption, comparatively low-cost and inbuilt 10-bit A/D converter facilitating direct analog inputs to be fed at its pin. This ADC works according to the principle of Successive Approximation Register (SAR) conversion with Conversion speeds of up to 500 kS/s. Another advantage of this ADC is the voltage reference input which can be adjusted externally during the design phase. With a 3.3 V reference supply; the ADC has a resolution as low as 3.22 mV.

A low power quad op-amp IC1 (IC LM324) is used here as analog signal preprocessing in conjunction with the A/D converter to sample signals directly from the power line. IC LM336 is used for a precision 2.5 V voltage reference that is needed for scaling the signal.

Input from power line is divided by the potential divider consisting of the resistor R2 and R3 which brings downs the peak value of power line voltage

![Pulse generation circuit](image.png)
within ±1.1 V. IC1 performs the addition of reference of +1.1V with the input signal to map the input voltage within 0 to 2.2V. This is essential because the A/D converter of the microcontroller cannot accept any negative value.

To ensure optimum circuit design and minimum power consumption, the ports of the microcontroller are used effectively. The scaled voltage from the operational amplifier (IC1) is fed to the port B pin (RB0/AN0) that is configured to accept analog input. The parallel master port (PMP) of the microcontroller is programmed as data line output to a 162 alpha-numeric backlit LCD based on Hitachi HD44780 microcontroller. The display is configured to show the status of the input power quality, i.e. "sag" "swell" etc. One pin of port A (RA3) of the microcontroller is programmed to drive a relay as output through a transistor TR1. The contacts of the relay could be used according to the convenience of the user. Two pins of port F (RF5/U2Tx and RF4/U2Rx), which are internally connected to the UART engine of the microcontroller are kept for communication with PC using serial interface. Another pin of port A

Figure B.1: Schematic of developed PQ event monitoring module
(RA2) is connected to a LED for annunciation purpose. Line RA2 is capable of sourcing 20 mA current that is used for directly driving this indicator LED. The status LED is lit when a logic 0 is placed on this port and is turned off by logic 1.

The reset pin on the microcontroller is active low and is normally held to a positive voltage by a 1kΩ pull-up resistor. Pressing the tact switch SW1 shorts the reset pin of the microcontroller to ground thereby causing total system reset.

Serial interfacing between the developed board and PC is implemented using the MAX 3232 level shifter IC3 which is used to convert 0-3.3V voltages at which the microcontroller operates to ±12 V needed by the computer for its RS 232 communication purposes. Only three RS232 lines are used for serial communication in this application. RF5, RF4 and ground from the microcontroller are connected to the controlling computer’s RS232 Transmit Data (Tx), Receive Data (Rx) and logic Ground lines, respectively. The terminals from IC3 are terminated into a 9 pin socket for easily connecting the serial communication wire to the module. The photograph of developed PQ event monitoring module is shown in Fig. B.2

![Figure B.2: Developed stand-alone PQ event monitoring module.](image-url)