CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

Internet traffic has become voluminous in recent times due to the growth of real-time multimedia applications such as the Video on demand, Video telephony, Video streaming and e-learning applications. These bandwidth-intensive, delay-sensitive and loss-tolerant multimedia applications suffer in providing good Quality of Service (QoS) to users, and hence addressing the QoS issues becomes extremely essential. IP networks are evolving rapidly towards a QoS enabled infrastructure that supports a variety of existing and emerging multimedia applications. QoS requirements can be satisfied by managing the network resources such as the server load, channel capacity and computing power. The requirements of multimedia application are described by media quality parameters, such as the media data rate, transmission response time, Quality of Experience (QoE) and User Satisfaction Factor (USF).

Knowledge of System parameters and Network parameters is required for controlling the QoS of multimedia applications. System parameters describe communication and operating system requirements that are needed by the application. They include quantitative parameters such as Processing time in bits per second, number of errors, Data unit size and qualitative parameters such as inter-stream synchronization, ordered delivery of data, error recovery mechanisms and scheduling/caching mechanisms.
Network parameters are specified in terms of network load and network performance. Network load refers to the ongoing traffic parameters such as the packet inter-arrival time and the network performance parameters include throughput, bandwidth, end-to-end delay and jitter. Network services depend on the traffic model and traffic parameters such as the peak data rate and burst length, and hence the traffic parameters are dependent on the network parameters.

An exponential growth in Internet traffic due to multimedia applications requires an increase in the bandwidth and high speed in processing at the intermediate Internetworking devices like routers. To handle this heavy traffic, the present routers must process a million packets per second with a need to support the encryption/decryption of data, intelligent routing and quality of service guarantee. As a consequence, application specific processors in routers have become the core element in the design of routers. Increased network speeds coupled with new services delivered via the Internet have increased the demand for intelligence and flexibility at the places of interface in the Internet. This intelligence and flexibility can be provided by new hardware platforms comprising of heterogeneous multi-core engines with specialized communication support, called as Network Processors.

Network Processors are the latest class of silicon chips that revolutionize the support for multimedia applications at line speeds in the routers. The high performance of Network Processors is achieved by implementing packet processing technologies, such as the high speed address lookup, packet classification, queue management and scheduling. Powerful Embedded Network Processors introduced by many companies, have made these services possible by multithreading and multiprocessing.
Network Processors are very high performance processors that have been designed to cope with the rapid increase in network traffic. These processors can support up to 60 million operations per second, which is indeed a very impressive rate of processing. In order to operate at line speed, Network Processors must process and forward packets to and from queues at a rate higher than the incoming rate. Research has demonstrated the utility of placing application services on to Network Processors. Commercial Network Processors employ multiple parallel processors (Micro Engines) to exploit the packet level parallelism inherent in the network workloads. Each Micro Engine supports multithreading and hence processes multiple packets to achieve effective classification and efficient utilization of resources. Each Micro Engine (ME) has multiple hardware threads/contexts that enable context switches with zero or minimal overhead (Johnson et.al 2004). Hence, Network Processors are utilized for performing various packet processing functions.

1.2 STATE OF THE ART

Multimedia applications provisioning in the Internet has proved to be a very challenging goal to attain because of its transmission nature, buffering at end systems and dynamic adjustment of transmission parameters. Multimedia applications need to address plenty of technical issues, such as Quality of Service, congestion and security. The Internet has recently seen a steady rise in traffic due to the increase in large number of adaptive and non-adaptive multimedia applications and a loss rate across the network due to higher congestion at the core routers. The effective handling of the tremendous amount of Internet traffic due to media applications hinges on the processing ability of the intermediate Internetworking systems, especially the routers. The performance of the routers depends on the implementation of the packet handling mechanisms, such as admission control, resource reservation,
classification, per-flow queuing and fair scheduling. Packet classification is an enabling technology for the above mentioned packet handling mechanisms and is often a bottleneck in high performance routers as mentioned by David and Turner (2007).

The classification of the packets that arrive at the input port of the router is carried out by comparing the fields in the L3 / L4 header of the incoming packet as pointed out by Pankaj et al. (2001). A set of rules named as Filters (R) having the relevant attributes of the packets are stored as fields in the router table for the purpose of classifying the incoming packets. The classifier extracts the fields from the header of the incoming packet in the same order as in the Filter to perform multidimensional packet classification as mentioned by Baker (1995). The fields considered for classification are the source and destination address, protocol type and source port and destination port. Lakshmanan and Stidialis (1998) have mentioned that the classification of packets involves complex tasks, such as Longest Prefix Matching (LPM) for the source and destination address, Exact Matching (EM) for protocol and Range Matching (RM) for port. With large matching conditions, the best matching rule based on filters is to be chosen. In addition to this complex task, the packet classification has to be done at wire speed, which is a bottleneck at the routers.

A survey of the packet classification algorithms by David et al. (2005) shows that the classification problem is inherently hard to solve and at line speed is much harder. Currently, two major types of implementations of packet classifications are executed on commercialized products such as the software based implementation on the General Purpose Processor (GPP) by Naik and Chandra (2004) and the hardware based implementation on Application Specific Integrated Circuits (ASIC) by Timothy Sherwood et al. (2003). Software based algorithms for packet classification improve the
search speed and reduce the memory usage, but the performance is not adequate for practical high end deployment, because of the low CPU cache hit. The ASIC can perform packet classification at Gbps speed but these devices are limited because of customization and inflexibility at high speed processing. This inflexibility causes difficulties while upgrading the routers, which need to support diverse networking services, newer applications and also the production cost.

Network Processors (NP) have emerged as embedded processors that provide the performance of the ASICs and the programmability of the GPP as pointed out by Michel et al. (2004). The design and development of routers using these Embedded Network Processors have gained significance due to their high performance and flexibility. Hence, these computationally intensive packet classification functions are to be implemented at line speed using these Embedded Network Processors as suggested by Douglas. (2003).

Since multi-dimensional packet classification is a complex problem, a wide variety of algorithms have been proposed and explored by many researchers like Srinivasan et al. (1998, 1999) and Pankaj et al. (1999). Yie Tarrg et al. (2003) have designed a packet classification algorithm using rules partition and clustering and then employing the level compression scheme. Michael et al. (2003) described the directions for the design and implementation of packet classification using Network Processor. Deepa et al. (2004) studied the performance analysis of Multi-dimensional packet classification on programmable Network Processors using two different design mappings of Bit Vector packet Classification algorithms. Stefano Giordano et al. (2006) designed a multidimensional packet classifier and realized it on the Intel IXP 2400 Network Processor. Robin et al. (2006) proposed a software based packet classification through the use of a bloom filter and hash table lookup in the Intrusion Detection System using the
Network Processor. ClassBench, a suite of tools for benchmarking packet classification algorithms and devices has been developed by David and Turner (2007).

In addition to effectively classifying the packets, scheduling the packets over a shared network link is also essential to ensure QoS. Packet scheduling plays a vital role in providing QoS for multimedia applications, because the queuing delay experienced by each packet at the intermediary router has a greater impact on the quality of multimedia services. The scheduler should schedule the packets based on the available resources, such as bandwidth and buffer space, to provide a fair service to all traffic flows. In order to meet the QoS challenges such as reducing the delay, jitter and increasing throughput and to enhance the QoS of multimedia traffic, efficient and intelligent scheduling algorithms must be implemented at the router.

Research on the design and implementation of Scheduling algorithms has been carried out by many scholars. Generalized Processor Sharing (GPS) also called Fluid Fair Queuing (FFQ) proposed by Parekh and Gallager (1993) is considered as the ideal scheduling discipline that achieves perfect fairness and isolation among competing flows. However, the fluid model assumed by the GPS is not amenable to practical implementation, as network communication takes place in the form of packets that must be transmitted atomically. The analysis and simulation of Weighted Fair Queuing (WFQ) algorithms have been carried out by Demers et al. (1989) by computing the deadline (timestamp) of each packet. The WFQ exhibits some short term unfairness, which is addressed by the Worst case Fair Weighted Fair Queuing (WF2Q) proposed by Bennett et al. (1996). The WFQ schedules the packet with the least deadline among all packets whereas the WF2Q considers those packets that have started receiving service from the GPS server. The Virtual Clock (VC) proposed by Zhang (1990) and the Self
clocked Fair Queuing (SCFQ) proposed by Golestani (1994) are timestamp
schedulers that computed deadlines efficiently without maintaining the GPS
server. Though deadline based schedulers have good delay properties and
fairness, they suffer from time complexity due to the sorting bottleneck.

Round-Robin schedulers are another broad class of schedulers that
eliminate bottlenecks due to sorting by assigning time slots to flows in a
round-robin fashion. The Weighted Round Robin (WRR) scheduling
proposed by Katevenis (1991) eliminates the drawbacks of fair queuing by
dividing the traffic classes based on bandwidth requirements and scheduling
them in a round-robin fashion. The Deficit Round Robin (DRR) proposed by
Shreedhar and Varghese (1996) assigns a quantum size to each flow that is
proportional to the weight of the flow, along with the deficit counter for each
flow. Though DRR is simple to implement, it has poor delay bounds and
shows output burstiness. Attempts have been made by researchers to achieve
the best of Time stamp schedulers and Round-Robin schedulers by combining
the fairness and delay properties with low complexity. Shun et al. (2002)
proposed the Bin Sort Fair Queuing (BSFQ) that uses an approximate bin
sorting mechanism to schedule packets. The Stratified Round Robin (SRR)
algorithm proposed by Sriram et al. (2006) achieves good fairness and delay
properties with low complexity. The Quantum Based Earliest Deadline First
(QEDF) algorithm proposed by Teck et al. (2007) provides throughput
guarantees for rate based flows and delay guarantees for delay sensitive flows
but does not support multimedia applications exclusively. Bernardinis et al.
(2003), Jiani et al. (2005), Fariza et al. (2005) have designed input packet
scheduling algorithms and emphasized their implementation using the
Network Processor.
1.3 MOTIVATION AND OBJECTIVES

The success of the digital video, distributed computing and communication networks has created widespread opportunities for multimedia applications on the Internet. Applications of digital technologies include Video on demand, Video conferencing, Video streaming and e-learning. Unfortunately, media handling and media transmission applications require a greater support offered by the distributed computing environment and their network connections. Due to the heterogeneity of requirements coming from different Internet applications, achieving a good quality in these multimedia applications under varied channel conditions is challenging. These challenges could be addressed by a good design of Packet processing functionalities at inter-mediatory Internetworking devices by balancing the trade-off between throughput and fairness. Hence in this thesis, an attempt has been made to recognize the requirements of media applications and issues in achieving a better Quality of Service.

Several proposals to improve the quality of service for media applications in the Internet by incorporating the management of both computing and communication resources at bottleneck devices are in the way. Hence in this thesis, to enhance the QoS of multimedia applications, novel packet classification and scheduling mechanisms have been proposed and implemented.

This thesis investigates the functions in processing packets, such as receiving IP packets from incoming links, classifying and scheduling the packets, Output porting and the provisioning of the embedded Network Processors in implementing these functionalities to support Quality of Service issues of multimedia applications in the Internet. It is proposed to improve the Quality of Service of multimedia applications in the Internet by
incorporating a proper packet classification and scheduling mechanism at the routers using a Network Processor. More specifically the approach advocated in this thesis has the following goals:

- To study and evaluate the existing packet classification and scheduling algorithms.
- To design an efficient packet classification algorithm with reduced complexity that supports the router to operate at line speed.
- To devise an intelligent scheduling algorithm at the router, that improves the QoS of multimedia applications.
- To implement the proposed Packet Classification and Scheduling algorithm using an Embedded Network Processor.
- To prove that these proposed algorithms provide better QoS than the existing algorithms at line speed.

### 1.4 CONTRIBUTIONS TO THE THESIS

In this thesis, attempts were made to develop new algorithms for packet classification and packet scheduling mechanism in the Internet that enhance the QoS of multimedia applications. Three computationally efficient four dimensional packet classification algorithms have been developed. The first one is **Trie based Tuple Space Search (TTSS)** packet classification algorithm. In this TTSS, the complete search of rule base is eliminated by searching only possible sub rule bases to find the best matching rule, which reduces the time complexity. The reduction in time complexity implies reduction in number of memory accesses but lesser than wire speed. Hence, a modification to TTSS namely **Optimized Trie based Tuple Space**
Search (OTTSS) packet classification algorithm has been proposed by introducing median based search that achieves near wire speed and higher throughput. The third algorithm namely Heuristic based Application Specific Packet Classification (HASPC) has been evolved as an extended version of OTTSS where the decomposed sub rule bases of OTTSS have been decomposed further using the Port field. Thus, HASPC further reduced the number of memory accesses, thereby enabling wire speed classification. If the rule size is increased, the density of the sub rule base will also be increased. As hierarchical partitioning is used, it continues till all the sub rule bases are small and until an exact match rule for the packet exists in only one sub rule base. Classification by the above algorithms causes an increase in pre processing time.

Two hybrid packet scheduling algorithms have been proposed. The first one is Bandwidth Adaptive Stratified Round Robin (BASRR) scheduling algorithm. BASRR services the packets of real-time applications using strict priority policy. Assigning priorities to multimedia packets blocks the other applications and also assigning bandwidth to privileged applications is not practically advisable. Hence, Dynamic Deadline Based Weighted Fairness Scheduling (D²WFS) algorithm has been proposed as a modification to the BASRR algorithm for inculcating the practical feasibility and for improving the performance further. The D²WFS algorithm assigns weight to each traffic flow based on its bandwidth requirement to provide rate differentiation and schedules the packets based on its deadline that ensures delay differentiation which helps in achieving lesser delay, lesser jitter and higher throughput compared to the existing algorithms. The proposed D²WFS packet scheduling algorithm used a fixed packet size to compute the weight and deadline for each packet which is not practical in the Internetworking environment. The proposed algorithms have been implemented and tested using the IXA SDK 3.51 simulator of the IXP 2400 Network Processor.
1.5 ORGANIZATION OF THE THESIS

The thesis entitled ‘Network Traffic Management using Embedded Network Processor for Enhancing Quality of Service of Multimedia Applications' aims to improve the Quality of Service of multimedia applications in the Internet. This dissertation is organized into five chapters as follows:

Chapter 1 gives an introduction to the research work carried out. It also highlights the motivation, findings of the literature survey, the objectives and organization of thesis.

Chapter 2 concentrates on the challenging issues of multimedia applications on the Internet. Further, this chapter zooms in the existing packet classification and packet scheduling mechanisms with their merits and demerits. This chapter also deals with the issues and challenges to be solved in the packet classification and scheduling algorithms. This chapter then presents some modifications suggested for the performance improvement of the classification and scheduling algorithms. Finally, it describes a detailed view of the Intel IXP 2400 embedded Network Processor and its architecture.

Chapter 3 deals with the proposed Trie based Tuple Space Search (TTSS) packet classification algorithm, the Optimized Trie based Tuple Space Search (OTTSS) packet classification algorithm and the Heuristic based Application Specific Packet Classification (HASPC) algorithm. The implementation of the proposed packet classification on the IXA SDK 3.51 simulator of the IXP 2400 Network Processor with the different evaluation results, in terms of various figures of merit, its comparison with the existing algorithms and a summary of the benefits of the proposed algorithm are
presented. The performance results show that the HASPC algorithm performs better than the other algorithms.

Chapter 4 explains the proposed Bandwidth Adaptive Stratified Round Robin (BASRR) scheduling algorithm and Dynamic Deadline Based Weighted Fairness Scheduling (D²WFS) algorithm that efficiently manages and schedules the traffic and enhances the Quality of multimedia applications. The results from the simulations indicate that the D²WFS algorithm has lower jitter, lower latency and higher throughput than the contemporary scheduling algorithms under various traffic conditions.

Chapter 5 summarizes the inferences arrived through this study and discusses the scope for future research in this field.

1.6 SUMMARY

This chapter gives an introduction to the scope of packet classification and packet scheduling functions for multimedia applications and their implementation in the Embedded Network Processor. The main issues in the design of packet classification and packet scheduling algorithms were discussed. Finally, the objectives and organization of different chapters in this thesis were described.