Chapter 1

Introduction

1.1. Background

It was as early as 1965 when Gordon Moore predicted that the number of transistors that can be integrated on to a single chip will double in every 18 months [1]. This law put forth by Moore has been a benchmark for semiconductor scaling for more than four decades. The IC industry which has been primarily driven by CMOS technology scaling is now forced to look into other alternatives as the scaling is fast approaching its fundamental limits. The International Technology Roadmap for Semiconductors (ITRS) has predicted that size limit of CMOS technology will be limited to about 5-nm to 10-nm and believes this limit will reach as early as 2017 [2].

CMOS ICs have become indispensable for daily life products, ranging from portable electronics to telecommunications and transportations [3]. Scaling of CMOS devices is being aggressively pursued by shrinking transistor dimensions, reducing power supply voltages and increasing operating frequencies. Such aggressive scaling adversely results in a series of non-ideal behaviors such as high leakage current and high-power density levels. Due to the incredible success of the Complementary Metal Oxide Semiconductor (CMOS) integrated circuits, computer chips have become ever cheaper, smaller, power-efficient, and at the same time much more capable. But there is a growing concern that CMOS is close to its scaling limits that it can no longer become ever faster and cheaper.

Historically, feature size scaling was limited by the photolithographic process used to manufacture semiconductor integrated circuits. But advances in fabrication technology, such as 193-nm immersion lithography and double patterning have pushed below the 32-nm mark, with 10-nm deemed possible [4-5]. Extreme Ultraviolet Lithography is being developed, promising even smaller feature sizes [6]. These dimensions approach the atomic scale and further downsizing is increasingly inhibited by the fundamental physical limits of the CMOS. Thus, the dimensions of CMOS transistor shrink and approaches towards the close proximity between source and drain,
which reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region.

CMOS lithography-based technology has encountered serious challenges in terms of power consumption, physical dimensions, leakage currents and doping fluctuations. The increasingly difficult and expensive lithography has pushed the researchers to find new alternatives in nano-meter regimes. For this very reason, researchers have been focusing on nanotechnology as an alternative. Nanotechnology, using new fabrication materials could potentially replace CMOS, because of the high device densities and low power consumption [2].

Extensive research has been conducted in recent years using transistor-less technologies at nano-scale, aiming to surpass the CMOS technology. These devices might achieve a device density of $10^{12}$ devices/cm$^2$, low power and operating frequencies in Tera Hertz [7]. In this direction Quantum-dot Cellular Automata (QCA) is a rising innovation and a good competitor for research domain. It is a new method of digital computation and information transformation originally proposed by Dr. Craig Lent [8] and appears to be implementing a possible alternative nanotechnology. QCA has received significant attention in recent years because of its high device density, extremely low power consumption and very high switching speed. QCA, as a new technology for nano-scale circuits with efficiency in structure and power consumption that can play influential role in next generation computing systems. In terms of future size, it is predicted that QCA cells of few nano-meter (nm) would be possible candidate in near future [8].

Quantum-dot cells are key components of QCA technologies to implement as Logic Gates, Wires, and Memories. The basic logic elements in QCA technology are the Majority gate and Inverter. Wires can be used for signal propagation in QCA circuits. Logic elements viz; AND gate & OR gate can be obtained by manipulating the Majority gate [9]. Though the technology is different from convention CMOS designs, it is effective and realistic to implement the low power logic circuits. Thus, QCA is a new innovation at nano-scale and an appealing substitute to ordinary CMOS. It is a possible technology for the next generation of digital circuits and systems and widely utilized as a part of advanced frameworks.
1.2. QCA an (Alternative) Solution

As an alternative of CMOS technology, Quantum-dot Cellular Automata (QCA) has received significant attention in recent years because of its high device density, extremely low power consumption, diminutive size and faster switching speed. Unlike conventional computers in which information is transferred from one place to another by means of electrical current, QCA transfers information by propagating a polarization state [10-11].

QCA is based upon encoding of binary information in the charge configuration within Quantum-dot cells. Computational power is provided by the Coulombic interaction between QCA cells. No current flows between cells and no power or information is delivered to internal cells. The interconnection between QCA cells is provided by cell-to-cell interaction due to the rearrangement of electron positions [9]. The two electrons are loaded in antipodal sides in Quantum-dots of a QCA cell.

The Quantum-dot in a QCA cell corresponds to a small semi-conductor nanostructure or Metal island with a diameter (2-10 nm), that is small enough to make their charging energy greater than $k_B T$ (where $k_B$ is Boltzmann's constant and $T$ is the operating temperature). The two mobile electrons in a QCA cell can move to different Quantum-dots by means of electron tunneling. The electronic sites, called “Quantum Dots” represent the locations which the electrons can occupy. Dots are coupled by tunnel junctions. Tunneling paths are represented by the lines connecting the Quantum-dots. An electron exhibits quantum mechanical properties in view of its size. A Quantum-dot structure is shown in Figure 1.1 [12].
QCA technologies can be implemented using 4-kinds of methods including Metal-island, Semiconductor, Molecular, and Magnetic. Metal-island can be fabricated using aluminum islands and aluminum-oxide tunnel junctions [13]. Semiconductor Quantum-dots are nanostructures implemented from standard semi-conductive materials such as InAs/GaAs [14], GaAs/AlGaAs [15-16] and GaAs or AlGa [17]. Molecular and Magnetic Quantum-dots have been introduced in [18-19].

The Metal-island implementations were introduced as a mean of proving the QCA concept. It is based on the Coulomb blocking phenomenon of nanostructures, and has shown to exhibit the electron switching as required by a QCA cell [20]. Coulomb blockade is lifted, by applying appropriate gate biases. The Coulomb blockade or Single-electron charging effect, which allows for the precise control of small numbers of electrons, provides an alternative operating principle for nano-meter scale devices.
1.3. Motivation

The design of a QCA circuit is radically different from the conventional design at both the logical level as well as the physical level. High-level designs focus on algorithm and logical design in addition to the physical design. Even though actual QCA circuit designs need to manage considerable physical interactions that are potentially undesirable and disruptive, the algorithmic approach is also an important aspect in large systems. Research into both circuit architectures and device design is required for profound understanding of QCA based nanotechnologies. This thesis focuses on the design, implementations and power analysis of novel logic circuits based on QCA.

As QCA device show great potential for computation, it is necessary to study design strategies and the performance of computer arithmetic circuits based on the new characteristics of QCA. There has been considerable research over the past decade on designing combinational and sequential logic circuits using QCA cells, as well as finding the suitable fabrication process. Arithmetic circuit design is a fundamental subject since Adders, Multipliers, Dividers and Square-Rooters are the most frequently used components in an Arithmetic Logic Unit (ALU). To exploit the characteristic of QCA technology and illustrate its potential benefit from a circuit design perspective, a performance, comparison with different circuits is needed, especially from large-scale designs with significant size and complexity issues. As used both conventional and novel structures of arithmetic circuits using QCA should be investigated. It would be interesting to investigate if large-scale designs in QCA are possible.

In contemporary QCA technology, the cells must be aligned precisely at nano-scale in order to provide correct functionality [7]. Thus proper testing for manufacturing defects and misalignment plays an important role for quality of QCA-based designs. Recent developments in cell manufacturing involves the deposition of molecule on substrate surface by self-assembly process [21]. These experiments that have indicated the missing or additional cells are inevitable for Molecular implementations because the process of cell deposition is very sensitive [22]. A small variation in process parameters may result in a defect. Moreover, these defects have pronounced functional effects when they occur within, or very near to the target device.
due to strong cell interaction [23]. Therefore, testing is an absolute necessity for detecting various types of defects like cell misplacements, presence or absence of cell etc., in QCA.

QCA systems may present some drawbacks, given the extremely pipelined architectures of QCA systems. As QCA seems very promising, there is a need to design and develop a QCA based circuits and systems for an end user. In this research, a QCADesigner and QCA-Pro, tool for QCA has been used to develop several novel logic circuits and power analysis respectively. Several efficient and low power circuits have been developed for QCA. Power analysis of low power QCA based circuits and implementations of reversible logic circuits have been carried in order to signify the clear-cut advantage of these circuits over there conventional counter parts. These circuits are found to have promising advantages such as a faster switching speed; low power consumption with a small size.

1.4. Objective and Scope of Thesis

Prior to this thesis, some research work has been done on QCA device and circuits. Few logic circuits have been designed by Lent, et al [9-10]. Initial work on the QCA architecture has been done to understand how QCA cells work physically and to subsequently understand QCA logical circuit designs. Other QCA circuits, such as Exclusive-OR (XOR) gate and Multiplexors using the QCA logic device-the Majority gate, were designed and studied. In doing so, it has been discovered that for some circuits/devices a QCA version could only be constructed by implementing the XOR-logical equation (i.e. Exclusive-OR (XOR) = A'B + AB') directly. However, combinational circuits such as the, XOR gates, Adder, Subtractor circuits could be constructed directly with QCA Majority gates.

Different kind of wire schemes (Standard, Coplanar, Multi-layer and Logical Crossing Wires) have been used to design new possible architectures for QCA. Care has been taken to reduce area, circuit complexity and clock delays of these circuits. The proposed XOR/XNOR topology evaluates the performance of various implementations of QCA circuits and proposes various efficient layouts with better performance. The proposed XOR/XNOR gates can be useful in phase detectors in digital circuits,
arithmetic operations and error detection & correction circuits. Accordingly, these designs have been utilized in various digital circuits and systems.

New logic gate called the Modified-Majority Voter (MMV) for QCA has been worked out. The proposed MMV gate has high significant attributes to explore new logic circuits with minimum area, circuit complexity and clock delays for QCA. Numerous combinational circuits have been designed and implemented using MMV gate. A new single-layer well-optimized structure for 3-input, 2-input Exclusive-OR (TIEO) /Exclusive-NOR (TIEN) gates have been proposed that are based on cell interactions. Since Full-Adders are the basic building blocks in designing arithmetic circuits, a low complexity and ultra-high speed QCA one-bit Single-layer Full-Adder cells and ultra-dense 1-bit Multi-layer Full-Adder cell is designed employing the TIEO gate. The detailed comprehensive energy consumption analysis as well as comparison has been performed over previously published QCA Full-Adder cells and the proposed design. QCADesigner and QCAPro-tools are used for verifying circuit functioning and estimating dissipated energy, respectively.

Novel reversible logic gates using QCA have been worked out and presented in this thesis. Several QCA arithmetic logic functions have been proved and implemented using the proposed reversible gates. The proposed arithmetic circuits have superior performance in terms of circuit parameters like cost, area, complexity and power consumption in comparison to the conventional approaches.

In addition, to the basic mathematical operations like Addition, Subtraction, Multiplication, and Division; a Square-Root is rendered as the most useful and applicable operation in scientific calculations. In this thesis, the first Logical Wire Crossing approach single-layer Square-Root array structure is successfully designed and implemented using Quantum-dot Cellular Automata technology. The simulation results achieved using QCADesigner tool authenticates the correct functionality of the proposed structure.

1.5. Literature Review

The evolution of electronic information technology (IT) and communications has been mainly possible by continuous progress in silicon-based Complementary
Metal Oxide Semiconductor (CMOS) technology. This continuous progress has been maintained mostly by its dimensional scaling, which results in exponential growth in both device density and performance. The reduction in costperfunction has steadily been increasing the economic productivity with every new technology. In addition to its scalability, the unique device properties such as high input resistance, self-isolation, zero static power dissipation, simple layout and process steps have made CMOS transistors as the main components of CMOS integrated circuits (ICs). However, the dimensions of CMOS transistor shrinks and approaches towards the close proximity between source and drain, which reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region. Thus avoiding further reduction size.

Dimensional scaling of CMOS transistors is reaching their fundamental physical limits [24-25]. Therefore, research has been actively carried out to find an alternative way to continue to follow Moore’s law. Among these efforts, various kinds of alternative memory and logic devices, so called “Beyond CMOS Devices,” have been proposed [8]. These nano-devices take advantage of the quantum mechanical phenomena and ballistic transport characteristics under lower supply voltage and hence low power consumption. These devices are expected to be used for ultra-high density integrated electronic computers due to their extremely small size.

Nano-wire Field-Effect Transistors (NWFETs) have drawn promising attention and have been considered an alternative to continue CMOS scaling, since their non-planar geometry provides superior electrostatic control of the channel than the conventional counter parts. The increasing attention in Nano-wire research stems from several key factors; their cost-effective “bottom-up” fabrication and high-yield reproducible electronic properties [26-28], which pave way for some fabrication challenges, higher carrier mobility, smooth surfaces and the ability to produce radial and axial Nano-wire hetero-structures [29-30], better scalability resulting from the fact that diameter of Nano-wires can be controlled down to well below 10 nm [31-32]. However, due to their smaller diameters, the inversion charge changes from surface inversion to bulk inversion due to quantum confinement. Thus, variations in Nano-wire dimensions due to fabrication imperfections can lead to perturbations in the carrier potential and scattering that degrade the charge transport characteristics. Also,
variations in Nano-wire diameters may lead to a variation in FET threshold voltage. Reducing variability is therefore a key challenge in making Nano-wire FETs a viable technology. Furthermore, quantum confinement effects make modeling of Nano-wire transistors a complex problem. The physics related to the operation of Nano-wire transistors needs to be well articulated so that simple compact models, including ballistic transport and realistic sub band parameters, can be developed for circuit design using SPICE-like simulators [33].

Carbon Nano Tubes (CNTs) were discovered in 1991 [34]. Due to their unique material properties [35], Carbon Nano Tubes (CNTs) have received worldwide attention from many research works. CNTs are grapheme (which is a two-dimensional honeycomb lattice of carbon atoms) sheets rolled up into cylinders. They show either metallic or semiconducting properties depending on the direction how CNTs are rolled up (chirality). Since the bandgap of semiconducting CNTs is inversely proportional to their diameters, threshold voltage can be easily controlled [36-38]. With their superior material properties, such as the excellent mechanical and thermal stability, large current carrying capacity, and high thermal conductivity, the metallic nano-tubes are attractive as future interconnects [39-41]. Along with these properties, the semiconducting nano-tubes also show great advantages as a channel material of high-performance FETs.

Single Electron Transistors (SETs) are very attractive devices for future large-scale integration, due to their small size and low-power dissipation at good speed. The basic structure of SET consists of three-terminals: drain, gate, source, and the second gate, is an optional. A schematic of SET is analogous to that of conventional MOSFETs. However, SET has a tiny conductive island coupled to a gate electrode with gate capacitance. Source and drain electrodes are connected to the island through a tunnel barrier (junction). In SETs small voltage is applied between the sources and drain electrodes by means of the “Coulomb blockade” phenomenon [42-44].

New applications and architectures that exploit the unique functionality of room temperature operating SET circuits have been developed, especially by monolithic integration of SETs with FET circuits to complement the conventional Si CMOS performance. Representative examples include SET/CMOS hybrid multi-value logic circuits [45], multiband filtering circuits [46], analog pattern matching circuits [47],
associative recognition tasks [48], and others [49], in which characteristic Coulomb blockade oscillations of SETs are typically utilized to reduce the number of devices. Note that certain aspects of the circuit performance, especially the room temperature operation [39], [47-49], already exceed the theoretical evaluation of the logic gate parameters for 2-nm SETs. These devices have theoretically estimated maximum operation temperature $T \sim 20$ K, integration density $n \sim 10^{11}$ cm$^{-2}$, and speed of the order of 1 GHz [50]. However, large threshold voltage variation continues to impede the realization of large scale SET circuits, making it difficult for SETs to compete directly with CMOS devices used to implement Boolean logic operations. Engineering breakthroughs are needed to eliminate the size and background charge fluctuations in order to suppress the threshold voltage variations.

Single-electron approaches, representing a bit by a Single-electron (“bit state logic”) [51] and the use of a single electron as a source of random number generations [52], have been limited to laboratory demonstrations. The problem of the limited fan-out, which is caused by using only a single electron in the truly Single-electron devices, may be solved by innovative circuit designs such as the binary decision-diagram [53]. Therefore, the deficiencies of CMOS have led to significant efforts to find appropriate alternatives and among the proposed solutions; nano-scale technologies such as Tunneling Phase Logic (TPL), Single Electron Tunneling (SET) and Quantum-dot Cellular Automata (QCA) have received considerable attention [54-58].

Recent researches have proposed Quantum-dot possible implementations for QCA cells. As such Quantum-dot cells has presented in [10, 59]. An adiabatic switching paradigm is developed for clock-controlled pipelined QCA architectures. The binary information is stored as electronic charge leading to less computing. Other investigators have been extending the theoretical analysis of QCA arrays. Tonamoto et al. [60] have proposed alternative ways of assembling QCA cells into useful devices. Lusth and Jackson [61] have applied graph theoretic analysis to QCA design. Chen and Porod [62] have developed sophisticated finite element models for gate depleted Quantum-dots in semiconductors that can relate Dot occupancy to particular bias conditions.
Authors in [63] have presented a simple clocked molecular QCA cell. The molecules show intrinsic bistability as a result of dipole charge configuration, which strongly couples to its neighbouring molecules. The study is elementary, indicative only of the possibility of using molecular QCA. Review of the possibility of implementing QCA in molecular scale or in nano-magnets has been done [64]. Quite a number of molecular structures for QCA have been suggested, and one such 2-Dot QCA has been implemented. It is predicted that the ultimate utility of QCA will come from combining currently existing technologies with advanced nanotechnology.

Experimental implementation of QCA in Nano-scale Metal-dot defined by tunnel barriers has been reported in [65]. Here the authors demonstrate a controlled polarization of QCA cell switching agreeing with theoretical predications. Clocked QCA operation is demonstrated on an example of a two cell shift register. In another study [66] fan-outs are presented.

Investigations related to switching speed and temperature dependence of QCA have been presented in [67]. Orthodox Coulomb blocked and master equation dynamic approach has been taken into consideration for a semi-infinite shift register design. The crucial role of power gain as a function of temperature has been shown. The behavior of such circuits as function of clock speed and temperature is yet to be fully explained [68]. It is found that circuit speed is limited by RC-time constant, so Majority Voters could work up to 450-degree K, while QCA wire could work up to room temperatures.

The QCA physical design problems have been addressed in context of VLSI physical design issues in [69]. It presents a comparison between ILP formulation and heuristic solution for problems like QCA partitioning, placement and routing of QCA circuits. It has been found that heuristic approach gives the most optimized results. Unidirectionality and Metastability problem within a QCA wire has been studied, 3D-architecture is proposed in place of asymmetric spacing in [70]. The classical calculation carried here has shown that 3D-configuration could also be the way to overcome Metastability problems. While H-memory is a design developed particularly for QCA, authors in [71] propose a new execution model that combines with H-memory for distributing the functionality of CPU throughout the memory structures.
Today’s QCA is almost constructed as four dot cells. However, five dot and even six dot QCA designs have also been reported in [72]. Recent, research studies are focusing for developing low power devices. First time, a QCA power dissipation model has been proposed by Timler and Lent in [73-74] by which average power dissipation of a typical QCA circuit is divided into two major components, “leakage” and “switching”. Power losses throughout clock vacillations (from low to high or high to low) is posited as leakage power and power losses during switching period is considered as switching power [73-75]. Numerous low power Adder circuits with the least energy dissipation have been proposed in literature [9, 76-79]. Additionally, considering fault-tolerant issues, lots of attempts have been made to implement QCA fault-tolerant Full-Adder cells [80-81]. In contrast to counterpart designs the proposed Full-Adder cell has the least energy dissipation. From the complexity, latency and area point of view the proposed adder structures virtually excels all the counter parts with a considerable superiority.

Since in this work, both gate level approach and a new explicit interaction approach have been utilized for designing QCA combinational circuits. We believe that the present research work will be of great interest to the future computations.

1.6. Thesis Organization

The thesis is organized Chapter-wise, as outlined below:

**Chapter 1** Presents an introduction of the work to be conducted under this research program. Background of the work, Motivation as well as Objectives to be followed under the research work has been summarized in this Chapter. A detailed introduction of literature review pertaining to the research conducted in the area has been discussed in this Chapter.

**Chapter 2** Provides comprehensive background information about QCA technology. Fundamental concepts, including basic operation of QCA cell, Wires, Majority gate, Inverters, and other Logic gates have been introduced. The basic logic gates are implemented using primitive Majority Voter. Moreover, the detailed clocking mechanism has been reviewed.
**Chapter 3** Presents a practical approach for implementing logic circuits using QCA technology. Conventional approach for implementing Exclusive-OR (XOR) gate and Exclusive-NOR (XNOR) gates has been reviewed. Some new designs for implementation of these gates using QCA have been proposed. These new implementations have been compared with conventional designs in terms of various QCA circuit parameters including complexity (cell counts), area, and latency (clock delays). The proposed designs have been analyzed with different types of Boolean algebra equations. Moreover, this Chapter presents implementation of a Multi-Layer Programmable Inverter/Buffer circuits using QCA XNOR / XOR gates.

**Chapter 4** Presents to implement various QCA Code Converter circuits using QCA Majority gate. Coding is used for reliable transmission over communication channels. Gray-codes are popularly used for such purposes. This Chapter presents the proposed implementation of several N-bit Binary-to-Gray converters, 4-bit Excess-3 code converter using QCA. Comparison of the existing code converters with conventional designs has been carried out to emphasize the advantage of the proposed implementations. The work conducted in this Chapter, thus, opens a wider path for digital communication circuits at nano-scale.

**Chapter 5** Presents a new QCA based multi-functional logic gate entitled Modified-Majority Voter (MMV) gate. The proposed MMV gate has been subjected to basic physical relation tests for potential energy analysis to confirm majority decisions. The proposed MMV gate is a new step towards computational studies. It is a programmable gate and can be used to implement various logic functions such as logic gates like 3-input, 2-input-AND, 3-input, 2-input-OR, 3-input, 2-Input-Exclusive-OR (XOR)/ Exclusive-NOR (XNOR) gates. Combinational logic circuits including one-bit Full Adder/Subtractor circuits, 4-bit Ripple Carry Adder and Parity Logic Generator/Checker circuits have been implemented using the proposed MMV gate. The circuits implemented using the MMV gate have been analyzed and compared on various circuit parameters with their conventional counterpart. Moreover, conventional QCA based Single layer 1-bit Full-Adder circuits have been compared with the proposed Single-layer Adder circuit in terms of power consumptions & other circuit parameters to demonstrate the advantages of the proposed design. QCADesigner and
QCAPro tools are used for verifying circuit functioning and estimating dissipated energy, respectively.

**Chapter 6** Presents QCA based implementation of Square-Root algorithms. These algorithms are referred to as non-restoring and restoring algorithm. A modular design called improved non-restoring 8-bit Square-Root has been used for implementation of Square-Root operation. As a result, Single-layer 8-bit Square-Root circuit has been presented in this Chapter. The necessity of designing Nanoelectronic-based architectures regardless of conventional gate-level designs has been the motivation behind the proposed designs.

**Chapter 7** Presents a new approach for implementation of new reversible logic gates using QCA. Reversible logic enjoys the advantages of low power consumption and reduced heat dissipation. A general purpose reversible logic QCA gates using QCA has been developed and tested. The said functional logic gates (called RLQG1, RLQG2 and RLQG3) have been used to implement several arithmetic functions like Full-Adder, Full-Subtractor and Full Adder-Subtractor. The Full Adder-Subtractor implemented using the said gates have been analyzed and compared on various circuit parameters with its conventional counterpart. The work conducted in this Chapter thus opens a new area of research for designing digital reversible logic circuits at nanoscale.

**Chapter 8** Presents summary of work done and various conclusions drawn out from the research work. A brief description of scope for future work has also been presented in the thesis.