CHAPTER 5

PERFORMANCE OF ISOLATED BDC

5.1 INTRODUCTION

The bidirectional converters enable energy transfer between the DC circuits of different voltage levels and also assure galvanic separation in both power distribution systems and HEV applications. This chapter presents an analysis of the power transfer between two DC circuits with the help of IBDC. The BDC allows both forward and reverse power flow between two sources. As the need of bidirectional DC-DC converters is increased, many researchers have focused various types of BDC design. Among those, the bidirectional DC-DC flyback converter becomes more popular because its structure is very simple and easy to control. Apart from this, the power devices used in these converters are subjected to high voltage stresses. This is mainly caused due to transformer’s energy leakage from inductor.

The configuration of an IBDC topology is also called Dual Active Bridge (DAB) converter which is implemented in high power transfer systems for isolation. It is suitable for accomplishing high power density and galvanic isolation between the sources. Apart from this, it also performs ZVS operation and higher bidirectional power transfer capability. The controller design issue for a DC-DC DAB converter is regulated using a single-phase DC–AC inverter (Hengsi et al. 2014). In this method, two control methods were implemented to achieve ripple reduction in the DAB converter.
Several soft computing methods were adapted for controlling DAB. A fuzzy based DAB converter system is introduced by Sowmya et al. (2015) which have reduced stress and good transient response. Then the implementation of DAB in medium and high power application is proposed by Preethi et al. (2014). The converter achieves ZVS for all the switches and is capable of performing DC to DC conversion with high efficiency. A three stage of solid state transformer configuration includes AC-DC rectifier, isolated DC-DC DAB converter and DC-AC inverter has been studied by Digvijay et al. (2015). The proposed configuration gives better transient response and achieves the ripple reduction at the output of inverter.

From the above discussion, it is revealed that the design of DAB converter is carried out with only PI and fuzzy controller. Hence, this chapter deals with the analysis of closed loop controlled DAB bidirectional DC-DC converter system suitable for HEV applications. Hence, to confirm the effectiveness of the proposed module, the simulation is carried out using MATLAB simulink and the results are verified experimentally.

5.2 DESCRIPTION OF THE PROPOSED CONVERTER

The proposed converter shown in Figure 5.1 provides a galvanic isolation between two electrical circuits to eliminate stray currents. Due to electrical supply system imbalances, it may results in stray currents. A galvanic isolator does offer protection from stray currents. Hence, transformer is used to achieve voltage matching and galvanic isolation. Therefore an AC link is needed for the energy transfer. The first stage of a DAB converter is connected to a single-phase rectifier. It converts the AC voltage into a fixed DC voltage. Then the output of the DAB converter is connected to inverter which in turn drives the load. As the output of the DAB converter is connected
to an inverter, a large capacitor band is required at its output. As a result, the harmonic current present in the system is absorbed by this capacitor bank and also minimizes the output ripple voltage.

![Image of circuit configuration](image)

**Figure 5.1 Circuit configuration of the proposed IBDC**

### 5.3 PROPOSED IBDC WITH FILTERS IN BOOST MODE

The quadratic passive filters are positioned at the proposed converter output, inorder to reduce the ripple content. The converter is simulated in boost mode using the blocks of simulink and the results are presented.

#### 5.3.1 IBDC with C-Filter

The input of 15 V DC is converted into high frequency AC using an inverter. The inverter output is stepped up using 1:2 transformer. The 30 V AC is converted into DC using a rectifier. The C-filter projected at the output of the converter reduces the ripple present in it. The boost mode control of IBDC with C-filter is presented in Figure 5.2. Thus the parameters used in the design of boost mode with C-filter are given below: Input DC voltage =15V; Primary
leakage inductance, \( L_1 = 0.5\mu H \); C-filter, \( C_o = 1000\mu F \) and RLE load of value 600\( \Omega \), 1mH and 2V respectively. The ripple in the output voltage is 0.05V for a 15V DC input which is depicted in Figure 5.3.

**Figure 5.2 Circuit diagram for proposed IBDC with C-filter in boost mode**

**Figure 5.3 Simulation results for proposed IBDC with C-filter in boost mode**
5.3.2 IBDC with Pi-filter

The proposed converter with Pi-filter is depicted in Figure 5.4. The simulation parameters used in the design of Pi-filter are as follows, $L_0=0.6\mu\text{H}$ and $C_1=C_2=1000\mu\text{F}$. Figure 5.5 shows the simulated output voltage during boost mode operation where the DC input voltage is 15V. The peak to peak output ripple voltage is 0.02V which is also described in Figure 5.5.

![Figure 5.4 Circuit diagram for proposed IBDC with Pi-filter in boost mode](image1)

![Figure 5.5 Simulation results for proposed IBDC with Pi-filter in boost mode](image2)
5.3.3 IBDC with Quad-Filter

The proposed converter operating in boost mode with Pi-filter is replaced by using quad-filter which is shown in Figure 5.6. The simulation parameters used for quad-filter are $L_o=0.6\mu H$, $C_1=C_2=500\mu F$, $C_3=1000\mu F$.

![Circuit Diagram](image)

**Figure 5.6 Circuit diagram for proposed IBDC with Quad-filter in boost mode**

![Simulation Results](image)

**Figure 5.7 Simulation results for proposed IBDC with Quad-filter in boost mode**

Figure 5.7 shows the simulated output voltage and ripple output voltage of IBDC for an input voltage of 15V DC. The peak to peak output ripple voltage is 0.0015V.
5.3.4 Results and discussion

The boost mode operation of IBDC in the presence of C, Pi and quad filter is studied and their corresponding results are thus compared to evaluate the performance of the converter. For an input voltage of 15V, the quad-filter produces 0.0015V. Thus the ripples are greatly reduced by using quad filter. For different values of input voltage, the corresponding ripple output voltages from C, Pi and Quad filters are tabulated which is shown in Table 5.1.

Table 5.1 Tabulation for IBDC – Forward mode ripple voltage

<table>
<thead>
<tr>
<th>Input voltage (V)</th>
<th>Forward mode output ripple voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>C-filter</td>
</tr>
<tr>
<td>15</td>
<td>0.05</td>
</tr>
<tr>
<td>30</td>
<td>0.13</td>
</tr>
<tr>
<td>45</td>
<td>0.21</td>
</tr>
<tr>
<td>60</td>
<td>0.3</td>
</tr>
</tbody>
</table>

From the above table, it is concluded that output ripple voltage is less for implementation of quad filter when compared to other two filters.

Figure 5.8 Comparative graph for IBDC – Forward mode ripple voltage
Figure 5.8 depicts the comparative graphical representation of all the three filters in proposed converter. Thus the proposed IBDC converter with quad filter is chosen as best and their performance is analysed with open loop and closed loop control.

5.4 STUDY OF PROPOSED IBDC IN BOOST MODE UNDER OPEN LOOP CONTROL

Figure 5.9 depicts the simulink model of the proposed IBDC in open loop control for a boost mode is performed successfully with quad-filter.

![Simulink model of the proposed IBDC in open loop control for boost mode](image)

The simulated voltage waveforms of input and output and also the corresponding power obtained during forward power flow direction is depicted in Figure 5.10. The proposed converter response is studied by varying the input voltage from 15V to 18V at time, t=1.0secs and the corresponding results are presented.
For the step input change of 4V, the corresponding output voltage changes by 8V and the load current increases by 0.01A is noted. The power also gets increased due to step change in the input voltage.

Figure 5.10 Analysis of proposed IBDC in open loop control for boost mode

5.5 STUDY OF PROPOSED IBDC IN BOOST MODE UNDER CLOSED LOOP CONTROL

The simulation results for proposed IBDC operating in boost mode using various controllers are discussed with a input voltage of 15V. The parameter settings for controllers are obtained using Zigler and Nicols method and are used for the simulation study.
5.5.1 IBDC with PI Controller

The simulink diagram of closed loop system with PI controller is shown in Figure 5.11. The following parameter settings are considered for PI controller: $K_p = 2.5$, $K_i = 3$ and $t_s = 50 \, \mu\text{secs}$.

![Simulink model of the proposed IBDC with PI controller in boost mode](image)

**Figure 5.11** Simulink model of the proposed IBDC with PI controller in boost mode

Figure 5.12 shows the output voltage and their corresponding output power obtained for an input voltage of 15V DC. At time $t=1.0\text{secs}$, it is suddenly incremented to 18V.

The input disturbance is given through switch combination. During this transition period, there is a change in the output power. Figure 5.12 demonstrates the converter output voltage for the nominal case of set value 30V and the PI controller response has reached its set value at $t=3.0\text{secs}$.
5.5.2 IBDC with PID Controller

Figure 5.13 shows the circuit diagram of the proposed IBDC with PID controller. The following parameter settings considered for PID controller are $K_p=5$, $K_i=7$, $K_d=0.92$ and $t_s=2\mu$secs. Figure 5.14 depicts the response of converter output voltage and output power when the input voltage is suddenly incremented from 15V to 18V at time $t=1.0$secs.

Figure 5.13 Simulink model of the proposed IBDC with PID controller in boost mode
From the results, it is inferred that there is slight variation in the output due to sudden change in the input voltage and the thus the controller effectively controls the converter output voltage and it reaches the steady state value quickly.

**5.5.3 IBDC with FPID Controller**

Figure 5.15 depicts the simulink diagram of proposed converter with FPID controller. The parameter settings considered for simulation studies are, $K_p=5$, $K_i=7$, $K_d=0.92$, $t_s=2\mu$secs, $\lambda=1.01$ and $\mu=0.98$. Figure 5.16 shows the proposed system output voltage and output power for the sudden variation in input voltage.

From the simulated waveforms, it is concluded that there is less fluctuation in the output, when the input is suddenly incremented from 15V to 18V at time $t=1.0$ secs. From the results, it is evident that the response of FPID controller is more efficient and less sensitive than a classical PID controller.
5.5.4 IBDC with Fuzzy Controller

The simulink model of the proposed IBDC with fuzzy controller in boost mode is depicted in Figure 5.17. The triangular membership function are chosen to estimate the input values. The switching pulses of the converter is controlled by the fuzzy controller output.
The proposed fuzzy system consists of five Membership Functions for error (E), change in error (CE), and output control signal (u). The implication from the system is obtained by means of Mamdani fuzzy reasoning method. The MAX-MIN composition is used as fuzzy reasoning approach. The Membersip Functions plots corresponding to the variables E (voltage error), CE (change in error) and fuzzy output control variable are illustrated in the Figures 5.18, 5.19 and 5.20 respectively. Table 5.3 summaries the rule table of the proposed controller.

Table 5.3 Rule base for IBDC

<table>
<thead>
<tr>
<th>e(n)/ce(n)</th>
<th>NB</th>
<th>NS</th>
<th>ZE</th>
<th>PS</th>
<th>PB</th>
</tr>
</thead>
<tbody>
<tr>
<td>NB</td>
<td>NB</td>
<td>NB</td>
<td>NB</td>
<td>NS</td>
<td>ZE</td>
</tr>
<tr>
<td>NS</td>
<td>NB</td>
<td>NB</td>
<td>NS</td>
<td>ZE</td>
<td>PS</td>
</tr>
<tr>
<td>ZE</td>
<td>NB</td>
<td>NS</td>
<td>ZE</td>
<td>PS</td>
<td>PB</td>
</tr>
<tr>
<td>PS</td>
<td>NS</td>
<td>ZE</td>
<td>PS</td>
<td>PB</td>
<td>PB</td>
</tr>
<tr>
<td>PB</td>
<td>ZE</td>
<td>PS</td>
<td>PB</td>
<td>PB</td>
<td>PB</td>
</tr>
</tbody>
</table>
Figure 5.18 Membership functions for \( e(n) \)

Figure 5.19 Membership functions for \( ce(n) \)

Figure 5.20 Membership functions for \( cu(n) \)

Figure 5.21 illustrates the performances of the proposed converter with fuzzy controller for the step change in input voltage from 15V to 18V. From the results, it is clearly stated that at any change in input voltage changes does not affect the performance of the converter and the output voltage attains its desired value very quickly without any overshoot.
5.5.5 IBDC with Neural Controller

Figure 5.22 shows the closed loop simulink diagram of IBDC using neural controller. The performance of the proposed converter is improved further by implementing an artificial neural network controller using multilayer back propagation method.

Figure 5.22 Simulink model of the proposed IBDC with Neural controller in boost mode
The back propagation algorithm trains the network. The structure of the neural network contains two layers, in which one acts as an input layer and the other one is the output layer. Each input layer has the input along with weights and thus the adder function computes the weighted sum and input layer. Thus the number of iteration executed is 100 and Stopping criterion: Maximum Epoch.

Figure 5.23 Analysis of proposed IBDC with Neural controller in boost mode

Figure 5.23 shows the waveforms of output voltage and power of IBDC with Neural controller. The steady state error of the neural controller is 0.002V. From the obtained results, it is observed that IBDC with neural controller posses a low settling time and low steady state error when compared with other controllers.

5.5.6 Results and discussion

The response of proposed IBDC is compared between the conventional and SCT based controllers operating in boost mode and are
summarized in Table 5.3. This is done in terms of rise time, peak time, settling time and steady state error.

Table 5.3 IBDC - Comparison of responses with various controllers in Boost mode

<table>
<thead>
<tr>
<th>Controllers for IBDC in Boost mode</th>
<th>Rise time</th>
<th>Settling time</th>
<th>Peak time</th>
<th>Steady state error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$T_r$</td>
<td>$T_s$</td>
<td>$T_p$</td>
<td>$E_{ss}$</td>
</tr>
<tr>
<td></td>
<td>(secs)</td>
<td>(secs)</td>
<td>(secs)</td>
<td>(V)</td>
</tr>
<tr>
<td>PI</td>
<td>0.25</td>
<td>3.5</td>
<td>1.35</td>
<td>0.6</td>
</tr>
<tr>
<td>PID</td>
<td>0.16</td>
<td>2.1</td>
<td>1.21</td>
<td>0.2</td>
</tr>
<tr>
<td>FPID</td>
<td>0.3</td>
<td>0.35</td>
<td>0.53</td>
<td>0.15</td>
</tr>
<tr>
<td>Fuzzy</td>
<td>0.12</td>
<td>-</td>
<td>-</td>
<td>0.005</td>
</tr>
<tr>
<td>Neural</td>
<td>0.1</td>
<td>-</td>
<td>-</td>
<td>0.002</td>
</tr>
</tbody>
</table>

From the above table, it is observed that proposed converter with neural controller provides better settling time. Also the steady state error gets reduced considerably from PI controller to neural controller. Thus, the choice of optimal control for the proposed converter operating in boost mode is chosen with neural controller which provides faster response with virtually no overshoots when compared to other controllers.

5.6 STUDY OF PROPOSED IBDC IN BOOST MODE WITH HYSTERESIS CONTROLLER

The proposed converter IBDC is designed with and without hysteresis controller so as to improve its dynamic response. The circuit models are developed with and without HC.
5.6.1 IBDC without HC

Figure 5.24 shows the proposed IBDC without HC in boost mode. The output boost voltage is compared with set voltage and thus it produces an error signal. This is then provided to the PI controller thereby improves the stability level of the converter by compensating the error signal. Voltage control is used to maintain a value of 30V at the output.

![Simulink model of IBDC without HC in boost mode](image)

**Figure 5.24 Simulink model of the proposed IBDC without HC in boost mode**

The step change in input is shown in Figure 5.25. At time t=1.0secs, the input voltage increases from 15V to 18V. Consequently, a corresponding variation in the output current is noted. The output current gets corrected and comes back to the normal value.

Figure 5.25 shows the output power of the converter without HC during change in input voltage. Thus the ripple current value of 0.05A is obtained without using HC.
Figure 5.25 Analysis of proposed IBDC without HC in boost mode

5.6.2 IBDC with HC

Figure 5.26 shows the proposed IBDC with HC in boost mode.

Figure 5.26 Simulink model of the proposed IBDC with HC in boost mode
Figure 5.27 represents the converter current response for the same variation in input voltage from 15V to 18V at time t=1.0secs. The output voltage and output current are sensed and compared with hysteresis controller to generate proper pulses for the switches. The simulated curve depicts that the ripples present in the output current is reduced from 0.05A to 0.003A with the presence of HC.

![Simulation curve](image)

**Figure 5.27 Analysis of proposed IBDC with HC in boost mode**

### 5.6.3 Results and discussion

The performance of IBDC with and without HC in boost mode is shown in Table 5.4.

<table>
<thead>
<tr>
<th>Mode of operation</th>
<th>Proposed IBDC</th>
<th>Rise time $T_r$ (secs)</th>
<th>Settling time $T_s$ (secs)</th>
<th>Peak time $T_p$ (secs)</th>
<th>Steady state error $E_{ss}$ (V)</th>
<th>Output ripple current $I_{or}$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Boost mode</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Without HC</td>
<td></td>
<td>1.21</td>
<td>2.5</td>
<td>1.2</td>
<td>2.5</td>
<td>0.05</td>
</tr>
<tr>
<td>With HC</td>
<td></td>
<td>1.1</td>
<td>1.3</td>
<td>1.1</td>
<td>1.7</td>
<td>0.003</td>
</tr>
</tbody>
</table>

Table 5.4 Time domain parameters in boost mode for IBDC
It is observed from the results, that while implementing HC in boost mode of operation, the steady state error and settling time is reduced to 0.8V and 1.2secs respectively. At the same time, the output current gets reduced to 0.0047A. Thus, the proposed converter with HC proposes an efficient regulated high quality output voltage with reduced ripple.

5.7 PROPOSED IBDC WITH FILTERS IN BUCK MODE

The performance of the proposed converter is also verified in buck mode with the same three types of filters and the results are presented.

5.7.1 IBDC with C-filter

The simulink model of proposed IBDC shown in Figure 5.28 is designed with C-filter for buck mode. The design parameters of buck mode with C-filter are given as follows: DC input voltage=15V; Primary leakage inductance, \( L_1 = 0.06\mu H \); C-filter, \( C_o = 2200\mu F \); RLE load of value 100\( \Omega \), 0.05\( \mu H \) and 2V respectively. The simulation results of 15V DC input voltage and the output DC voltage of 7.5V are depicted in Figure 5.29.

![Figure 5.28 Circuit diagram for proposed IBDC with C-filter in buck mode](image-url)
Simulation results for proposed IBDC with C-filter in buck mode

From the results, it can be observed that the output voltage is free from the ripple voltage and its peak to peak ripple voltage is about 0.18V.

5.7.2 IBDC with Pi-filter

The proposed IBDC with Pi-filter in buck mode is shown in Figure 5.30. The simulation parameters for Pi-filter is as follows, \( L_0=0.06\mu H \) and \( C_1=C_2=2200\mu F \). Figure 5.31 shows the simulated output voltage of 7V for buck mode with the DC input voltage of 15V. The ripple present in the output voltage is also described in Figure 5.31.
Figure 5.30 Circuit diagram for proposed IBDC with Pi-filter in buck mode

Figure 5.31 Simulation results for proposed IBDC with Pi-filter in buck mode

From the above waveforms, it is clearly stated that the peak to peak ripple voltage is reduced to 0.028V for the input of 15V DC.

3.7.3 IBDC with Quad-filter

The Pi-filter is replaced by using quad-filter in IBDC which is shown in Figure 5.32. The simulation parameters for quad-filter is as follows, \(L_0=0.06\mu H\), \(C_1 = C_2 = 5000 \mu F\) and \(C_3 = 1000 \mu F\).
The output voltage and output ripple voltage is shown in Figure 5.33. The output ripple voltage is 0.0012V. Thus from the graph, it is inferred that ripple voltage of the converter is much reduced with the help of quad filter.
5.7.4 Results and discussion

The proposed IBDC operating in buck mode is simulated with C, Pi and Quad filter and their corresponding results are thus compared, to evaluate the IBDC performance. For different values of input voltage, the corresponding results are tabulated which is shown in Table 5.5.

Table 5.5 Tabulation for IBDC – Reverse mode ripple voltage

<table>
<thead>
<tr>
<th>Input voltage (V)</th>
<th>Reverse mode output ripple voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>C-filter</td>
</tr>
<tr>
<td>15</td>
<td>0.18</td>
</tr>
<tr>
<td>30</td>
<td>0.21</td>
</tr>
<tr>
<td>60</td>
<td>0.25</td>
</tr>
<tr>
<td>120</td>
<td>0.31</td>
</tr>
</tbody>
</table>

Figure 5.34 illustrates the pictorial representation of all the three filter performance in reverse mode of operation.

![Graph showing Input Voltage Vs Output Ripple Voltage](image)

Figure 5.34 Comparative graph for IBDC – Reverse mode ripple voltage
From results, it is proven that the comparatively quad filter has a low ripple voltage with C and Pi filters and its ripple output voltage value increases, if the input voltage is increased. The reduction in ripple voltage enhances the converter efficiency. Hence the proposed converter with quad filter is chosen as best and the proposed converter performance is analysed under various modes of control.

5.8 STUDY OF PROPOSED IBDC IN BUCK MODE UNDER OPEN LOOP CONTROL

Figure 5.35 illustrates the simulink model of the proposed IBDC in open loop control. Figure 5.36 represents the simulated waveform of input voltage, output power and output voltage in the reverse power flow direction.

![Simulink model of the proposed IBDC in open loop control for buck mode](image)

The input voltage is kept at 15V for RLE load. The output voltage possesses less ripple due to the presence of quad filter. It also demonstrates the response of the proposed converter, where the input voltage is suddenly incremented at time t=0.5secs.
5.9 STUDY OF PROPOSED IBDC IN BUCK MODE UNDER CLOSED LOOP CONTROL

The performance of the proposed converter is improved by implementing conventional controllers such as PI, PID and FPID. Simulation results under closed loop controller using conventional controllers are discussed for buck mode with an input voltage of 15V.

5.9.1 IBDC with PI Controller

Figure 5.37 demonstrates the circuit diagram of the IBDC with PI controller. The following parameter settings are considered for PI controller: $K_p = 1.0$, $K_i = 3.0$ and $t_s=10\mu\text{secs}$. Figure 5.38 demonstrates the converter output power and output voltage.
Figure 5.37 Simulink model of the proposed IBDC with PI controller in buck mode

For the nominal case of set value 7.5V; the controller response has reached its set value at t=1.2secs. The input voltage is suddenly incremented to 16.5V at time t=0.5secs. The output voltage increases and then reduces to the required value. For the sudden change in input voltage, the PI controller regulates the voltage of the converter effectively. During this period, the output power is slightly varied.

Figure 5.38 Analysis of proposed IBDC with PI controller in buck mode
5.9.2 IBDC with PID Controller

Figure 5.39 demonstrates the simulink diagram of proposed converter using PID controller in buck mode. The parameter settings are considered for PID are $K_p=4$, $K_i=3$, $K_d=1$ and $t_s=5\mu\text{secs}$. Figure 5.40 depicts response of the converter output voltage and output power, when the input voltage is suddenly incremented to 16.5V. It reaches the steady state condition at time $t=1.12\text{secs}$. During this period the output power is slightly varied.

![Simulink model of the proposed IBDC with PID controller in buck mode](image)

**Figure 5.39 Simulink model of the proposed IBDC with PID controller in buck mode**

![Output Voltage vs. Time](image)

**Figure 5.40 Analysis of proposed IBDC with PID controller in buck mode**
5.9.3 IBDC with FPID Controller

The proposed converter with PID controller is replaced with FPID controller which is shown in Figure 5.41. The parameter settings are considered to be the same as used in boost mode of operation.

![Simulink model of the proposed IBDC with FPID controller in buck mode](image1)

**Figure 5.41 Simulink model of the proposed IBDC with FPID controller in buck mode**

![Output Voltage vs Time](image2)

![Output Power vs Time](image3)

**Figure 5.42 Analysis of proposed IBDC with FPID controller in buck mode**

Figure 5.42 shows the system output voltage and output power for the same step change in input from 15V to 16.5V. The settling time of the FPID controller is about 0.5secs. From the waveforms, it is inferred that the controller response is smooth eventhough there is sudden input variation.
5.9.4 IBDC with Fuzzy Controller

The simulink model of the IBDC with fuzzy controller is illustrated in Figure 5.43. The performance of the converter with fuzzy controller is depicted in Figure 5.44.

![Simulink model of the proposed IBDC with Fuzzy controller in buck mode](image)

**Figure 5.43 Simulink model of the proposed IBDC with Fuzzy controller in buck mode**

![Analysis of proposed IBDC with Fuzzy controller in buck mode](image)

**Figure 5.44 Analysis of proposed IBDC with Fuzzy controller in buck mode**

The result analysis clearly states that change in input voltage does not cause any overshoot or any other disturbances in the output voltage and it reaches the stabilized condition at time t=0.004secs.
5.9.5 IBDC with Neural Controller

The closed loop model of IBDC with Neural controller in buck mode is shown in Figure 5.45. Figure 5.46 displays the converter output voltage and output power with neural controller.

![Simulink model of the proposed IBDC with Neural controller in buck mode](image1)

![Analysis of proposed IBDC with Neural controller in buck mode](image2)

From the results, it is evident that the steady state error gets reduced to 0.002V when compared to fuzzy controller. The faster response and reduced steady state error improves the converter efficiency.
5.9.6 Results and discussion

Table 5.6 precise the response of IBDC operating in buck mode with conventional and SCT based controllers. The comparison is done in terms of peak time, settling time, rise time and steady state error.

Table 5.6 IBDC - Comparison of responses with various controllers in buck mode

<table>
<thead>
<tr>
<th>Controllers for IBDC in Buck mode</th>
<th>Rise time $T_r$ (secs)</th>
<th>Settling time $T_s$ (secs)</th>
<th>Peak time $T_p$ (secs)</th>
<th>Steady state error $E_{ss}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PI</td>
<td>0.035</td>
<td>1.03</td>
<td>0.7</td>
<td>0.06</td>
</tr>
<tr>
<td>PID</td>
<td>0.03</td>
<td>0.8</td>
<td>0.65</td>
<td>0.03</td>
</tr>
<tr>
<td>FPID</td>
<td>0.03</td>
<td>0.5</td>
<td>0.6</td>
<td>0.01</td>
</tr>
<tr>
<td>Fuzzy</td>
<td>0.025</td>
<td>-</td>
<td>-</td>
<td>0.004</td>
</tr>
<tr>
<td>Neural</td>
<td>0.02</td>
<td>-</td>
<td>-</td>
<td>0.002</td>
</tr>
</tbody>
</table>

It is obvious that the converter designed with neural controller posses less settling time and has minimised steady state error. Hence the converter efficiency is improved and shows improved transient response. Thus from the simulation results, the choice of optimal control for the proposed converter operating in buck mode is also chosen with neural controller.

5.10 STUDY OF PROPOSED IBDC WITH HYSTERESIS CONTROLLER IN BUCK MODE

Hysteresis controller is implemented to improve the dynamic response of the proposed converter. The proposed IBDC is designed with and
without HC for buck mode. The performance is analysed for the step change in input from 15V to 16.5V at time t=0.5secs and their corresponding results are presented.

5.10.1 IBDC without HC

Figure 5.47 shows the proposed IBDC without HC in buck mode. For the step change in input voltage, the corresponding output variation is shown in Figure 5.48.

![Simulink model of the proposed IBDC without HC in buck mode](image1)

![Analysis of proposed IBDC without HC in buck mode](image2)
It is found that the value of peak to peak ripple in output current of 0.004A is obtained from the below waveform.

5.10.2 IBDC with HC

Figure 5.49 shows the proposed IBDC with HC in buck mode. The voltage and current responses are sensed and compared with HC to generate proper pulses for the switches.

![Simulink model of the proposed IBDC with HC in buck mode](image)

**Figure 5.49 Simulink model of the proposed IBDC with HC in buck mode**

![Analysis of proposed IBDC with HC in buck mode](image)

**Figure 5.50 Analysis of proposed IBDC with HC in buck mode**
The simulated waveforms are shown in Figure 5.50. The peak to peak current ripple is 0.001A. The above waveforms depicts that the ripples present in the output current is reduced from 0.004A to 0.001A and the steady state error value measures to be 1.4V which is comparatively less as compared to IBDC without HC.

5.10.3 Results and discussion

The performance of IBDC with and without hysteresis controller in buck mode is shown in Table 5.7.

Table 5.7 IBDC-Time domain parameters in buck mode

<table>
<thead>
<tr>
<th>Mode of operation</th>
<th>Proposed IBDC</th>
<th>Rise time ($T_r$ (secs))</th>
<th>Settling time ($T_s$ (secs))</th>
<th>Peak time ($T_p$ (secs))</th>
<th>Steady state error ($E_{ss}$ (V))</th>
<th>Output ripple current ($I_{or}$ (A))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck mode</td>
<td>Without HC</td>
<td>0.56</td>
<td>1</td>
<td>0.63</td>
<td>2.9</td>
<td>0.004</td>
</tr>
<tr>
<td></td>
<td>With HC</td>
<td>0.55</td>
<td>0.6</td>
<td>0.54</td>
<td>1.4</td>
<td>0.001</td>
</tr>
</tbody>
</table>

From the above table, it is observed that the steady state error and the settling time are reduced to 1.5V and 0.4secs respectively by using HC in buck mode of operation. It can also be observed that the output current gets reduced to 0.003A by using HC.

Thus, the proposed converter with HC in buck mode proposes an efficient regulated high quality output voltage with reduced ripple.
5.11 EXPERIMENTAL RESULTS

Figure 5.51 presents the photograph of prototype model of the proposed IBDC. The prototype consists of control circuit, power circuit and load modules. The PWM signals generated by PWM generators drive the gate drivers, so that the power switches were set to ON and OFF condition.

![Prototype of the proposed IBDC](image)

**Figure 5.51 Prototype of the proposed IBDC**

Experimental results of transformer output voltage during boost and buck mode is represented in Figure 5.52. The output voltage waveform obtained during both the modes is also illustrated in Figure 5.52. From the waveforms, it is observed that the IBDC reduces the ripple present in output voltage of the converter.
Figure 5.52 Experimental results

Figure 5.53 Efficiency graph

Figure 5.53 shows the efficiency curves of IBDC in both control methods. It can be clearly found that the proposed converter achieves higher efficiency than the existing converter (Preethi et al. 2014). For all conditions
investigated, soft switching bidirectional proposed IBDC can be significantly improved by reducing system losses.

5.12 SUMMARY

In this work, the performance of proposed IBDC was presented. Simulation was done for IBDC with various filters and controllers and their comparative analysis were presented for both boost and buck mode. IBDC was also simulated with and without hysteresis controller in MATLAB by changing the step input voltage value. Simulation results were analyzed and compared with the results obtained using hardware circuits and the simulation model is validated. Thus, the IBDC ensures better voltage gains with ripple minimization than the conventional bidirectional boost/buck converter.