CHAPTER 3

PERFORMANCE OF NON-ISOLATED BDC

3.1 INTRODUCTION

The switching frequency of the BDC is increased to make the size of the converter compact. This in turn results in higher switching losses. To overcome this problem, various topologies of non-isolated BDCs are proposed with soft switching to improve the converter efficiency.

A non-isolated DC-DC converter with soft switching consists of an auxiliary circuit, an inductor, two switches and two diodes is proposed for achieving high efficiency at full range of load (Kirti et al. 2016). At the same time, during low and heavy loads, ZVS of switching device is achieved by energy storing component. Hence, the maximum efficiencies of 95.68% in step up mode and 94.02% in step down mode are measured in the proposed converter. The NBDC has been modeled by Minho Kwon et al. (2014) for high power applications. To obtain smooth change of mode, an optimized switching sequence has been introduced in addition to an intermediate switching pattern. The converter used for low power applications can be modified by separating the input and output side using a transformer for high power applications.

A non-isolated BDC with Liquid Crystal Display (LCD) clamp circuit is designed specifically (Barsana et al. 2016) for battery applications.
The proposed non-dissipative LCD snubber recycles the energy that flows throughout the switching period. Soft switching capability is achieved at all operating modes which in turn reduce the current ripple and switching loss with proper operation of the switches.

However, all these schemes indicate one or more drawbacks such as poor system efficiency and complexity of control methods and difficulty in hardware implementation. Keeping in view the above considerations, a new NBDC is proposed and their performances are analysed in this chapter. The proposed converter was simulated by using MATLAB /SIMULINK and the simulation results were successfully verified with experimental results.

### 3.2 DESCRIPTION OF THE PROPOSED CONVERTER

The circuit configuration of proposed NBDC is shown in Figure 3.1. In this proposed model, the switching loss can be reduced by adding passive elements to the conventional converter. The auxiliary circuit unit comprises of resonant inductor and resonant capacitors. This auxiliary circuit affords ZVS function and it cancels the ripple component present in the main inductor current irrespective of the power flow direction. This converter has two operation modes namely – step up and step down mode.

During step up mode, the ZVS condition is obtained by turning ON the switch S₁ and by switching OFF the switch S₂. Even though the inductor current level falls below zero, it flows continuously through the main inductor. When the level of the current crosses zero, there will be a change in direction of current. During step down mode, the performance of the switch S₁ and S₂ is reversed but is analysis is analogous to that of step up mode. (Jun-Gu Kim et al. (2010).
Figure 3.1 Circuit configuration of the proposed NBDC

The proposed NBDC transfers the power from input side, $V_L$ to output side, $V_H$ in step up mode whereas the power from output to input side is transferred during step down mode. During step up operation, the switch $S_2$ acts as a main switch whereas the switch $S_1$ acts as an auxiliary switch. Similarly, during step down process, the switch $S_1$ functions as a main switch and switch $S_2$ functions as an auxiliary switch. The switches $S_1$ and $S_2$ remains ON, whenever the current flows through anti-parallel diodes. Correspondingly, the conduction loss of the MOSFET is very low because of $R_{DS(ON)}$ value which is assumed to be low. Energy storable devices such as battery or Super-capacitor can be applied in the low voltage side whereas the converter high voltage side is associated with the inverter based systems.

3.3 PROPOSED NBDC WITH FILTERS IN BOOST MODE

In order to remove the ripples present in the output of the converter, filters are implemented. Thus the performance of the proposed converter is verified with three types of different filters like $C$, $Pi$ and Quad filters. The converter is simulated in boost mode using the blocks of simulink and the results are presented.
3.3.1 NBDC with C-filter

The operation of NBDC in step up mode with C-filter is presented in Figure 3.2. Voltage and current across the load are measured using voltage and current blocks. The output power is the product of output voltage and the output current. For simulation studies, the capacitor’s Equivalent Series Resistance (ESR) and internal resistance of the source are assumed to be negligible. The simulation parameters utilized in designing step mode with C-filter is given below: Input DC voltage=15V; Main Inductor, L = 20mH; Resonant inductor, $L_r = 60\mu$H and resonant capacitors, $C_{o1}=C_{o2}=100nF$; C-filter, $C_o = 100\mu$F and RLE load of value 50Ω, 1mH and 2V respectively. Figure 3.3 represents the DC input voltage of 15V. The PWM signals are applied across the MOSFET which acts as a switch.

![Figure 3.2 Circuit diagram for proposed NBDC with C-filter in boost mode](image)

The output voltage of 30V and the ripple present in output voltage are also described in Figure 3.3. The peak to peak ripple is 0.06V.
3.3.2 NBDC with Pi-filter

The proposed converter operating in boost mode with C-filter is replaced by using Pi-filter which is shown in Figure 3.4.
The simulation parameters used for Pi-filter are, \( L_0=60\mu \text{H} \) and \( C_1=C_2=100\mu \text{F} \). From the Figure 3.5, it is observed that the simulated output voltage is about 28.38V during step up mode for an input voltage of 15V DC.

![Figure 3.5 Simulation results for proposed NBDC with Pi-filter in boost mode](image)

The output ripple voltage is also described in Figure 3.5. The peak to peak ripple voltage is 0.02V. From the above waveforms it is clearly stated that the primary switch is also operated under ZVS method and hence the ripple voltage is reduced.

### 3.3.3 NBDC with Quad-filter

The proposed converter operating in boost mode with Pi-filter is replaced by using quad-filter which is shown in Figure 3.6. The simulation parameters used for quad-filter are \( L_0=60\mu \text{H} \), \( C_0=10\text{nF} \) and \( C_1=C_2=100\mu \text{F} \). Figure 3.7 shows the simulated output voltage of 28.38V in boost mode for the DC input voltage of 15V. The output voltage and output ripple voltage are also described in Figure 3.7.
The peak to peak ripple voltage is about 0.0013V. Therefore from the results, it is evident that the ripple present in output voltage gets reduced from 0.02V to 0.0013V with the help of quad-filter.
3.3.4 Results and discussion

The operation of the proposed NBDC under step up mode with C, Pi and Quad filter is studied using MATLAB simulation and their corresponding results are thus compared, to evaluate the performance of the converter. For an input voltage of 15V, the C-filter produces ripple output voltage of 0.09V, Pi-filter produces 0.02V whereas the quad-filter produces 0.0013V. Thus the ripples are greatly reduced by using quad filter. For different values of input voltage, the corresponding ripple output voltages from C, Pi and Quad filters are tabulated which is shown in Table 3.1. Figure 3.8 depicts the graphical illustration of the performance of proposed converter with three filters used.

<table>
<thead>
<tr>
<th>Input voltage, (V)</th>
<th>Boost mode output ripple voltage in (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>C-filter</td>
</tr>
<tr>
<td>15</td>
<td>0.09</td>
</tr>
<tr>
<td>30</td>
<td>0.12</td>
</tr>
<tr>
<td>45</td>
<td>0.19</td>
</tr>
<tr>
<td>60</td>
<td>0.25</td>
</tr>
</tbody>
</table>

From the above table, it is concluded that output ripple voltage is less for implementation of quad filter with the converter when compared to that of the other two filters. Thus the proposed NBDC converter with quad filter is chosen as best among the other two filters and the feasibility of the proposed converter is analysed under open loop and closed loop control. From the results, it is also inferred that the output ripple voltage is less with filters when compared to NBDC without filters.
3.4 STUDY OF OPEN LOOP CONTROL OF PROPOSED NBDC IN BOOST MODE

Figure 3.9 illustrates the NBDC operating in open loop system for a boost mode which is performed successfully with quad-filter and motor load. The simulated waveforms of NBDC under open loop control for an input voltage of 15V is shown in Figure 3.10.
3.5 STUDY OF CLOSED LOOP CONTROL OF PROPOSED NBDC IN BOOST MODE

The performance of the proposed converter can be further improved by implementing the conventional controllers such as PI, PID & FPID and SCT based controllers like Fuzzy & Neural controllers and a comparative study is carried out to analyse their performance. Simulation results under closed loop control in boost mode of operation with motor load are discussed for an input voltage of 15V. The parameter settings for controllers are obtained using Zigler and Nicols method and are used for the simulation study.

3.5.1 NBDC with PI Controller

Figure 3.11 and Figure 3.12 demonstrates the simulink model and simulation results of the proposed NBDC with PI controller in boost mode respectively. The values chosen for the controller design are given as follows: Proportional gain constant, $K_p = 0.1$ and Integral time constant, $K_i = 5$. 
The corresponding changes in the output voltage and speed are noted. The PI controller regulates the voltage and reaches its steady state condition at time $t=0.85\text{secs}$.

### 3.5.2 NBDC with PID Controller

The proposed NBDC operating in boost mode with PI controller is replaced by PID controller. Figure 3.13 demonstrates the closed loop simulink
diagram of proposed converter using PID controller. Initially $K_p$ and $K_i$ is set to zero. Then the values of $K_p$ and $K_i$ can be increased until the oscillation begins. Set the final value as the value of $K_p$ and $K_i$ for the proposed system. Finally, increase the value of $K_d$, until the system reaches its reference set point. Based on this, $K_p = 0.5010$, $K_i = 4.8940$ and Derivative time constant, $K_d = 4.8940$ is chosen for this controller design.

Figure 3.13 Simulink model of the proposed NBDC with PID controller in boost mode

Figure 3.14 Analysis of proposed NBDC with PID controller in boost mode
The corresponding voltage achieved at the output of 30V for a given 15V input is shown in Figure 3.14. It is noted that the speed of the motor settles at 330 rad/sec. From the simulated waveforms, it can be noted that the output gets settled quickly with reduced overshoot as compared with PI controlled systems. Hence it is proven that the response of PID controller is more efficient and also fast in regulating the output voltage of the proposed converter.

### 3.5.3 NBDC with FPID Controller

Although the analog control mechanism is proven to be the best for any industrial drive systems and are very sensitive to its parameter changes. Hence in order to overcome the above said drawbacks, Fractional PID is implemented. These controllers are less sensitive to changes of parameters of a controlled system.

![Simulink model of the proposed NBDC using FPID controller with its subsystem in boost mode](image)

**Figure 3.15** Simulink model of the proposed NBDC using FPID controller with its subsystem in boost mode
Figure 3.15 demonstrates the simulink model of the proposed NBDC using FPID controller with its subsystem in boost mode. The following parameter settings are considered for FPID controller: $K_p = 0.5010$, $K_i = 4.8940$, $K_d = 4.8940$, $\lambda = 0.99$ and $\mu = 1$.

![Figure 3.15 Simulink model of the proposed NBDC using FPID controller](image)

3.5.4 NBDC with Fuzzy Controller

The soft computing technique provides fast response time with virtually no overshoot. At the same time, self-tuning ability of controllers designed using SCT makes it more suitable for industrial applications. Apart from this, the property of on-line adaptation of controller to nonlinear system provides a favorable preference for industrial oriented applications. Therefore, SCT based controllers are implemented in this work.

Figure 3.16 Analysis of proposed NBDC with FPID controller in boost mode

Figure 3.16 displays the simulated output voltage and speed waveform of the motor. Therefore, it is evident that the response of FPID controller is more efficient and less sensitive than a classical PID controller.
Figure 3.17 Simulink model of the proposed NBDC with Fuzzy controller in boost mode

Figure 3.17 shows the closed loop simulink diagram of NBDC using Fuzzy controller. The design of FLC is categorized as follows,

- Five fuzzy sets (NB, NS, ZE, PS, PB) for each input and output variables.
- Triangular membership function is used for the simplicity.
- Implication using Mamdani-type.
- Defuzzification using Centroid method.

In this fuzzy control system, the error signal $e(k)$, change of error signal $ce(k)$, change of control signal $cu(k)$ and output current $I_{\text{max}}$ are considered as membership functions. It can be categorized as Negative Big (NB), Negative Small (NS), Zero (ZE), Positive Small (PS), and Positive Big (PB) as shown in Figure 3.18, Figure 3.19 and Figure 3.20 respectively. The control rules formed using the linguistic variables which is stored in the rule base using a rule evaluator. Thus the rules formed using the above said linguistic variables are specified in the Table 3.2.
Table 3.2 Rule base for NBDC

<table>
<thead>
<tr>
<th>e(k)/ce(k)</th>
<th>NB</th>
<th>NS</th>
<th>ZE</th>
<th>PS</th>
<th>PB</th>
</tr>
</thead>
<tbody>
<tr>
<td>NB</td>
<td>NB</td>
<td>NB</td>
<td>NB</td>
<td>NS</td>
<td>ZE</td>
</tr>
<tr>
<td>NS</td>
<td>NB</td>
<td>NB</td>
<td>NS</td>
<td>ZE</td>
<td>PS</td>
</tr>
<tr>
<td>ZE</td>
<td>NB</td>
<td>NS</td>
<td>ZE</td>
<td>PS</td>
<td>PB</td>
</tr>
<tr>
<td>PS</td>
<td>NS</td>
<td>ZE</td>
<td>PS</td>
<td>PB</td>
<td>PB</td>
</tr>
<tr>
<td>PB</td>
<td>ZE</td>
<td>PS</td>
<td>PB</td>
<td>PB</td>
<td>PB</td>
</tr>
</tbody>
</table>

In order to estimate the degree of membership of input values, a triangular membership functions are preferred because of its simplicity. The control signal obtained from the output of the fuzzy controller controls the PWM signals applied to the converter switches.

![Figure 3.18 Membership functions for e(k)](image)

**Figure 3.18 Membership functions for e(k)**

![Figure 3.19 Membership functions for ce(k)](image)

**Figure 3.19 Membership functions for ce(k)**

Figure 3.21 displays the response of the NBDC with fuzzy controller. From the results, it is evident that the settling time will be very less.
when compared to conventional controllers. And at the same time, the fuzzy controller exhibits faster response time with virtually no overshoot which results in improved dynamic performance of the proposed converter.

![Figure 3.20 Membership functions for cu(k)](image)

**Figure 3.20 Membership functions for cu(k)**

![Figure 3.21 Analysis of proposed NBDC with Fuzzy controller in boost mode](image)

**Figure 3.21 Analysis of proposed NBDC with Fuzzy controller in boost mode**

### 3.5.5 NBDC with Neural Controller

An artificial neural network controller using multilayer back propagation type is implemented to improve the performance of the NBDC furthermore. The proposed neural network is designed with the two layers. Out of these two layers, one layer is considered as input layer and the other
one is as output layer. Thus the weights of the input layer associated with the
adder function computes the weighted sum of the input layer. According to the
weighted sum, output of the neural network is obtained. Figure 3.22 shows the
simulink diagram of NBDC using neural controller and the Figure 3.23
displays voltage response and speed of the motor.

Figure 3.22 Simulink model of the proposed NBDC with Neural controller
in boost mode

Figure 3.23 Analysis of proposed NBDC with Neural controller
in boost mode
From the results, it is concluded that the settling time and steady state error value is very low with neural controller when compared to other controllers.

3.5.6 Results and discussion

Table 3.3 depicts the comparison of responses of various controlled NBDC in boost mode is done in terms of terms of rise time, peak time, settling time and steady state error.

Table 3.3 Comparison of responses with various controllers in boost mode

<table>
<thead>
<tr>
<th>NBDC with Controllers</th>
<th>Rise time $T_r$ (secs)</th>
<th>Settling time $T_s$ (secs)</th>
<th>Peak time $T_p$ (secs)</th>
<th>Steady state error $E_{ss}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boost mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PI</td>
<td>0.15</td>
<td>0.38</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>PID</td>
<td>0.10</td>
<td>0.23</td>
<td>0.83</td>
<td>2.4</td>
</tr>
<tr>
<td>F PID</td>
<td>0.09</td>
<td>0.04</td>
<td>0.21</td>
<td>0.15</td>
</tr>
<tr>
<td>Fuzzy</td>
<td>0.08</td>
<td>-</td>
<td>-</td>
<td>0.10</td>
</tr>
<tr>
<td>Neural</td>
<td>0.06</td>
<td>-</td>
<td>-</td>
<td>0.10</td>
</tr>
</tbody>
</table>

From the table, it is observed that proposed converter with neural controller provides better settling time. Also the steady state error gets reduced considerably from PI controller to neural controller. This ensures that the system can be controlled effectively with feedback. Thus, the choice of optimal control for the proposed converter operating in boost mode is chosen with neural controller when compared to other controllers. It is also shown that there is considerable improvement in the system transient characteristics in terms of time domain analysis and at the same time, performance index was also reduced by this proposed application.
3.6 STUDY OF PROPOSED NBDC IN BOOST MODE WITH HYSTERESIS CONTROLLER

In order to examine the greater time response, reduced settling time and low steady state value, the Hysteresis Controller (HC) is proposed. HC is designed for the converter so as to improve its dynamic response. The proposed converter is designed with and without HC for boost mode.

3.6.1 NBDC without HC

Figure 3.24 shows the proposed NBDC without HC in step up mode. The output voltage of the converter is measured and is compared with a set voltage of 30V. The difference between these two voltages is processed through PI controller. The output of PI controller is then compared with a sawtooth waveform and thus generates the switching pulses for the switch $S_2$. The change in input voltage is shown in Figure 3.25. At time $t=0.06$secs, the input voltage is raised from 15V to 19V. The corresponding variation in the output current for the disturbance in the input is presented in Figure 3.25.

Figure 3.24 Simulink model of the proposed NBDC without HC in boost mode
It is noted from the waveforms, the output voltage increases again at time $t=0.06\text{secs}$ for the input disturbance and then settles to 0.6A at time $t=0.16\text{secs}$.

![Figure 3.25 Analysis of proposed NBDC without HC in boost mode](image)

### 3.6.2 NBDC with HC

Figure 3.26 shows the proposed NBDC with HC in boost mode.

![Figure 3.26 Simulink model of the proposed NBDC with HC in boost mode](image)
Figure 3.27 presents the converter current response for the same variation in input voltage from 15V to 19V at time t=0.06secs. The output voltage and output current are sensed and compared with HC to generate proper switching pulses for switches $S_1$ and $S_2$.

![Graph showing output current response](image1)

![Graph showing output ripple current](image2)

Figure 3.27 Analysis of proposed NBDC with HC in boost mode

From the above waveforms, it clearly states the output ripple current gets reduced and therefore current through the inductor is continuous.

3.6.3 Results and discussion

The performance of NBDC with and without Hysteresis controller in boost mode of operation is shown in Table 3.4. It is observed from the table that the settling time and steady state error are reduced to 0.05secs and 0.27V respectively by using HC in boost mode. It can also be seen from the above table, the output current gets reduced to 0.02A.
Table 3.4 Time domain parameters in boost mode

<table>
<thead>
<tr>
<th>Mode of operation</th>
<th>Proposed NBDC</th>
<th>Rise time</th>
<th>Settling time</th>
<th>Peak time</th>
<th>Steady state error</th>
<th>Output ripple current</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$T_r$ (secs)</td>
<td>$T_s$ (secs)</td>
<td>$T_p$ (secs)</td>
<td>$E_{ss}$ (V)</td>
<td>$I_{or}$ (A)</td>
</tr>
<tr>
<td>Boost mode</td>
<td></td>
<td>0.13</td>
<td>0.17</td>
<td>0.16</td>
<td>0.4</td>
<td>0.13</td>
</tr>
<tr>
<td></td>
<td>With HC</td>
<td>0.11</td>
<td>0.12</td>
<td>0.10</td>
<td>0.13</td>
<td>0.11</td>
</tr>
<tr>
<td></td>
<td>With HC</td>
<td>0.11</td>
<td>0.12</td>
<td>0.10</td>
<td>0.13</td>
<td>0.11</td>
</tr>
</tbody>
</table>

Thus, the proposed converter with HC in boost mode proposes an efficient regulated high quality output voltage with reduced ripple.

3.7 PROPOSED NBDC WITH FILTERS IN BUCK MODE

The proposed NBDC performance is also verified in buck mode with the same three types of filters. The converter operating in buck mode is simulated using the blocks of MATLAB simulink and the corresponding results are presented.

3.7.1 NBDC with C-filter

Figure 3.28 shows the simulink model for NBDC in buck mode with C-filter. The simulation setup for buck mode with C-filter are given below: Input voltage, $V_{in}$=30V; Inductor, $L = 1.5\text{mH} \& L_r = 60\text{µH}$; C-filter, $C_0 = 10\text{µF}$; Capacitors $C_{o1}$ and $C_{o2}$=100nF and RLE load of value 25$\Omega$,1mH and 2V respectively. The output voltage of 15V is shown in Figure 3.29. The output voltage ripple is also described in Figure 3.29. The peak to peak ripple voltage is 0.08V.
Figure 3.28 Circuit diagram for proposed NBDC with C-filter in buck mode

Figure 3.29 Simulation results for proposed NBDC with C-filter in buck mode
3.7.2 NBDC with Pi-filter

The C-filter at the output of the NBDC is replaced by using Pi-filter which is shown in Figure 3.30. The parameters design for simulation set up with Pi-filter is given as, $L_0=1.5\text{mH}$ and $C_1 = C_2=10\mu\text{F}$. Figure 3.31 shows the simulated output voltage of 15V for buck mode with the 30V DC input.

![Figure 3.30 Circuit diagram for proposed NBDC with Pi-filter in buck mode](image)

![Figure 3.31 Simulation results for proposed NBDC with Pi-filter in buck mode](image)
The ripple output voltage is also described in Figure 3.31. The peak to peak ripple voltage is about 0.005V. From the waveforms it is clearly stated that the primary switch is also operated under ZVS method and hence the ripple voltage is reduced.

3.7.3 NBDC with Quad-filter

The Pi-filter is replaced by using quad-filter in the NBDC which is shown in Figure 3.32. The simulation parameters for quad-filter is as follows, Lo= 50µH, Co=1µF and C₁=C₂=10µF.

![Figure 3.32 Circuit diagram for proposed NBDC with Quad-filter in buck mode](image)

![Figure 3.33 Simulation results for proposed NBDC with Quad-filter in buck mode](image)
Figure 3.33 shows the simulated output voltage of 15V and output ripple voltage. The peak to peak ripple voltage is 0.002V.

3.7.4 Results and discussion

The proposed NBDC operating in buck mode is simulated with C, Pi and quad filter and their corresponding results are thus compared in order to evaluate the performance of the converter. For a given input voltage of 30V, the C-filter produces ripple output voltage of 0.08V, Pi-filter produces 0.005V whereas the quad-filter produces 0.002V. Thus the ripples are greatly reduced by using quad filter. For different values of input voltage, the corresponding ripple output voltages from C, Pi and Quad filters are tabulated which is shown in Table 3.5.

Table 3.5 Tabulation for NBDC – Buck mode ripple voltage

<table>
<thead>
<tr>
<th>Input voltage, (V)</th>
<th>Buck mode output ripple voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>C-filter</td>
</tr>
<tr>
<td>30</td>
<td>0.08</td>
</tr>
<tr>
<td>60</td>
<td>0.12</td>
</tr>
<tr>
<td>120</td>
<td>0.21</td>
</tr>
<tr>
<td>180</td>
<td>0.33</td>
</tr>
</tbody>
</table>

From the above table, it is concluded that output ripple voltage is less in quad-filter when compared to that of the other two filters. Figure 3.34 shows the graphical illustration of performance of the filters in reverse mode for the proposed converter. Thus the proposed NBDC converter in buck mode with quad filter is chosen as best among the other two filters and the feasibility of the proposed converter is analysed under open loop and closed loop control.
3.8 STUDY OF OPEN LOOP CONTROL OF PROPOSED NBDC IN BUCK MODE

Figure 3.35 illustrates the NBDC operating in buck mode under open loop system which is performed successfully with quad-filter and motor load. The simulated waveforms of NBDC under open loop control for an input voltage of 30V is shown in Figure 3.36. The speed of the motor settles at 160 rad/sec. The torque response is also shown in the Figure 3.36.
3.9 STUDY OF CLOSED LOOP CONTROL OF PROPOSED NBDC IN BUCK MODE

To equip the proposed converter against any disturbances, closed loop control is implemented. Thus, an analysis of converter under closed loop control is carried out with both the conventional controllers such as PI, PID and FPID and SCT based controllers like fuzzy and neural controllers. Simulation results for various controllers with motor load are discussed for buck mode. The input voltage applied to the converter is 30V.

3.9.1 NBDC with PI Controller

Figure 3.37 and Figure 3.38 demonstrates the circuit diagram of the NBDC with PI controller and its corresponding simulation waveforms. The following parameter settings are considered for PI controller: \( K_p = 0.1 \), \( K_i = 1 \) and sample time, \( ts=50\mu\text{secs} \).
Figure 3.37 Simulink model of the proposed NBDC with PI controller in buck mode

Figure 3.38 Analysis of proposed NBDC with PI controller in buck mode

From the waveforms, it is seen that the output voltage regulated by PI controller reaches its steady state condition.

3.9.2 NBDC with PID Controller

Figure 3.39 demonstrates the simulink diagram of proposed converter using PID controller in buck mode. The parameter settings
considered for PID controller are $K_p = 1.0$, $K_i = 1.0$ and $K_d = 1.0$, $t_s = 0.5 \mu$secs.

Figure 3.40 illustrates the simulated waveforms of output voltage and speed of the motor.

![Simulink model of the proposed NBDC with PID controller in buck mode](image)

**Figure 3.39 Simulink model of the proposed NBDC with PID controller in buck mode**

From the analysis, it is proven that the responses of PID controller is more efficient and are fast in regulating the output voltage of the proposed converter.

![Output Voltage](image)

![Speed](image)

**Figure 3.40 Analysis of proposed NBDC with PID controller in buck mode**
3.9.3 NBDC with FPID Controller

Figure 3.41 demonstrates the simulink model of proposed converter using FPID controller. The parameter settings, $K_p = 0.5010$, $K_i = K_d = 4.8940$, $\lambda=0.99$ and $\mu=1$ are considered for simulation study.

![Simulink model of the proposed NBDC with FPID controller in buck mode](image)

From the results, it is concluded that the response of FPID controller is more efficient and less sensitive than a classical PID controller.

![Analysis of proposed NBDC with FPID controller in buck mode](image)
3.9.4 NBDC with Fuzzy Controller

Figure 3.43 shows the closed loop model of NBDC with Fuzzy controller in buck mode. Figure 3.44 displays output voltage and speed of the motor with fuzzy controller.

Figure 3.43 Simulink model of the proposed NBDC with Fuzzy controller in buck mode

Figure 3.44 Analysis of proposed NBDC with Fuzzy controller in buck mode
From the results, it is evident that the settling time in buck mode is very less when compared to conventional controllers. This results in improved dynamic performance of the converter.

3.9.5 NBDC with Neural Controller

Figure 3.45 shows the closed loop model of NBDC with Neural controller in buck mode. Figure 3.46 displays output voltage and speed of the motor with neural controller.

**Figure 3.45 Simulink model of the proposed NBDC with Neural controller in buck mode**

**Figure 3.46 Analysis of proposed NBDC with Neural controller in buck mode**
From the results, it is evident that the settling time of 0.125secs is very low in buck mode for neural controller when compared to fuzzy controller whose settling time is 0.15secs. The steady state error also gets reduced to 0.8V. The faster response time as well as reduced steady state error improves the converter efficiency.

3.9.6 Results and discussion

Table 3.6 depicts the comparison of responses of various controlled NBDC in buck mode is done in terms of rise time, peak time, settling time and steady state error.

<table>
<thead>
<tr>
<th>NBDC with Controllers</th>
<th>Rise time</th>
<th>Settling time</th>
<th>Peak time</th>
<th>Steady state error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$T_r$</td>
<td>$T_s$</td>
<td>$T_p$</td>
<td>$E_{ss}$</td>
</tr>
<tr>
<td>Buck mode</td>
<td>(secs)</td>
<td>(secs)</td>
<td>(secs)</td>
<td>(V)</td>
</tr>
<tr>
<td>PI</td>
<td>0.1</td>
<td>0.11</td>
<td>0.63</td>
<td>4</td>
</tr>
<tr>
<td>PID</td>
<td>0.08</td>
<td>0.09</td>
<td>0.52</td>
<td>2.7</td>
</tr>
<tr>
<td>FPID</td>
<td>0.07</td>
<td>0.08</td>
<td>0.03</td>
<td>1.2</td>
</tr>
<tr>
<td>Fuzzy</td>
<td>0.15</td>
<td>-</td>
<td>-</td>
<td>0.9</td>
</tr>
<tr>
<td>Neural</td>
<td>0.125</td>
<td>-</td>
<td>-</td>
<td>0.8</td>
</tr>
</tbody>
</table>

From the above table, it is observed that the proposed converter with neural controller provides faster response with low steady state error. Thus from the simulation results, the choice of optimal control for the proposed converter operating in buck mode is also chosen with neural controller which provides improved performance when compared to other controllers used.
3.10 STUDY OF PROPOSED NBDC IN BUCK MODE WITH HYSTERESIS CONTROLLER

Hysteresis controller is implemented to improve the dynamic response of NBDC. The proposed NBDC is designed with and without HC for buck mode.

3.10.1 NBDC without HC

Figure 3.47 shows the proposed NBDC without HC in boost mode. The output voltage is compared with a set voltage of 15V. The difference between these voltages is processed using a PI Controller. The output of PI controller in comparison with a saw tooth waveform generates proper switching pulses for switch S2. The step change in input voltage is shown in Figure 3.48. At time T=0.06secs, the input voltage is disturbed from 30V to 34V. Due to input disturbance, the corresponding variation in the output current is noted.

![Simulink model of the proposed NBDC without HC in buck mode](image_url)
The ripple present in the output current is depicted in the above waveform. The peak to peak value of a ripple current is about 0.4A.

Figure 3.48 Analysis of proposed NBDC without HC in buck mode

3.10.2 NBDC with HC

Figure 3.49 shows the proposed NBDC with HC in boost mode. The output voltage and output current are sensed and compared with HC to generate proper pulses for switches $S_1$ and $S_2$.

Figure 3.49 Simulink model of the proposed NBDC with HC in buck mode
For the same step change in input voltage from 30V to 34V at time \( t=0.06 \) sec, the corresponding changes in the output current is presented in Figure 3.50. The output ripple current is about 0.05A.

![Figure 3.50 Analysis of proposed NBDC with HC in buck mode](image)

### 3.10.3 Results and discussion

The performance of NBDC with and without Hysteresis controller in buck mode is shown in Table 3.7. It is observed from the table, that the steady state error and settling time are reduced to 0.61V and 0.026secs respectively by using HC in buck mode of operation.

<table>
<thead>
<tr>
<th>Mode of operation</th>
<th>Proposed NBDC</th>
<th>Rise time ( T_r ) (secs)</th>
<th>Settling time ( T_s ) (secs)</th>
<th>Peak time ( T_p ) (secs)</th>
<th>Steady state error ( E_{ss} ) (V)</th>
<th>Output ripple current ( I_{or} ) (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck mode</td>
<td>Without HC</td>
<td>0.067</td>
<td>0.08</td>
<td>0.07</td>
<td>0.7</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td>With HC</td>
<td>0.053</td>
<td>0.054</td>
<td>0.05</td>
<td>0.09</td>
<td>0.05</td>
</tr>
</tbody>
</table>
It can also be seen from the above table, the output current gets reduced to 0.35A by using HC. Thus, the proposed converter with HC in buck mode proposes an efficient regulated high quality output voltage with reduced ripple.

3.11 EXPERIMENTAL RESULTS

To test the performance of the studied NBDC, a laboratory prototype circuit illustrated in Figure 3.51 is implemented. The proposed NBDC parameters and specifications of the constructed hardware prototype are given as high-side voltage of 30 V and low-side voltage of 15V. IRF540 is used for all of the switches which provide fast switching and low on-state resistance.

Figure 3.51 Prototype of the proposed NBDC

Figure 3.52 shows the voltage waveform of the BDC in boost and buck mode respectively. During boost mode under ZVS condition, the main switch was in OFF condition. The switch S2 turns on under ZVS condition
while current flows through anti-parallel diode. During step down mode, both $S_1$ and $S_2$ were turned ON and turned OFF under ZVS condition similar to boost mode, even though the role of switches $S_1$ and $S_2$ was altered. The gate pulse and driver output pulse for the switches are also shown in Figure 3.52.

![Output voltage for buck mode](image1)

![Switching pulse for switches (5V)](image2)

![Output voltage for boost mode](image3)

![Driver output pulse for switches (10V)](image4)

**Figure 3.52 Experimental results of proposed NBDC**

Figure 3.53 describes the output power and efficiency comparative plots for both step down and step up mode. The efficiency graphs of conventional BDC examined by Neven et al. (2013) and proposed BDC is presented. When compared to the conventional converter, it is proved that NBDC posses higher efficiency. During boost mode, maximum efficiency of about 97.6% is achieved whereas during buck mode, it is about 97.48%. From the below curves, it is inferred that the proposed NBDC topology achieves higher efficiency about 2 to 3% than conventional converter topologies.
For all the conditions investigated, soft switching bidirectional buck-boost converter provides higher efficiency than the conventional converters.

3.12 SUMMARY

In this work, the performance of proposed NBDC was presented. Circuit models were developed for both buck and boost mode. The performance of the NBDC was measured by both simulation and hardware results. Thus the proposed NBDC provides improved performance in terms of low ripple at its output, better efficiency and good regulation when compared to conventional converter.