Chapter-7

Conclusions And Recommendations for Future Work

7.1 Conclusions

This chapter deals with the overall conclusions derived from the present work and a brief discussion about the probable extension of present work in future.

In this thesis, a generic surface potential based current voltage (I-V) model for doped or undoped asymmetric Double Gate (DG) MOSFET is presented. The model is derived from the 1-D Poisson equation with all the charge terms included and the channel potential is solved for the asymmetric DG MOSFET based on the Newton Raphson Iterative method. A non charge sheet based drain current model based on the Pao-Sah’s double integral method is formulated in terms of front and back gate surface potentials at the source and drain ends. The model is able to show clearly the dependence of the front and back surface potentials and the drain current on the terminal voltages, gate oxide thicknesses, channel doping concentrations and the silicon body thickness and A good agreement is observed with the 2-D numerical simulation results.

In recent times, the transistors with heavily doped channel have generated much interest due to its junction-less channel. In addition, the proper threshold voltage regulation requires adjustment of the channel doping so that most of the compact models become invalid as they consider an intrinsic body. In this thesis, a compact surface potential based threshold voltage model is developed for short channel asymmetric Double Gate MOSFETs with heavily / lightly doped channel. The 2D surface potential is computed and compared with TCAD and a relative error of 2-4 % was obtained. The threshold voltage is solved from 2-D Poisson’s equation using “virtual cathode” method and a good agreement is observed with the numerical simulations. Also the model is compared with the present existing model and a better result is obtained for heavily doped channel.

Here a surface potential based drain current and threshold voltage model for surrounding gate MOSFETs (SG MOSFETs) is also presented for all doping concentrations. The Newton Raphson iterative technique is implemented for the calculation of the potential at the surface and the center of the channel and the drain current is then computed. The relative error between the potential values obtained from the model and TCAD is within 2%. The drain current based on first iteration is much more accurate than the full depletion approximation. In the final part of this work, the threshold voltage is modeled based on two dimensional Poisson’s equation and the variation with channel radius is explored. A good match with the reference data is observed.

The last chapter of the thesis presents a systematic analytical model development for a sub-45-nm gate length Tunnel FET (TFET) and, assessment of the tunneling current based on the
classical model under asymmetric circumstances with the ambipolar effect. Performance analysis of the tunneling current for a sub-45 nm gate length TFET is performed using Kane’s model by considering high doping in the source and the drain regions and keeping the channel region low doped. The model explains the variation of tunneling current with the change in the oxide thickness under symmetric front and back gate voltages with, different metal work functions. The variation in the tunnel current is also analysed for the change in channel thickness under the symmetric front and back gate voltages for symmetric oxide thickness. A small decrement in tunnelling current with the increment of channel thickness due to reduced quantization effect under symmetric or asymmetric operation of the DG TFET is also efficiently captured by the developed model. The model is compared and verified with Sentaurus TCAD for all bias conditions and a good agreement has been achieved.

7.2 Recommendations for Future Work

In this thesis, the surface potential based compact drain current model is derived from 1-D Poisson’s expression using gradual channel approximation method to avoid charge sheet approximation technique for long channel MOSFETs considering all the charges i.e. depletion charge, inversion charge and hole charge such that it can be operated in both sub-threshold and super-threshold regions. To capture 2-D coupling effect in the surface potential for short channel devices and also for the surface potential based threshold voltage calculation, a nonhomogeneous 2-D Poisson’s expression is solved using superposition theorem considering all the charges. To determine surface potential in both long channel and short channel MOSFETs from a complex nonlinear mathematical form, an iterative method is used which generally suffers from more number of iterations and requires more convergence time. So to reduce simulation time and model complexity, a non iterative surface potential calculation method involving all the charge particles is highly recommended.

Gate tunneling effect also plays a significant role in MOS device modeling with scaling down of gate oxide thickness without corresponding reduction in operating voltage in the circuit. So, for thin oxide thickness, gate oxide faces high electric field for which large band bending occurs at Si-SiO₂ interface. This large band bending creates a potential well whose width is perpendicular to the surface and it is small compare to the carrier wavelength. So, quantization of electron energy occurs normal to the surface. Due to this strong vertical electric field, electrons tunnel through the triangular potential barrier induced at the gate oxide which cannot be explained classically but can only be described by quantum mechanical theorem. So, the gate tunneling effect should be incorporated in the drain current modeling as further extension of the present work.

Noise analysis is also an effective research area in MOS device modeling for RF IC applications which is not included in the present work. The noise generated by the device itself plays an important role when it is operated in GHz region for RF application. Thermal noise for the motion of charge carriers within the inversion layer, Flicker noise(1/f) for the surface conduction mechanism, Generation-Recombination noise for the trapping of charge particles near oxide-silicon interface, Gate resistance noise for the resistance of the polysilicon gate, substrate resistance noise incorporated to the substrate and Gate Tunneling Current Shot noise (GTC) which is generated due to scaling of gate oxide thickness are the various types of noises.
in MOS transistors which should be demonstrated by the corresponding analytical modeling for noise analysis in MOS device modeling. Therefore a physics based noise model which can accurately determine the noise characteristics of deep sub-micron MOSFETs is highly required. Gate misalignment is a vital problem at the time of fabrication of MOS transistors. When gates are not properly aligned, fringing effect plays an effective role in MOS device characteristics. Surface potential, threshold voltage and drain current characteristics of MOSFETs depend on the fringing effect emanating from the side walls of the front and back gates. Using conformal mapping transformation approach considering fringing effect on the non gate overlapping region, compact models for MOSFETs with gate misalignment effect should be formulated which should be considered as an extension of the present work. Same effect should be considered in modeling of DG TFET also. Development of a non-quasi static model of MOSFETs and TFETs are also should be considered as an extension of the present work in future.