CHAPTER 6

LINEARITY AND DISTORTION ANALYSIS: IMPACT OF HIGH TEMPERATURES
6.1: INTRODUCTION TO HIGH TEMPERATURE EFFECTS

Although the device performance is significantly improved over the time, the on-chip performance of the device is subject to various external factors such as operating temperature. With increasing number of on-chip transistors the total amount of heat dissipation significantly increases; as a result the operating temperature also increases. Thus, it is important to pre-emptively analyse the impact of temperature on device performance for better reliability. In previous works, the impact of temperature on silicon on insulator (SOI) MOSFET devices like FinFETs has been studied extensively for digital and analog applications [1]-[2]. However, for reliable analog and RF circuit design it is crucial to estimate the impact of temperature on the inherent reliability issues such as the linearity and the harmonic distortion (HD) of the CMOS devices [3][4].

In this chapter, a detailed analysis of the distortion characteristic of asymmetric underlap FinFET (U-FinFETs) due to the non-linear nature of the drain current ($I_{ds}$) is presented as a function of increasing operating temperature. The details regarding origin of U-FinFET structures were described in Chapter 5. In the following section the device structure and the simulation procedure for this analysis is presented. The analysis procedure description is followed by the linearity analysis and the HD analysis of the devices in order.

6.2: DEVICE STRUCTURE AND SIMULATION PROCEDURE

The specifications of the U-FinFET structure analyzed are illustrated in Fig. 6.1. The device structure is described by the silicon body thickness ($t_{si}$) of 16 nm, the gate length ($L_{gate}$) of 45 nm with an oxide thickness ($T_{ox}$) of 1.9 nm and a drain side underlap [5].

![Cross section of an idealized Underlap FinFET (U-FinFET) with drain side underlap.](image)
The source/drain (S/D) lengths are 50 nm. The Drain to Gate underlap length \((L_{un})\) is considered to be 20 nm after optimization, as described in [5]. The n\(^+\) S/D doping of the device is \(10^{20}\ \text{cm}^{-3}\) and the silicon body is lightly doped with doping concentration of \(10^{15}\ \text{cm}^{-3}\).

The U-FinFET Device presented in Fig. 6.1 is simulated with the three-dimensional (3D) numerical device simulator Sentaurus [6] and for accuracy and robustness the meshing strategy is optimized as described in [7]. The calibration of the simulator is done with the experimental data [8] considering the carrier mobility as described in [9]. In the device simulation, Density-Gradient model is used for carrier transport. The active carrier lifetime and density is dictated by the Shockley-Read-Hall (SRH) recombination and the incomplete ionization models, respectively. The mobility degradation including ionized impurity scattering is accounted by using the Lombardi mobility model. The simulated device is used to extract the \(I_{ds} - V_{gs}\) characteristics at different ambient temperatures as shown in Fig. 6.2 where, \(V_{gs}\) is the gate to source voltage. Subsequently, the \(I_{ds} - V_{gs}\) characteristics data are used for extracting and analysing the distortion characteristics.

![Fig. 6.2: The drain current \(I_{ds}\) of U-FinFETs as a function of gate voltage, \(V_{gs}\) for increasing operating temperature, \(T\).](image)

In the study, the distortion characteristics are extracted by implementing the Integral function method (IFM) [10]. In the IFM, the deviation of the non-linear characteristics from the linear one is represented by different integral functions. For linearity analysis of the device, the third order intercept point \((IIP_3)\) is considered. For
harmonic distortion, the impact of temperature is studied on distortion figure of merits (FOMs), the total harmonic distortion (THD), second order harmonic distortion (HD2), and the third order harmonic distortion (HD3) introduced by the device.

6.3: LINEARITY ANALYSIS OF U-FinFETs AT HIGH TEMPERATURES

An important aspect for an analog/RF circuit design using CMOS technology is to ensure minimum intermodulation and higher-order harmonics at the output. Also, the HD of a circuit is important because the device non-linearity should be nominal. However, the non-linear characteristics of the device vary with increasing operating temperature posing a reliability concern.

![Graph showing variation in third order output power point of intercept, IP3 for U-FinFETs at maximum g_m point as a function of operating temperature, T.](image)

Fig. 6.3: Variation in the third order output power point of intercept, IP3 for U-FinFETs at maximum g_m point as a function of operating temperature, T.

The linearity of the device is evaluated as a function of the intercept point between the fundamental frequency and the third harmonic output power defined as IIP3 [11]-[13]. The IIP3 of a device is inversely proportional to third order derivative of Ids [11]. The variation in IIP3 at the point of maximum g_m for U-FinFETs with increasing operating temperature is presented in Fig. 6.3.

It is observed from Fig. 6.3 that the linearity of U-FinFETs decreases with increasing operating temperature however, the degradation is noticeably low. The reduction in
linearity observed is about 1.4 dBm for an about 200 K temperature change. This degradation in the linearity can be elucidated from the $g_m - I_{ds}$ plot presented in Fig. 6.4.

![Image](image1.png)

**Fig. 6.4:** Transconductance ($g_m$) of the UFinFET with drain current ($I_{ds}$) for increasing temperature at drain voltage, $V_{ds} = 1.0 \text{ V}$. 

It is observed in Fig. 6.4 that the flattening of the $g_m - I_{ds}$ characteristics decreases with increasing temperature resulting in higher value for third order derivative of $I_{ds}$ thereby, degrading the linearity of the device [11]. The reduced flattening at higher temperatures is physically attributed to a rapid reduction in $g_m$ with $I_{ds}$ due to enhanced lattice vibration induced carrier scattering. However, due to the presence of non-inverted underlap, the impact of the high temperature is to some extent restricted in the channel region preventing a substantial change in the linearity characteristics. In the following section, the influence of this linearity variation is studied on the HD characteristics of the device.

**6.4: HARMONIC DISTORTION ANALYSIS OF U-FINFETS AT HIGH TEMPERATURES**

It is known that with the increase in the linearity of device characteristics, the HD introduced in the circuits is significantly diminished. However, as the linearity characteristics of U-FinFETs varies with increasing operating temperature it is necessary to analyse the HD of the device considering the carrier transport properties in the
device. In the present section, the HD characteristics of the device are analysed as a function of HD FOMs along with the analog parameters $g_m$ and $I_{ds}$.

A. Effects of Temperature on Harmonics Distortion of device

The HD FOMs of the UFinFET for high temperatures are extracted by implementing IFM on the $I_{ds}$-$V_{gs}$ characteristics of the device as described in [10] [12]-[13]. In order to understand the variations in the HD characteristics, approximate analytical expressions given by Eq. 5.1 and 5.5 are considered for the $HD2$ and the $HD3$ [14]. The amplitude of input sinusoid $V_a$ is considered to be very small [14].

The variation in $g_m$ and the absolute value of the rate of change of $g_m$, $|dg_m/dV_{gs}|$ with $V_{gs}$ for U-FinFETs as a function of the temperature is as presented in Fig. 6.5, and is vital for understanding the HD variation.

![Extracted transconductance of U-FinFETs with gate voltage, $V_{gs}$ for increasing temperature at drain voltage, $V_d=1.0$ V.](image)

Fig. 6.5: Extracted transconductance of U-FinFETs with gate voltage, $V_{gs}$ for increasing temperature at drain voltage, $V_d=1.0$ V.

In Fig. 6.6 and 6.7, the $HD2$ and $THD$ of U-FinFETs for different operating temperatures are presented as a function of $V_{gs}$, respectively. Since $HD2$ is the major distortion component, it is observed that the $THD$ of the device follows the $HD2$ characteristics. The HD2 characteristic of U-FinFETs at any temperature is described as following.
1. Initially, at low $V_{gs} < \sim 0.3$ V both $|dgm/dV_{gs}|$ and $g_m$ are high as a result, considering Eq. 5.1 the HD2 is high and almost constant with respect to $V_{gs}$ as observed in Fig. 6.6. However, the value of HD2 is lower for higher temperatures. This reduction in HD2 is due to the fact that, the increase in $g_m$ of the device at higher temperatures is much higher than that in $|dgm/dV_{gs}|$ with $V_{gs}$ as seen in Fig. 6.5 attributed to higher intrinsic carrier density.

2. As the $V_{gs}$ gradually increases in the range, $\sim 0.3$ V $< V_{gs} < \sim 0.9$ V, $|dgm/dV_{gs}|$ begins to decrease with $V_{gs}$ after reaching a maximum whereas, $g_m$ keeps increasing. Thus, considering Eq. 5.1, the HD2 of U-FinFETs begins to decrease gradually with respect to $V_{gs}$ and reaches a minimum at $\sim$0.9 V. The maximum in $|dgm/dV_{gs}|$ characteristics marks the onset of lattice scattering induced mobility degradation and it shifts to lower $V_{gs}$ for higher temperatures [15]-[17]. Thus, at higher temperatures the value of $g_m$ of U-FinFETs begins to decrease quickly. As a result considering Eq. 5.1, the rate of reduction in HD2 with $V_{gs}$ for higher temperature is low as observed in Fig. 6.6.

3. At $V_{gs} = \sim 0.9$ V, the $g_m$ of U-FinFETs reaches maximum and $|dgm/dV_{gs}|$ is almost ‘0.’ This marks the minimum of HD2 characteristics in Fig. 6.6. It is also observed that the $V_{gs}$ at minimum remains almost constant with temperature. This is attributed to slower rate of reduction in HD2 at higher temperatures as described above. In addition to this it is also observed from Fig. 6.5 that the maximum value of $g_m$ at higher temperatures is lower due to higher scattering rate.

4. For $V_{gs} > \sim 0.9$ V, the $|dgm/dV_{gs}|$ of U-FinFETs begins to increase again whereas, the $g_m$ decreases after achieving the maximum. Thus considering Eq. 5.1 again the HD2 of U-FinFETs begins to increase again. However, as the value of $g_m$ at higher temperatures is lower and $|dgm/dV_{gs}|$ almost constant with temperature as in Fig. 6.5, the HD2 at higher temperatures slightly increases as per Eq. 5.1.

5. At $V_{gs} = \sim 1.2$ V, the $|dgm/dV_{gs}|$ of U-FinFETs reaches maximum representing onset of surface roughness scattering degradation dependent mobility which is independent of temperature [15]. Beyond this point both $|dgm/dV_{gs}|$ and $g_m$ decrease as observed in Fig. 6.5 resulting in almost constant HD2 as observed in Fig. 6.6.
The impact of temperature on HD2 characteristics is physically described as following. As the ambient temperature increases, the intrinsic carrier density in the silicon body increases resulting in enhanced subthreshold current. However, as the effective electric field in the channel increases, the scattering due to lattice vibration degrades the carrier mobility and begin to reduce the enhancement in $I_{ds}$ due to the higher intrinsic carrier density. The presence of underlap to some extent retains the advantage of high intrinsic carrier density and prevents rapid HD2 degradation. In order to better understand the impact of mobility degradation the HD3 characteristics is analysed in details since it traces the variation in various mobility degradation mechanisms [12] [13] [18].

Fig. 5.6: Variation of 2nd order harmonic distortion (HD2) of U-FinFETs with gate voltage, $V_{gs}$ for increasing temperature at drain voltage, $V_{ds} = 1.0$ V.

Fig. 6.7: Variation of total harmonic distortion (THD) of U-FinFETs with gate voltage, $V_{gs}$ for increasing temperature at drain voltage, $V_{ds} = 1.0$ V.
The HD3 for the device as a function of $V_{gs}$ is presented in Fig. 6.8 and is analysed considering the effective carrier mobility in the device. The effective carrier mobility ($\mu_{UF}$) of U-FinFETs is specified by the resultant of effective mobility in the underlap ($\mu_{ul}$) and the channel ($\mu_{ch}$) region. From Matthiessen’s rule, the effective mobility is represented by:

$$\frac{1}{\mu_{UF}} = \frac{1}{\mu_{ul}} + \frac{1}{\mu_{ch}}$$

(6.1)

Both $\mu_{ul}$ and $\mu_{ch}$ are individually the summation of contributions from coulomb, phonon and Surface roughness scattering dependent mobility and are given by Eq. 5.6 and 5.7, respectively [12].

![Fig. 6.8: Variation of third order harmonic distortion (HD3) of U-FinFETs with gate voltage, $V_{gs}$ for increasing temperature at drain voltage, $V_{ds} = 1.0$ V.](image)

Now, in the HD3 characteristics of U-FinFETs, there are three separate minima representing the transition between different mobility degradation mechanism [12] [13]. The first minimum in Fig. 6.8 represents the transition from $\mu_{ch}^{\text{co}}$ to $\mu_{ph}^{\text{ch}}$. The second minimum corresponds to transition from $\mu_{ul}^{\text{co}}$ to $\mu_{ph}^{\text{ul}}$ whereas; the third minimum represents transition form $\mu_{ph}^{ch}$ to $\mu_{sr}^{ch}$. At low $V_{gs}$ the channel and underlap mobilities are dependent on bulk scattering dependent mobility $\mu_{ch}^{\text{co}}$ and $\mu_{ul}^{\text{co}}$, respectively. On gradually increasing $V_{gs}$ the channel region begins to invert while the underlap remains depleted. The onset of inversion in the channel region results in first minimum corresponding to transition from $\mu_{ch}^{\text{co}}$ to $\mu_{ph}^{ch}$.
Fig. 6.9: The impact of temperature on electron mobility as a function of effective field [25]. The arrow represents the trend of phonon scattering dependent mobility initiation with increasing temperature.

At higher operating temperatures the effective intrinsic carrier density is more resulting in an early onset of lattice scattering dependent degradation and corresponding mobility $\mu_{ph}^{ch}$ as illustrated in Fig. 6.9 [15]. As a result of this early onset of lattice scattering dependent degradation at high temperature, the first minima shift towards the lower $V_{gs}$ as observed in Fig. 6.8. It is also observed that due to increase in intrinsic carrier density with temperature, the HD3 is greatly reduced before first minima. However, beyond the first minima the HD3 reduction decreases due to onset of acoustic phonon scattering dependent mobility degradation.

When $V_{gs}$ is increased further, a secondary minimum is observed for $\mu_{coul}^{ul}$ to $\mu_{ph}^{ul}$ transition. However, under high $V_{ds}$, the sharpness of the secondary minima diminishes at the onset of transition between $\mu_{coul}^{ul}$ and $\mu_{ph}^{ul}$ due to extremely low inversion charge in the underlap region. It is also observed that under low $V_{ds}$ the secondary minimum is absent as observed in Fig. 6.10. The minimum is absent since, the underlap is not depleted and carrier mobility in underlap is dominated by $\mu_{coul}^{ul}$ only. Whereas, in the channel region due to low $V_{ds}$, $\mu_{coul}^{ch}$ to $\mu_{ph}^{ch}$ and $\mu_{ph}^{ch}$ to $\mu_{sr}^{ch}$ the transition occurs quickly and dominate the overall device mobility as per Eq. 5.7. The secondary minima is sharp for intermediate values $V_{ds}$ only where, the carrier mobility in underlap is initially dominated by $\mu_{coul}^{ul}$ and become $\mu_{ph}^{ul}$ dominated when $V_{gs}$ approaches $V_{ds}$ [12][13].
Fig. 6.10: Variation of third order harmonic distortion (HD3) of U-FinFETs with gate voltage, $V_{gs}$ for increasing temperature at drain voltage, $V_{ds}$ = 0.05 V.

Now, with increasing $V_{gs}$ the HD3 at high temperatures keeps on increasing due to mobility degradation in the channel region. As a result, beyond a certain $V_{gs}$ the HD3 at high temperatures becomes more than that at lower temperatures as observed in Fig. 6.8. As the $V_{gs}$ is further increased a tertiary minima is observed corresponding to transition from $\mu_{ph}^{ch}$ to $\mu_{sr}^{ch}$ in the channel region. It is observed that the tertiary minima shift towards lower $V_{gs}$ with increasing temperature although high temperature has negligible impact on surface roughness dependent mobility. It is observed by comparing Fig. 6.8 and 6.10 that the shift in minimum for $\mu_{ph}^{ch}$ to $\mu_{sr}^{ch}$ transition occurs only under high $V_{ds}$ that is explained as follows.

Fig. 6.11: The impact of high temperature on carrier drift velocity as a function of effective field [29]. The arrow represents the trend of drift velocity variation with increasing temperature.
As under high drain bias condition the underlap region is under depletion, the carrier transport is dominated by drain bias and temperature controlled drift velocity. It has been established earlier that with increasing temperature the drift velocity ($v_d$) decreases as illustrated in Fig. 6.11 [19] [20]. As a result of this reduced drift velocity the surface interactions increase and the mobility degradation due to surface roughness shifts to a slightly lower gate bias as in Fig. 6.8 indicating early onset of $\mu_{\text{ch}}$ to $\mu_{\text{sr}}$ transition.

**B. Effects of Temperature on HD of amplifier circuit**

In this section, the impact of temperature on distortion characteristics of U-FinFET-cascode amplifiers is analyzed. A typical cascode amplifier circuit used for analysis of U-FinFETs is same as presented in Fig. 5.11. For circuit analysis, the load resistance, $R_L$ of 10 kΩ is used, the supply voltage, $V_{dd}$ is maintained at 1.0 V and the bias voltage, $V_{bias}$ is fixed at 0.5 V. The value of $V_{bias}$ is selected such that it is near the zero temperature-coefficient (ZTC) point to achieve almost constant saturation current at any high temperature. The output characteristics of the cascode amplifier at different ambient temperatures are presented in Fig. 6.12. It is to be noted that for an amplifier, the region of importance is the dynamic region and is subject to distortion analysis [11].

The HD FOMs of the amplifier in the dynamic region of operation are extracted using IFM and are shown in Fig. 6.13 and Fig. 6.14.
Fig. 6.13: Variation of (a) total harmonic distortion (THD) and (b) second order harmonic distortion (HD2) for the cascode amplifier as a function of input voltage, $V_{\text{in}}$ at different operating temperatures.

The THD of the cascode amplifier is dictated by the $HD2$ characteristics, similar to the HD characteristics of the U-FinFET devices. At any operating temperature, the minimum of $HD2$ as well as THD characteristics of the amplifier represents the Quiescent-point (Q-point) for the circuit. It is observed that the Q-point shifts to a lower value of $V_{\text{in}}$ at higher temperatures. However, it is also observed that the total distortion under high temperatures decreases as a result of high intrinsic carrier density that improves the gain of the circuit. The output current variations with temperature are illustrated from the $HD3$ plot in Fig. 6.14.

Fig. 6.14: Variation of third order harmonic distortion (HD3) for the cascode amplifier as a function of input voltage, $V_{\text{in}}$ under different operating temperatures. Inset presents a clear depiction of the two minima at 300 K temperature.
The first minimum in Fig. 6.14 is the point where the current starts to increase and represents $V_{th}$ of the devices. Whereas, the second minimum represents the point where the output current ($I_{out}$) begins to reach the M1 controlled saturation current of the amplifier.

6.4: CONCLUSION

In this chapter, the distortion characteristics of U-FinFETs are studied for the first time at high temperature conditions. The impact of high temperature on distortion characteristics is analysed considering the variations in carrier mobility. It is observed that, in the subthreshold region the distortion is minimized at high temperatures due to high intrinsic carrier density assisted improved conductivity. Whereas, at higher gate bias HD and linearity characteristics of U-FinFETs degrade significantly due to higher lattice vibration dependent scattering. However, the degradation in HD and linearity of U-FinFETs at high temperatures are restricted to some extent due to the presence of underlap which retains the increased intrinsic carrier density, and suppresses the impact of increased lattice vibration assisted mobility degradation in the channel region. Finally, it is inferred from the distortion analysis of the cascode amplifier that the Q-point shifts to a low gate bias necessitating the need for compensating circuits to meet the desired design specifications.
REFERENCES:


