CHAPTER 5

LINEARITY AND DISTORTION ANALYSIS: IMPACT OF STRUCTURAL ADAPTATION
5.1: INTRODUCTION TO ANALOG/RF APPLICATION RELIABILITY OF MODIFIED MOSFETS

In previous chapters it is inferred that slight structural modification such as spacer engineering and channel material modification such as use of strained silicon channel can significantly improve the analog/RF performance of MOSFETs. However, for reliable circuit implementation these modifications are required to be assessed for their impact on the inherent issue of nonlinearity which introduces harmonic distortion. The impact of channel material modification on the distortion characteristics has been analyzed earlier [1]. In this chapter introduction to some basic structural modifications and their impact on the linearity and distortion characteristics are analyzed based on physical description.

5.2: DISTORTION CHARACTERISTICS OF HIGH-K SPACER UNDERLAPPED MOSFETS

With the evolution of CMOS technology, the integration of RF, analog, and mixed-signal integrated circuits (ICs) for system on chip (SOC) application has become a feasible option. It is now conceived that the double gate MOSFET (DG-MOSFET) architecture provides an improved analog/RF performance than others [2]-[4]. However, this device suffers from the higher short channel effects (SCE) [4]. After rigorous experimental and analytical studies by several researchers, the symmetric underlap double-gate MOSFET (UDG-MOSFET) structure has been shown to offer superior device performance such as improved analog/RF performance [2] [5]-[9], reduced drain induced barrier lowering (DIBL) [8]-[11] and extrinsic capacitance [12]-[14] compared to the DG-MOSFETs. However, in the conventional UDG-MOSFETs, the on current ($I_{on}$) is considerably reduced due to the increase in the distributed channel resistance [9]. It is established earlier that the analog/RF performance of UDG-MOSFETs is improved by use of asymmetric underlap where only drain side underlap is retained and is described by AUDG-MOSFET [15]. Also, it is constituted that the low $I_{on}$ shortcoming of the UDG-MOSFETs can be further minimized by using high-$k$ spacers with improved analog/RF performance, where $k$ is the dielectric constant of the high-$k$ gate dielectric [16]. Thus, the UDG-MOSFETs with high-$k$ spacers are better suited for RF applications. Again, for RF implementation, it is crucial to study the various reliability issues such as harmonic
distortion (HD) [17]-[19] of the UDG-MOSFETs with high-\(k\) spacers. Therefore, it is necessary to analyze the impact of \(k\) of the high-\(k\) spacers on HD for high-\(k\) spacer UDG-MOSFETs and the associated circuits. Thus, the objective of this chapter is to study the effect high-\(k\) spacers on the HD of high-\(k\) spacer UDG-MOSFETs for reliable analog/RF performance of the UDG-MOSFETs. In order to achieve this objective, first of all, we have designed the UDG-MOSFET and AUDG-MOSFET device structures with high-\(k\) spacers. The typical spacer materials considered here are \(\text{SiO}_2\) with \(k = 3.9\), Nitride with \(k = 7.5\), \(\text{Al}_2\text{O}_3\) with \(k = 11.5\) and \(\text{HfO}_2\) with \(k = 22.5\). In this following sections, the effect of high-\(k\) spacers on HD due to the nonlinearity in the drain current (\(I_{ds}\)) of the high-\(k\) spacer UDG-MOSFET and AUDG-MOSFET and is presented as a function of \(k\). Then, the HD at the output of cascode and differential amplifier circuits designed with the high-\(k\) spacer UDG-MOSFETs and AUDG-MOSFETs is also investigated.

5.2A: SYMMETRIC UNDERLAP MOSFETS

5.2A.1: DEVICE ARCHITECTURE AND SIMULATION PROCEDURE

The UDG-MOSFET structure used for HD analysis is shown in Fig.1. The structural specifications of the device include silicon body thickness (\(t_{si}\)) of 16 nm and gate length (\(L_{gate}\)) of 45 nm with oxide thickness (\(T_{ox}\)) of 1.9 nm in accordance with the International Technology Roadmap for Semiconductors (ITRS) for RF and mixed signal applications [20]. The source/drain (S/D) lengths (\(L_{sd}\)) are maintained at 50 nm with 20 nm underlap length (\(L_{un}\)) from the S/D end near the gate to the nearest gate edge (S/D–G) as shown in Fig.1.

![Fig. 5.1: Cross section of an idealized UDG-NMOSFET with symmetric source/ drain underlap used for numerical device simulation; in Figure, \(L_{sd}\) and \(L_{un}\) are the source/drain length and spacer width, respectively; \(T_{si}\) is the body thickness; \(T_{ox}\) is the gate oxide thickness; and \(T_g\) is the gate height.](image)
In Fig. 5.1, a heavily doped n\textsuperscript{+} S/D with concentration of $10^{20}$ cm\textsuperscript{-3} and a lightly doped $(10^{15}$ cm\textsuperscript{-3}) silicon substrate are used for device analysis. The detailed device architecture of the UDG-MOSFETs with high-$k$ spacers for device simulation is reported elsewhere [16]. The simulation of UDG-MOSFETs with high-$k$ spacers are performed using two-dimensional numerical device simulation tool Sentaurus [21] with an optimized meshing strategy as described in [22] for accurate results. The physical device models including carrier mobility were calibrated with the experimental data for accurate device analysis [16, 23]. In this study, the density-gradient carrier transport model is used. The Shockley-Read-Hall (SRH) recombination and incomplete ionization models are included in simulation for active carrier lifetime and density, respectively. The Arora mobility model is used for the carrier mobility incorporating doping and temperature dependence [24]. For mobility degradation including ionized impurity scattering, Lombardi mobility model is incorporated [25].

The above device structure is biased appropriately to generate drain current, $I_{ds}$ versus gate to source voltage, $V_{gs}$ characteristics at an ambient temperature ($T$) of 300 K. The drain voltage ($V_{ds}$) for the simulations is fixed at 0.55 V. The simulated $I_{ds} - V_{gs}$ data are used for extracting the distortion characteristics. The distortion characteristics extracted by quasi-static transport are valid to analyze the impact of spacer $k$ on the UDG-MOSFETs up to the maximum frequency of $f_T/2$ under different gate and drain voltage pair [26]. Here, $f_T$ is the cut-off frequency of the device. The distortion characteristics are extracted by the Integral function method (IFM) [27]. In this method, the different integral functions are used to estimate the distortion. The integral functions used represent the deviation of the non-linear characteristics from linear characteristics. The analysis is performed as a function of the primary non-linear HD-figure of merits (FOMs) given by the total harmonic distortion (THD), the second order harmonic distortion (HD2), and the third order harmonic distortion (HD3). The non-linearity of the devices is, also, compared as a function of the third order intercept point (IP\textsubscript{3}).

\textbf{5.2A.2: Linearity Analysis of High-$k$ Spacer UDG-MOSFETs}

For devices in analog and RF circuits, the important criteria are to minimize the contribution of the higher-order harmonics, inter-modulation at the output, and HD of the circuit output associated with the device characteristics. These criteria can be
achieved by reducing the non-linearity in the device characteristics.

![Graph showing the third order harmonic and fundamental harmonic power equivalence point, IP3 of UDG-MOSFET at maximum gm point as a function of the dielectric constant, k of the high-k spacers.]

Fig. 5.2: The third order harmonic and fundamental harmonic power equivalence point, IP3 of UDG-MOSFET at maximum gm point as a function of the dielectric constant, k of the high-k spacers.

In this study, the linearity of the high-k spacer devices is evaluated as a function of IP3 of the drain current characteristics [28]. Figure 5.2 shows the variation of IP3 with spacer dielectric constant, k at the point of maximum transconductance, gm.

![Graph showing transconductance of UDG-MOSFET for different values of k starting from k = 3.9 corresponding to SiO2 spacer to k = 22.5 representing high dielectric constant spacer material versus Ids; where Ids is the drain current.]

Fig. 5.3: Transconductance of UDG-MOSFET for different values of k starting from k = 3.9 corresponding to SiO2 spacer to k = 22.5 representing high dielectric constant spacer material versus Ids; where Ids is the drain current.

It is observed from the values of IP3 that the UDG-MOSFETs become more linear for
increasing value of $k$. The increase in the linearity of the device characteristics with increasing $k$ can be explained from the $g_{m}-I_{ds}$ plot presented in Fig. 5.3. Since higher the degree of flatness of the $g_{m}$, greater is the linearity [28]. Therefore, from the $g_{m}-I_{ds}$ plot it is obvious that for high-$k$ spacer devices with higher flatness results in increased linearity.

### 5.2A.3: Harmonic Distortion Analysis of High-$k$ Spacer UDG-MOSFETs

In this section the HD performance of the high-$k$ spacer UDG-MOSFET devices and circuits are analyzed as a function of HD FOMs.

#### A. Effects of High-$k$ Spacers on Harmonics

The HD FOMs for the devices are extracted in decibels (dB) with 1V/V reference level [1]. The extraction is performed using IFM on the $I_{ds}-V_{GT}$, where $V_{GT}$ is the gate overdrive voltage defined by $V_{GT} = V_{gs} - V_{th}$. Where, $V_{th}$ is the threshold voltage of the device. It is known that with increase in the non-linearity, the device distortion becomes more and more dependent on the signal amplitude. So, a small value of ac signal amplitude ($V_{a}$) of about 50 mV is used for the IFM analysis [27]. Thus, the input gate voltage at a particular bias point is given by:

$$V_{G} = V_{GT} + V_{a} \sin (\omega t)$$

Where, $\omega$ is the angular frequency and $t$ is the time. The phase angle, $\omega t$ varies from 0 to $2\pi$. Since, our objective is to analyze the effect of high-$k$ spacer on harmonics, the other device parameters such as the S/D resistance ($R_{S/D}$) and the device width ($W$) are kept constant. The effect of high-$k$ spacers on HD FOMs of the UDG-MOSFET is described in the following subsections.

1) **Effect of high-$k$ spacer on HD2**: For the analysis and description of the HD characteristics with respect to the transconductance generation factor ($g_{m}/I_{ds}$), a simplified analytical expression for HD2 is considered for small values of $V_{a}$ and is given by [29]:

$$HD2 = \left( \frac{1}{2} \right) V_{a} (1/2g_{m}) (dg_{m}/dV_{GT})$$  \hspace{1cm} (5.1)
The variation of $HD_2$ as a function of $V_{GT}$ and $g_m/I_{ds}$ of UDG-MOSFETs with high-$k$ spacers are presented in Fig. 5.4.

![HD2 plots](image)

**Fig. 5.4:** $HD_2$ plots for different values of $k$ starting from $k = 3.9$ corresponding to SiO₂ spacers to $k = 22.5$ representing high dielectric constant spacer material: (a) $HD_2$ versus $V_{GT}$ and (b) $HD_2$ versus $g_m/I_{ds}$; here, $V_{GT}$ is the gate over drive voltage.

In Fig. 5.4, a significant reduction in $HD_2$ is observed at lower $g_m/I_{ds}$ corresponding to higher $V_{GT}$. This reduction can be explained as follows. From Eq. 5.1, the $HD_2$ is described by two components; the $g_m$ and the slope of $g_m$ vs. $V_{GT}$ characteristics. We know, from [30] that the $g_m$ for UDG-MOSFETs is expressed as:

$$g_m = \frac{\partial I_{ds}}{\partial V_{GT}} = \left( \mu_{eff} \frac{W}{L_{eff}} \right) \cdot (Q_s - Q_d) \tag{5.2}$$
Where, $L_{eff}$ is the effective channel length and the $Q_s$ and $Q_d$ are the inversion charges at the source and drain ends, respectively. From Eq. 5.2, $g_m$ is proportional to the effective carrier mobility, $\mu_{eff}$ and the difference in the S/D end charges, $(Q_s - Q_d)$. So, the value of $g_m$ for UDG-MOSFETs with high-$k$ spacers increases due to higher $\mu_{eff}$ and $(Q_s - Q_d)$ due to inversion charge enhancement in the underlap region [16]. However, the slope of $g_m$ differs at lower and higher overdrive voltages and is expressed as:

$$
\frac{\partial g_m}{\partial V_{GT}} = \frac{\partial^2 I_{ds}}{\partial V_{GT}^2} = \left( \frac{\mu_{eff} W}{L_{eff}} \right) \cdot \frac{\partial (Q_s - Q_d)}{\partial V_{GT}}
$$

(5.3)

Now considering Eq. 5.3 at lower $V_{GT}$, the slope, $\frac{\partial g_m}{\partial V_{GT}}$ is large due to higher $(Q_s - Q_d)$. While, at higher $V_{GT}$ it becomes very low and almost constant as $(Q_s - Q_d)$ becomes very small due to reduced influence of drain voltage. So, at higher $V_{GT}$ the $g_m$ dominates $HD2$ while at lower $V_{GT}$, the effect of increased $g_m$ is compensated by higher $\frac{\partial g_m}{\partial V_{GT}}$. Thus, at higher $V_{GT}$ and lower $g_m/I_d$ a reduction in $HD2$ is observed in Fig. 5.4 and, it becomes almost constant at lower $V_{GT}$. The minimum of the $HD2$ represents the point of maximum $g_m$ for the devices.

![Graph](image)

Fig. 5.5: Extracted $g_m$ and $\frac{\partial g_m}{\partial V_{GT}}$ for different values of $k$ starting from $k = 3.9$ corresponding to SiO$_2$ spacer to $k = 22.5$ representing high dielectric constant spacer material versus $g_m/I_d$.

The improvement in the distortion characteristics of UDG-MOSFETs by high–$k$ spacers can be further elucidated considering the carrier mobility variations in the devices. From Eq. 5.2 and 5.3, it can be observed that $g_m$ and $\frac{\partial g_m}{\partial V_{GT}}$ have a strong dependence on $\mu_{eff}$. The variation of $g_m$ and $\frac{\partial g_m}{\partial V_{GT}}$ as a function of $g_m/I_d$ is presented in Fig. 5.5. It can be
observed from Fig. 5.5 that with the increase in the value of \( k \) the value of \( \partial g_m/\partial V_{GT} \) also increases. This is due to the variation in the \( \mu_{\text{eff}} \) of the UDG-MOSFETs with increase in the value of \( k \). For better understanding the variation in mobility an elemental model for \( \mu_{\text{eff}} \) is considered and presented below [1]:

\[
\mu_{\text{eff}} = \mu_0/(1 + \theta V_{GT})
\]

(5.4)

Where \( \mu_0 \) is the low field mobility and \( \theta \) is the mobility degradation factor [1]. In Eq. 5.4, \( \theta \) is a complex parameter described by different underlying physical phenomena [31] [32].

It is obvious from Eq. 5.4 that \( \theta \) significantly influences \( \mu_{\text{eff}} \) of the devices. The essential factors that dominate \( \theta \) and hence \( \mu_{\text{eff}} \) are the Coulomb, phonon, and surface roughness scattering dependent mobilities [33]. These mobilities depend on the channel and the underlap inversion charge (\( Q_{\text{inv}} \)) variation due to the gate field and the high-\( k \) spacer controlled gate fringing field, respectively. However, it is difficult to visualize the effect of variation in \( k \), on these mobilities in \( HD2 \) due to its stronger charge dependence. The influence on \( HD2 \) manifests as a shift in the \( HD2 \) characteristics. In this study, the influence of the high-\( k \) spacer devices on these mobilities are analysed through the \( HD3 \) characteristic which interprets the variations in mobility, as discussed in following subsection.

2) Effect of high-\( k \) spacer on \( HD3 \): The \( HD3 \) of the devices can be represented by a simplified analytical expression:

\[
HD3 = (1/4)V_a^2 (1/6 g_m)(d^2 g_m/dV_{GT}^2)
\]

(5.5)

From Eq. 5.5 it can be perceived that the nature of \( HD3 \) is characterized mainly by \( d^2 g_m/dV_{GT}^2 \) which determines its minima [1]. The variation of \( HD3 \) as a function of \( V_{GT} \) and \( g_m/I_{ds} \) of UDG-MOSFETs with high-\( k \) spacers are presented in Fig. 5.6.

In Fig. 5.6, the minima represent the transitions between the Coulomb, phonon, and surface roughness scattering dependent mobilities. And, the shift in HD characteristics is due to the influence of high-\( k \) spacers on coulomb, phonon, and surface roughness scattering dependent mobilities. These phenomena, transition and shift, in \( HD3 \) characteristics are discussed in details subsequently. In the following discussion, first of
all the cause of HD3 minima is described, followed by, cause of shift in HD3 minima and finally, the cause of reduction in HD3 at minima for high-k spacers.

Fig. 5.6: HD3 plots for different values of \( k \) starting from \( k = 3.9 \) corresponding to SiO\(_2\) spacer to \( k = 22.5 \) representing high dielectric constant spacer material: (a) HD3 versus \( g_m/I_{ds} \); (b) HD3 versus \( V_{GT} \).

The effective mobility of carriers (\( \mu_{udc} \)) in the UDG-MOSFET is determined by the resultant of effective mobility in the underlap region (\( \mu_{ul} \)) and the effective mobility in the channel region (\( \mu_{ch} \)), and is represented by the Matthiessen’s rule as:
\frac{1}{\mu_{UDG}} = \frac{1}{\mu_{ul}} + \frac{1}{\mu_{ch}}

In the channel region, $\mu_{ch}$ for all the devices remains the same since the gate dielectric is SiO$_2$ and the body thickness is constant for all the devices. So, the $Q_{inv}$ in the channel region is constant. On the other hand, $\mu_{ul}$ in the underlap region is dependent on $Q_{inv}$ controlled by spacer engineering. As a result, $\mu_{UDG}$ is dependent, primarily, on $\mu_{ul}$. Now, $\mu_{ul}$ is represented by:

\frac{1}{\mu_{ul}} = \frac{1}{\mu_{coul}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}

Where, $\mu_{coul}$, $\mu_{ph}$, and $\mu_{sr}$ are mobilities due to coulomb, phonon, and surface roughness scattering, respectively. A similar representation can also be used for the $\mu_{ch}$, but it remains constant for the devices under consideration because the body thickness and the inversion layer under the gate due to SiO$_2$ gate dielectric are the same and thus, not focused upon presently.

The mobilities $\mu_{coul}$, $\mu_{ph}$, and $\mu_{ch}$ are controlled by the transverse electric fields in the channel and the underlap region. The transverse electric field in the channel region depends on gate field ($E_g$) whereas, in the underlap region, depends on the gate fringing fields ($E_f$) as shown in Fig. 5.7 and governs the mobility. Due to this $E_f$ the phenomenon of gate fringe-induced barrier lowering (GFIBL) is observed in the underlap region [34]. The barrier lowering in the underlap region assists in improving the carrier mobility in this region.

Fig. 5.7: Cross Section of an idealized UDG-NMOSFET with symmetric source/ drain underlap depicting the feedback of gate sidewall field ($E_f$) into the underlap region.
Now, the phonon scattering is an energy-dependent processes and the coulomb scattering is $Q_{\text{inv}}$ dependent [33]. Thus, from Fig. 5.8 [35], we find that initially, $\mu_{\text{eff}}$ is dominated by $\mu_{\text{coul}}$ and increases with $E_f$. For higher $E_f$ and corresponding $V_{GT}$ the $Q_{\text{inv}}$ increases; the $\mu_{\text{coul}}$ achieves a maximum and then $\mu_{\text{ph}}$ becomes dominant. This transition occurs due to valley repopulation at higher transverse fields [36]. The sharp transition from coulomb to phonon scattering at intersection of $\mu_{\text{ph}}$ and $\mu_{\text{coul}}$ (Fig. 5.8) results mobility alteration in both underlap and channel region producing the $HD3$ minimum. At this point, an increased mobility is observed, as coulomb scattering ceases and the phonon scattering effect is very less in the underlap region at different $V_{GT}$ and corresponding $E_f$.

![Fig. 5.8: Mobility versus effective electric field plots for $k = 3.9$ and 22.5 corresponding to SiO2 and high-$k$ dielectric material, respectively; plots show the impact of high-$k$ in reducing the coulomb and phonon scattering limited mobility compared to lower-$k$ materials; all plots are obtained for the same effective oxide thickness. [35].](image)

A similar minimum in $HD3$ is produced again for the $\mu_{\text{ph}}$ to $\mu_{\text{sr}}$ transition. From Fig. 5.8, it can also be observed that the $\mu_{\text{coul}}$ remains dominant for comparatively higher fields for high-$k$ material in correspondence to its low-$k$ counterpart or we can say that the $Q_{\text{inv}}$ required is more. Thus, the $HD3$ minima for high-$k$ shift to a higher overdrive voltage as observed in Fig. 5.6.
In Fig. 5.6 four separate minima can be noticed at different $V_{GT}$ as presented in Table 5.1. These minima correspond to the transition between coulomb, phonon, and surface roughness scattering dependent mobilities. The first minima correspond to the transition from $\mu_{coul}$ to $\mu_{ph}$ in the channel region. Since channel characteristics are same for all the devices, the minima occur at the same $V_{GT}$ and represent the point of maximum $g_m$. The subsequent two minima represent $\mu_{coul}$ to $\mu_{ph}$ transition in the underlap regions. In the source end, the $E_f$ is more in comparison to the drain end [16]. Thus, the second minimum is for the mobility change in the source end underlap region and the third for the drain end underlap region. For extreme case of high-$k$, the two minima almost merge together as the $E_f$ required is comparatively high and the coulomb scattering is overcome almost simultaneously in both the underlap regions. The fourth minimum corresponds to the $\mu_{ph}$ to $\mu_{sr}$ transition in the channel region. Since, the channel characteristics are the same for the devices and at higher $V_{GT}$ the effective channel length ($L_{eff}$) is $L_{gate}$ [16], the minima are expected at the same $V_{GT}$. But, a shift towards higher $V_{GT}$ is encountered for high-$k$ spacer devices. This is due to sluggish mobility degradation for high-$k$ spacers with $V_{GT}$. Since the correlation length ($L_c$) for the devices considered here is identical [33] the effect of surface roughness remains constant. The $Q_{inv}$ in the underlap is enhanced for the high-$k$ spacer resulting in delayed $\mu_{ph}$ to $\mu_{sr}$ transition [1].

The reduction in HD3 observed in Fig. 5.6 due enhance carrier mobility is described as succeeding. In Fig. 8, the mobility of high-$k$ material is less than the lower $k$ counterpart,
considering effective gate oxide thickness that produces equal $Q_{inv}$ [35]. However, in this study the high-$k$ and low-$k$ material spacer have same specification resulting in unequal $Q_{inv}$. The $Q_{inv}$ is higher for high-$k$ spacer material at a particular $V_{GT}$, due to higher fringing field line density that is fed back in to the underlap region. This improvement in $Q_{inv}$ has dual advantage. Firstly, it improves the bulk carrier mobility due to higher charge screening by the inversion layer. Secondly, it compensates the low carrier mobility for high-$k$, by improving the conductivity of inversion layer which behaves like two-dimensional electron gas (2DEG) [36], and is a function of carrier density and mobility. So, the underlap conductivity is more resulting in reduced HD as observed in Fig. 5.6 for $HD3$ at minima.

3) **Effect of high-$k$ spacers on THD:** For any devices, THD represents the contribution to distortion from all the harmonics. The major component of THD is $HD2$ which is followed distantly by $HD3$. Though, it is $HD2$ that dictates the THD, the $HD3$ becomes significant when the even harmonics are subdued or rejected. The variation of THD as a function of $V_{GT}$ and $g_m/|d_s|$ of UDG-MOSFETs with high-$k$ spacers is presented in Fig. 9. It is observed from Fig. 5.9 that the THD follows $HD2$ except at the minima where the presence of $HD3$ is recognized as $HD2$ is less. Thus, THD characteristics can be described essentially by $HD2$. So, it can be established from the THD, $HD2$, $HD3$ and $\mu_{UDG}$ characteristics that the high-$k$ spacer UDG-MOSFETs present us with a better distortion characteristic for analog and RF circuit applications.
Fig. 5.9: THD and HD2 plots for different values of $k$ starting from $k = 3.9$ corresponding to SiO$_2$ spacer to $k = 22.5$ representing high dielectric constant spacer material: (a) THD and HD2 versus $V_{GT}$ and (b) THD and HD2 versus $g_m/I_{ds}$. Inset in (b) clarifies the HD2 dominance of THD.

B. Effects of High-$k$ Spacer on HD of Circuits

The impact of high-$k$ spacer on the circuits under consideration is restricted to the change in $I_{ds}$ of the UDG-MOSFETs in the circuit with regards to input voltage ($V_{in}$). Here, $V_{in}$ is applied DC bias on which the ac small signal voltage ($V_a$) is superimposed to extract HD FOM by IFM. Since the dynamic region in the output characteristics of the circuit is critical, we have analysed this region only as described below:

1) Cascode Amplifier: The output characteristic of a typical two transistor UDG-MOSFET Cascode amplifier as a function of high-$k$ spacer is shown in Fig. 5.10.

The circuit of the cascode amplifier implement with the UDG-MOSFET is presented in Fig. 5.11. For the circuit, the load resistance, $R_L$ of 10 kΩ is used, the supply voltage, $V_{dd}$ is maintained at 0.55 V and the bias voltage, $V_{bias}$ is fixed at 0.6 V. The UDG-MOSFETs $M1$, with variable spacer $k$ and $M2$, with constant spacer $k$ of 7.5, are specified by $W$ of 1 µm and $L_{gate}$ of 45 nm.
Fig. 5.10: Output characteristics of cascode amplifier for different values of $k$ starting from $k = 3.9$ corresponding to SiO$_2$ spacer to $k = 22.5$ representing high dielectric constant spacer material.

Fig. 5.11: Circuit of cascode amplifier using the UDG-MOSFET. In Figure, $R_L$ is the load resistance, $V_{in}$ is the input voltage, $V_{dd}$ is the supply voltage, $V_{bias}$ is the bias voltage, $V_{out}$ is the output voltage and $I_{out}$ is the output current. M1 and M2 are the UDG-MOSFETs with variable spacer $k$ and with fixed spacer $k$ of 7.5 respectively.
The corresponding HD FOMs extracted using IFM in the dynamic regions are as presented in Fig. 5.12 and Fig. 5.13. Here, also, it can be found that THD follows HD2 except at the minima, where the influence of HD3 shows up. Also, the minima of HD2 correspond to the voltage of maximum gain.

![Graph](image1)

**Fig. 5.12:** THD2 versus $V_{in}$ for different values of $k$ starting from $k = 3.9$ corresponding to SiO$_2$ spacer to $k = 22.5$ representing high dielectric constant spacer material.

![Graph](image2)

**Fig. 5.13:** HD3 versus $V_{in}$ for different values of $k$ starting from $k = 3.9$ corresponding to SiO$_2$ spacer to $k = 22.5$ representing high dielectric constant spacer material.
It is observed from Fig. 5.13 that the minima for the high-\(k\) spacer MOSFET shift to a lower \(V_{in}\). This is because for higher \(k\) spacers with increase in \(V_{in}\) the current (\(I_{out}\)) ascends rapidly causing output voltage (\(V_{out}\)) to fall quickly. Thus, the maximum gain input voltage, which is at the mid of the dynamic region of operation, shifts to lower \(V_{in}\). The variations in the current can be explained from the HD3 plot. The first minimum corresponds to the point of maximum \(g_m\) of the devices where the current starts to increase; whereas, the second minimum represents the point in the dynamic region where current begins to reach the saturation.

2) Differential Amplifier: The HD FOMs for the three transistor differential amplifiers of the UDG-MOSFETs with high-\(k\) spacers are extracted from the common mode characteristics using IFM in the dynamic region. The UDG-MOSFET implemented differential amplifier is as presented in Fig. 5.14. For the circuit, the load resistance, \(R\) of 50 k\(\Omega\) is used and the supply voltage, \(V_{dd}\) is maintained at 0.55 V. The UDG-MOSFETs M1, M2 with variable spacer \(k\) and M3, with constant spacer \(k\) are specified by \(W\) of 1 \(\mu\)m and \(L_{gate}\) of 45 nm. The current across M1 and M2 represented by \(I_1\) and \(I_2\) are used to extract the HD FOMs.

![Circuit of the differential amplifier using the UDG-MOSFET in common mode operation.](image)

**Fig. 5.14:** Circuit of the differential amplifier using the UDG-MOSFET in common mode operation. In Figure, \(R\) is the load resistance, \(V_{in}\) is the input common mode voltage, \(V_{dd}\) is the supply voltage, \(I_{bias}\) is the bias current and \(V_b\) is the bias voltage. M1, M2 and M3 are the UDG-MOSFETs and \(I_1\) and \(I_2\) are the currents across M1 and M2 respectively.
The extracted HD data are shown in Fig. 5.15. In Fig. 5.15, the minimum value of HD corresponds to the point of maximum differential gain.

![HD Data Illustration](image)

**Fig. 5.15**: HD2 and HD3 for different values of \( k \) starting from \( k = 3.9 \) corresponding to SiO2 spacer to \( k = 22.5 \) representing high dielectric constant spacer material. Where Inset is the enlarged view of the HD2 depicting the shift for increasing spacer \( k \).

The HD2 of the circuit output is very low compared to HD3 due to the common mode rejection in the differential mode of operation as observed in Fig. 5.15. The HD2 is non-zero because of the non-linear device characteristics. Also, it can be seen from Fig. 5.15, and clarified in the HD2 inset, that the distortion for the high-\( k \) spacer devices shifts to a lower input common mode voltage. This affirms that the high-\( k \) spacer devices are better alternative for low power amplifiers.

### 5.2B: ASYMMETRIC UNDERLAP MOSFETS

#### 5.2B.1: DEVICE ARCHITECTURE AND SIMULATION PROCEDURE

The structural attributes of the AUDG-MOSFET structure considered here for the analysis is illustrated in Fig. 5.16. The structural description of the device is given by the silicon body thickness \( t_{si} \) of 16 nm and the gate length \( L_{gate} \) of 45 nm with an oxide...
thickness ($T_{ox}$) of 1.9 nm in accordance to the International Technology Roadmap for Semiconductors (ITRS) for RF and Mixed Signal application [20]. The source/drain (S/D) lengths are maintained at 50 nm. The Drain to Gate underlap length ($L_{un}$) is considered to be 20 nm after optimization, as stated in [15]. The n$^+$ S/D doping is $10^{20}$ cm$^{-3}$ with a low silicon body doping of $10^{15}$ cm$^{-3}$.

![Cross section of a DG MOSFET with asymmetric underlap (AUDG-MOSFET) used for numerical device simulation; in Figure, $L_{un}$ is the underlap length; $T_{si}$ is the body thickness; $t_{ox}$ is the gate oxide thickness; and $Tg$ is the gate height.](image)

The AUDG-MOSFET Device presented in Fig. 5.16 is simulated with the two-dimensional numerical device simulator Sentaurus [21] and for accurate results the meshing is optimized according to the strategy described in [22]. The simulator was calibrated with the experimental data [23] considering the carrier mobility as mentioned in [16]. For carrier transport in the device simulation Density-Gradient model is used. The active carrier lifetime and density is dictated by the Shockley-Read-Hall (SRH) recombination and the incomplete ionization models respectively. Beside this, the mobility degradation including ionized impurity scattering is determined by the Lombardi mobility model. The simulated device is used to extract the $I_d$ - $V_{gs}$ characteristic at an ambient temperature of 300 K where, $V_{gs}$ is the gate to source voltage. Subsequently, the data points of $I_d$ - $V_{gs}$ characteristics are used for extracting the distortion characteristics in a manner similar to presented in earlier section. In analysis of this device also IFM is employed for extracting the distortion characteristics and the linearity of the devices is compared considering the third order intercept point ($IP_3$) [27] [28].
5.2B.2: Linearity Analysis of High-k Spacer AUDG-MOSFETs

An analog/RF circuit design using MOSFET must ensure minimum intermodulation and higher-order harmonics at the output as mentioned earlier for UDG-MOSFETs. In addition to this, the HD of a circuit because of the device non-linearity should be nominal. Thus, the primary source of HD represented by the non-linear characteristics of the device must be reduced. It is corroborated here that by using high-

The linearity of the device is evaluated as a function of $IP_3$ which is the intercept point of the fundamental frequency and the third harmonic output power with respect to the input power [20]. The variation in $IP_3$ at the point of maximum $g_m$ for the AUDG-MOSFET with the increasing spacer dielectric is presented in Fig. 5.17.

![Graph showing variation in $IP_3$](image)

**Fig. 5.17**: Variation in the third order output power point of intercept, $IP_3$ for the asymmetric UDG-MOSFET at maximum $g_m$ point as a function of the spacer dielectric $k$.

It is observed that the linearity of the AUDG-MOSFET increases with $k$. This improvement in the linearity can be elucidated from the $g_m - I_d$ plot presented in Fig. 5.18.
It can be noted in Fig. 5.18, the flatness of the $g_m - I_d$ characteristics increases with the spacer $k$ resulting in reduced third order derivative of $I_d$. This causes an improvement in the linearity of the device [28]. Following this, it is studied how this improvement in the linearity influences the HD characteristics.

### 5.2B.3: HARMONIC DISTORTION ANALYSIS OF HIGH-K SPACER AUDG-MOSFETS

It is known that a linear device characteristic produces minimum HD in circuits. Thus the improved linearity of the AUDG-MOSFET with the high-$k$ spacer as observed in earlier subsection reduces the HD. In the present section, the reduction in the HD of the device and the circuit performance are analysed as function of HD FOMs along with the analog parameters $g_m$ and $I_d$. The device performance is evaluated in the first subsection and the circuit performance for the devices is analysed considering the cascode and the differential amplifier in the following subsection.

#### A. Effects of High-$k$ Device on Harmonics

The HD FOMs of the AUDG-MOSFET with high-$k$ spacer are extracted by implementing IFM on the $I_d - V_{gs}$ characteristics of the device. The HD is evaluated in decibels with 1V/V reference level [21]. The $I_d - V_{gs}$ characteristic is obtained from well calibrated TCAD simulations as mentioned in Chapter 2.
The distortion due to non-linearity of the device becomes increasingly dependent on the signal amplitude with increasing non-linearity. So, the ac signal amplitude ($V_a$) is considered very small, of about 50 mV for the IFM analysis here as well. Thus, at a particular bias point the ac signal superimposed input gate voltage ($V_{GS}$) is given by: $V_{GS} = V_{gs} + V_a \sin (\omega t)$ where, $\omega t$ varies from 0 to $2\pi$. In this study all other device parameters such as the S/D resistances ($R_{S/D}$), the device width ($W$) that also contributes to the HD, are kept constant so as to analyze the effect of high-$k$ spacer only.

In order to account for the variations in the HD characteristics, as a function of the transconductance generation factor ($g_m/I_d$), approximate analytical expressions for the $HD2$ and the $HD3$ are chosen as presented earlier in Eq. 5.1 and 5.5 for small $V_a$ [22]. The variation in $g_m$ of the AUDG-MOSFET with $V_{gs}$ as a function of the high-$k$ spacer is as presented in Fig. 5.20, and is vital for understanding the HD improvement.

![Graph](image.png)

**Fig. 5.20:** Extracted transconductance of the asymmetric UDG-MOSFET as a function of gate voltage, $V_{gs}$ for the spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$ at drain voltage, $V_{ds} = 0.55$ V.

The $THD$ and $HD2$, for the AUDG-MOSFET with high-$k$ spacer, as function of $V_{gs}$ and $g_m/I_d$ are as presented in Fig. 5.21 and 5.22 respectively and the position of minima are presented in Table 5.2. It is observed that the $THD$ follows the $HD2$ since it is the major distortion component, except at the minima where the distortion is governed by the $HD3$. The $HD3$ for the device as a function of $g_m/I_d$ is as presented in Fig. 5.23.
### Table 5.2: Position of Minima in HD2 and THD Characteristics

<table>
<thead>
<tr>
<th>Spacer k</th>
<th>$V_{gs}$ at minima for THD (V)</th>
<th>$g_m/I_d$ at minima for THD (V⁻¹)</th>
<th>$g_m/I_d$ at minima for HD2 (V⁻¹)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.9</td>
<td>0.63</td>
<td>4.18</td>
<td>4.18</td>
</tr>
<tr>
<td>7.5</td>
<td>0.715</td>
<td>3.27</td>
<td>3.27</td>
</tr>
<tr>
<td>11.5</td>
<td>0.78</td>
<td>2.8</td>
<td>2.8</td>
</tr>
<tr>
<td>22.5</td>
<td>0.865</td>
<td>2.39</td>
<td>2.39</td>
</tr>
</tbody>
</table>

The THD and the HD2 of the device are significantly reduced at lower $g_m/I_d$ corresponding to the higher $V_{gs}$, this can be explained as following. In the subthreshold region, both $g_m$ and the slope of $g_m - V_{gs}$ remain almost constant for the spacer $k$ variations. Therefore, considering Eq. 5.1, almost constant and high HD2 is observed in Fig. 5.21. At higher $V_{gs}$ however, the slope of $g_m - V_{gs}$ decreases with respect to the subthreshold region, but remains almost constant for the spacer $k$ variations and $V_{gs}$. While, the $g_m$ for the high-$k$ spacer AUDG-MOSFET is higher due to the charge enhancement in the underlap region [16].

![Fig. 5.21(a): Variation of total harmonic distortion of the asymmetric UDG-MOSFET as a function of gate voltage, $V_{gs}$ for the spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$ at drain voltage, $V_{ds} = 0.55$ V.](image)
Fig. 5.21(b): Variation of total harmonic distortion of the asymmetric UDG-MOSFET as a function of transconductance generation factor ($g_m/I_d$) for the spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$ at drain voltage, $V_{ds} = 0.55$ V.

So, from Eq. 5.1 again, the reduction in the HD2 at lower $g_m/I_d$ and higher $V_{gs}$ can be interpreted. The HD2 minimum is the point of maximum $g_m$ for the devices.

Fig. 5.22(a): Variation of 2nd order harmonic distortion (HD2) of the asymmetric UDG-MOSFET with gate voltage, $V_{gs}$ for the spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$ at drain voltage, $V_{ds} = 0.55$ V.
Fig. 5.22(b): Variation of 2nd order harmonic distortion (HD2) of the asymmetric UDG-MOSFET with transconductance generation factor ($g_m/I_d$) for the spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$ at drain voltage, $V_{ds} = 0.55$ V.

Fig. 5.23: Variation of 3rd order harmonic distortion (HD3) of the asymmetric UDG-MOSFET with transconductance generation factor ($g_m/I_d$) for the spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$ at drain voltage, $V_{ds} = 0.55$ V.

The HD of the AUDG-MOSFET is also characterized by a shift in the HD minima due to variation in $\mu_{eff}$ as described earlier for UDG-MOSFETs in Section 5.2B.3. Thus, HD3 of AUDG-MOSFETs are also required to be analysed in detail for reasoning the shift in the HD characteristics. The variation in $\mu_{eff}$ is comprehended from the plot of $g_m$ with $g_m/I_d$.
as in Fig. 5.24. In Fig. 5.24, it can be observed that the slope of $g_m$ with regards to $g_m/I_d$ increases for the higher–$k$ spacer device, foreseeing the variation in mobility. The effect of the mobility variations on the HD is discussed in detail as following.

An important parameter controlling the carrier mobility of a device is $\theta$ In Eq. 5.4, thus its characterization is crucial for the analysis. The $\theta$ for the device under the gate remains constant for the spacer $k$ variations, since the characteristics of the channel region under the gate are same as observed earlier for UDG-MOSFETs. The constituents that dominate $\theta$ and hence the associated mobility are the coulomb, the phonon and surface roughness scattering as described earlier. These constituents in turn are regulated by the variation in the spacer $k$, the gate fringing field and the underlap inversion charge ($Q_{inv}$).

![Figure 5.24: Extracted transconductance ($g_m$) of the asymmetric UDG-MOSFET with transconductance generation factor ($g_m/I_d$) for the spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$ at drain voltage, $V_{ds} = 0.55$ V.](image)

In this study the effective carrier mobility ($\mu_{AUDG}$) in the AUDG-MOSFET is specified by the resultant of effective mobility in the underlap ($\mu_{ul}$) and the channel ($\mu_{ch}$) region. The effective mobility by the Matthiessen’s rule is represented by:

$$\frac{1}{\mu_{AUDG}} = \frac{1}{\mu_{ul}} + \frac{1}{\mu_{ch}}$$

The $Q_{inv}$ in the channel region is constant due to SiO$_2$ gate dielectric for all the devices so, the $\mu_{ch}$ remains same. However, the $\mu_{ul}$ is dependent on the high–$k$ spacer controlled $Q_{inv}$ thus; $\mu_{AUDG}$ is $\mu_{ul}$ dependent. Now both $\mu_{ul}$ and $\mu_{ch}$ are individually the summation of
Contributions from coulomb, phonon and surface roughness scattering dependent mobility and are given by:

\[
\frac{1}{\mu_{ul}} = \frac{1}{\mu_{coul}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}
\]  \hspace{1cm} (5.6)

\[
\frac{1}{\mu_{ch}} = \frac{1}{\mu_{coul}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}
\]  \hspace{1cm} (5.7)

Here \( \mu_{coul} \) is the coulomb scattering limited mobility, \( \mu_{ph} \) is the phonon scattering limited mobility and \( \mu_{sr} \) is the mobility due to surface roughness scattering. The superscripts in Eq. 5.6 and 5.7 represent the corresponding regions. In each region, the mobility determining factors are controlled by the transverse electric field. The gate fringing field \( (E_f) \) controls the electric field in the underlap region while the channel field is controlled by the gate field \( (E_g) \) itself.

The mobility determining factors depend on the transverse electric field distinctively. While, phonon scattering is energy-dependent process and dominates at high fields, coulomb scattering is \( Q_{inv} \) dependent and dominates at low fields [33]. Thus in both underlap and channel regions the mobility is restricted by the coulomb scattering initially and then becomes phonon scattering dependent for higher \( E_f \) and \( E_g \) that increases with the gate voltage.

![Figure 5.25: Variation of third order harmonic distortion (HD3) of the asymmetric UDG-MOSFET with gate voltage, \( V_{gs} \) for the spacer dielectric \( k \), varying from \( k = 3.9 \) to \( k = 22.5 \) at drain voltage, \( V_{ds} = 0.55 \) V.](image)
The coulomb scattering increases up to certain value of the transverse field beyond that it ceases as described earlier for UDG-MOSFETs in Fig. 5.8 [35]. This is due to increase in the $Q_{inv}$ with increasing $E_f$ and $E_g$. This transition from the coulomb to the phonon scattering (Fig. 5.8) manifests itself as HD3 minima. In Fig. 5.8 it is also observed that the required field for the transition from $\mu_{coul}$ to $\mu_{ph}$ is greater for the high-$k$ material. Thus, the minima of HD3 for the high-$k$ spacer AUDG-MOSFET also encounters a shift towards higher gate voltage as observed in Fig. 5.25.

Before proceeding, it must be pointed out in Fig. 5.8 that for different materials effective mobility is compared considering the effective oxide thickness (EOT) producing equal inversion charges [35]. On the other hand, in the AUDG-MOSFET, the $Q_{inv}$ in the higher $k$ spacers controlled underlap region is unequal because of equal spacer thickness and length. Since, the electric flux for the high-$k$ spacer at a particular high $V_{gs}$ is more in comparison to its low-$k$ counterpart, corresponding $E_f$ is more. So, the underlap $Q_{inv}$ is more resulting enhanced conductivity that dominates over reduced mobility due to high-$k$. As a result of this increased conductivity, HD at minima is reduced, as observed in Fig. 5.25 for HD3.

In the HD3 characteristics, three separate minima as illustrated in Table 2 can be recognized representing the mobility transitions mentioned earlier in this section in contrast to UDG-MOSFETs.

<table>
<thead>
<tr>
<th>Spacer $k$</th>
<th>$V_{gs}$ at 1st minima (V)</th>
<th>$V_{gs}$ at 2nd minima (V)</th>
<th>$V_{gs}$ at 3rd minima (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.9</td>
<td>0.35</td>
<td>0.545</td>
<td>0.77</td>
</tr>
<tr>
<td>7.5</td>
<td>0.35</td>
<td>0.635</td>
<td>0.885</td>
</tr>
<tr>
<td>11.5</td>
<td>0.355</td>
<td>0.68</td>
<td>0.97</td>
</tr>
<tr>
<td>22.5</td>
<td>0.355</td>
<td>0.72</td>
<td>1.195</td>
</tr>
</tbody>
</table>

The first minimum in Fig. 5.25 represents the transition from $\mu_{coul}^{ch}$ to $\mu_{ph}^{ch}$. Since at low $V_{gs}$ the channel mobility is determined by the $Q_{inv}$ controlled by $E_g$ which is equal for all the high-$k$ spacer variants and $E_f$ is small, the minima occur at the same $V_{gs}$ representing device threshold voltage ($V_{th}$). The secondary minima represent the transition from $\mu_{coul}^{ul}$.
to $\mu_{ph}^{\mu}$. This transition ensues at a higher $V_{gs}$ as it is dependent on $E_f$, strength of which increases with increasing $V_{gs}$. The increase in effective mobility because of this transition results in improved HD. The shift in the minimum for the high-$k$ spacer device is due to the higher required field for the mobility transition which is shown in Fig. 5.8. The tertiary minimum corresponds to transition from $\mu_{ph}^{ch}$ to $\mu_{sr}^{ch}$ at higher $V_{gs}$. Now, at high $V_{gs}$ and strong inversion the effective channel length ($L_{eff}$) is $L_{gate}$ [16] and dictates the effective mobility. Thus, the minima are expected at the same point however a shift towards higher $V_{gs}$ is encountered for the AUDG-MOSFET with high-$k$ spacer. This is due to the slower mobility degradation for the high-$k$ spacers with regards to $V_{gs}$. Since the correlation length ($L_c$) for the device under consideration is same [35] the effect of surface roughness is constant for the high-$k$ variants. The $Q_{inv}$ in the underlap is enhanced for the high-$k$ spacer resulting delayed $\mu_{ph}^{\mu}$ to $\mu_{sr}^{\mu}$ transition [33]. So, form the HD3 and $\mu_{AUDG}$ characteristics, it is established that the AUDG-MOSFET with the high-$k$ spacer has improved distortion characteristic. In the ensuing subsection, the influence of the AUDG-MOSFET with high-$k$ spacer is analysed as function of the HD FOMs in analog circuits.

B. Effects of High-$k$ Device on HD of Circuits

The circuits designed using the AUDG-MOSFET with high-$k$ spacer significantly improves the circuit performance. The performance is improved due to higher currents at a particular input voltage ($V_{in}$) for high-$k$ spacers and improved linearity. The circuit performance is analysed here for the distortion characteristics, in the dynamic region of operation, and presented as below.

1) Cascode Amplifier: In this subsection, a Cascode amplifier designed using the AUDG-MOSFET is analysed for its distortion characteristics as a function of the spacer-$k$. The circuit of the cascode amplifier implement with the AUDG-MOSFET is same as presented in Fig. 5.11 where the UDG-MOSFETS are replaced with AUDG-MOSFETs. For the circuit, the load resistance, $R_L$ of 10 kΩ is used, the supply voltage, $V_{dd}$ is maintained at 0.55 V and the bias voltage, $V_{bias}$ is fixed at 0.5 V. The AUDG-MOSFETs M1, with variable spacer k and M2, with constant spacer k of 7.5, are specified by $W$ of 1 µm and $L_{gate}$ of 45 nm. In Fig. 5.26 the output characteristics of the cascode amplifier with varying spacer-$k$ is presented.
Fig. 5.26: Output characteristics of the cascode amplifier designed with the asymmetric UDG-MOSFET for the spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$. In Figure $V_{out}$ is the output voltage, $V_{in}$ is the input voltage and $I_{out}$ is the output current.

<table>
<thead>
<tr>
<th>Spacer $k$</th>
<th>$V_{in}$ at minima for THD (V)</th>
<th>$V_{in}$ at minima for HD2 (V)</th>
<th>$V_{in}$ at minima for HD3 (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$1^{st}$ minimum</td>
<td>$2^{nd}$ minimum</td>
<td></td>
</tr>
<tr>
<td>3.9</td>
<td>0.34</td>
<td>0.35</td>
<td>0.32</td>
</tr>
<tr>
<td>7.5</td>
<td>0.335</td>
<td>0.34</td>
<td>0.31</td>
</tr>
<tr>
<td>11.5</td>
<td>0.325</td>
<td>0.335</td>
<td>0.305</td>
</tr>
<tr>
<td>22.5</td>
<td>0.32</td>
<td>0.33</td>
<td>0.3</td>
</tr>
</tbody>
</table>

The HD FOMs of the amplifier in the dynamic region of operation extracted using IFM are as depicted in Fig. 5.27 and Fig. 5.28. The position of minima for the HD FOMs is summarized in Table 5.4.
Fig. 5.27: Variation of total harmonic distortion (THD) and second order harmonic distortion (HD2) for the cascode amplifier as a function of input voltage, $V_{in}$ with the spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$.

The $HD2$ dictates the THD in the cascode amplifier, similar to the device HD characteristics, except at the minima where the influence of $HD3$ shows up. The minimum of $HD2$ for the devices represents the voltage of maximum gain. It can be observed that the minima for the high-$k$ spacer MOSFET shifts to a lower $V_{in}$.

Fig. 5.28: Variation of third order harmonic distortion (HD3) for the cascode amplifier as a function of input voltage, $V_{in}$ with the spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$. 
This is because the current ($I_{out}$) ascends rapidly with increase in $V_{in}$ for higher $k$ spacers causing output voltage ($V_{out}$) to fall quickly. The output current variations can be illustrated from the HD3 plot. The first minimum in Fig. 5.28 is the point where the current starts to increase and represents $V_{th}$ of the devices. The second minimum represents the point in the dynamic region where the current begins to reach the saturation current of the amplifier.

2) Differential Amplifier: In this subsection, differential amplifiers designed with high-$k$ spacer AUDG-MOSFET is analysed for HD. The AUDG-MOSFET implemented differential amplifier is same as presented in Fig. 5.14 where, UDG-MOSFETs are replaced with AUDG-MOSFETs. For the circuit, the load resistance, $R$ of 50 kΩ is used and the supply voltage, $V_{dd}$ is maintained at 0.55 V. The bias voltage, $V_b$ is fixed at 0.5 V and the bias current, $I_{bias}$ is 43.2 μA. The AUDG-MOSFETs M1, M2 with variable spacer $k$ and M3, with constant spacer $k$ are specified by $W$ of 1 µm and $L_{gate}$ of 45 nm. The current across M1 and M2 represented by $I_1$ and $I_2$ are used to extract the HD FOMs. The HD FOMs obtained from the common mode characteristic is presented in Fig. 5.29 and the positions of minima are tabulated in Table 5.5.

<table>
<thead>
<tr>
<th>Spacer $k$</th>
<th>$V_{in}$ at minima for HD2 (V)</th>
<th>$V_{in}$ at minima for HD3 (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.9</td>
<td>0.34</td>
<td>0.345</td>
</tr>
<tr>
<td>7.5</td>
<td>0.335</td>
<td>0.335</td>
</tr>
<tr>
<td>11.5</td>
<td>0.325</td>
<td>0.33</td>
</tr>
<tr>
<td>22.5</td>
<td>0.32</td>
<td>0.325</td>
</tr>
</tbody>
</table>

The minimum in the figure represents the point of maximum differential gain. In addition to that, because of common mode rejection the HD2 of differential amplifier is lesser than HD3, evident in Fig. 5.29. This illustrates that HD3 is the primary distortion component in differential amplifiers unlike the cascode amplifier and the total distortion is significantly reduced. It can be also observed that the distortion minimum for the high
$k$ spacer AUDG-MOSFET device shifts to a lower input common mode voltage indicating lower power consumption.

Fig. 5.29: Variation in the harmonic distortion for the differential amplifier as a function of input voltage, $V_{in}$ with the spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$.

5.3: DISTORTION CHARACTERISTICS OF DUAL MATERIAL GATE MOSFETS

In this section another important structural modification of MOSFETs is analysed for its impact on linearity and HD characteristics for RF circuit application reliability. This particular modification involves gate material engineering for performance improvement. Here, first a brief description about evolution of dual material gate technology in FinFETs including underlaps is described followed by its linearity and HD characteristics analysis.

5.3.1: INTRODUCTION TO DUAL MATERIAL GATE TECHNOLOGY EVOLUTION

The CMOS technology is being progressively used for analog and RF system on chip (SOC) applications owing to efficient scaling and improved performance [37]. In order to sustain the improvements, the CMOS devices are evolving structurally [37].
Consequently, the conventional MOSFET structure was replaced by silicon on insulator (SOI) technology paving the way for the present SOI FinFET technology with superior analog/RF performance [2] [38]. However, with increased scaling, the performance variability significantly increases due to random discrete dopant (RDD) effect. Therefore, the body of FinFETs is kept undoped or lightly doped [39] [40]. On the other hand, the use of undoped body significantly increases the short channel effects (SCE) and degrades gate control. Thus, optimized underlaps are used to isolate both source and drain in the FinFET devices and are described as the symmetric underlap FinFETs (SUFET) as mentioned in earlier sections [9]. The underlap in SUFETs is subsequently engineered to obtain superior analog/RF performance [8]. However, the use of the underlap on both source/drain (S/D) ends significantly reduces the on current ($I_{on}$) of SUFETs [34]. Hence, the source side underlap is eliminated and the drain side underlap is retained for improved performance. The devices with only drain side underlap, represented as the asymmetric underlap FinFETs (AUFET), presents superior analog/RF performance [15].

Although the device performance is significantly improved however, for sustaining efficient scaling, the AUFETs are modified to include Dual Material metal Gate (DMG) technology. The DMG technology, where a low workfunction metal (M2) and higher workfunction metal (M1) are used near drain and source respectively, has some inherent advantages such as improved SCE suppression and improved carrier transport efficiency [41]-[44]. The integration of DMG technology in AUFETs, represented as DMG AUFET devices, offers improved analog/RF performance and better scalability [45] [46]. However, for reliable analog/RF circuit design it is crucial to estimate the impact of DMG technology integration on the inherent reliability issues such as the linearity and the harmonic distortion (HD) of the CMOS devices [18] [19].

In the following sections a detailed analysis of the distortion characteristics of DMG AUFETs due to the non-linear drain current ($I_{ds}$) characteristics is presented as a function of increasing workfunction difference ($\Delta W$) and ratio of the metal lengths. Firstly, the device structure description and the simulation procedure for this analysis is presented, followed by the linearity analysis and, HD analysis in respective order.
5.3.2: Device Structure & Simulation Procedure for Dual Material Gate FinFETs

The structural details of DMG AUFET devices used for simulation are presented in Fig. 5.30. The structural attributes are described by the silicon fin thickness \((t_{si})\) of 16 nm, \(L_{gate}\) of 45 nm and oxide thickness \((T_{ox})\) of 1.9 nm with a drain side underlap [15] [46].

The fin height \((H_{Fin})\) is considered to be 65 nm [47]. The drain to gate underlap length \((L_{un})\) is considered to be 20 nm after optimization, as described in [15]. The \(n^+\) S/D doping of the device is \(10^{20}\) cm\(^{-3}\) and the silicon body is lightly doped with doping concentration of \(10^{15}\) cm\(^{-3}\). The \(L_{gate}\) of the structures is split into high workfunction metal, M1 and low workfunction metal, M2. The workfunction and length of M1 is represented by \(WF_1\) and \(L_1\) whereas, for M2 they are represented by \(WF_2\) and \(L_2\) respectively.

The DMG AUFET devices presented in Fig. 5.30 are simulated with the three-dimensional (3D) numerical device simulator Sentaurus [21]. For accurate and robust results, the meshing strategy is optimized as described in [22]. The simulator is calibrated with the experimental data [23] taking into account inversion charge dependent carrier mobility as described in [16] [46]. The device simulation is performed using Density-Gradient model for carrier transport. The active carrier lifetime and density are accounted by including the Shockley-Read-Hall (SRH) recombination and the incomplete ionization models respectively. The Lombardi mobility model is used for...
considering mobility degradation including ionized impurity scattering [25]. The device simulation is performed to generate $I_{ds}$-$V_{gs}$ characteristic for two different cases: 1) different WF2 with WF1 = 4.53 eV and L1=L2 =22.5 nm and 2) different L2 with WF2 = 4.1 eV, WF1 = 4.53 eV and fixed $L_{gate}$ as shown in Fig. 5.31 (a) and (b). Where, $V_{gs}$ is the gate to source voltage. The drain to source voltage, $V_{ds}$ is kept fixed at 1 V for the analysis. The simulated $I_{ds}$-$V_{gs}$ data are subsequently used for extracting and analysing the distortion characteristics of DMG AUFETs.

Fig. 5.31: The drain current ($I_{ds}$) of DMG AUFETs as a function of gate voltage, $V_{gs}$ for (a) increasing workfunction of M2 (WF2) with L1=L2 and (b) increasing L2 with WF2 = 4.1, WF1 = 4.53 and fixed $L_{gate}$.

In this study, the distortion characteristics of the DMG AUFETs are extracted by employing the Integral function method (IFM) [27]. The IFM estimates the deviation of the non-linear characteristics from the linear one and represents it in the form of different integral functions. For linearity analysis of the device the third order intercept point ($I_{IP3}$) is considered. For harmonic distortion analysis, the impact of different WF2 and L2 values are studied on the total harmonic distortion (THD), the second order harmonic distortion (HD2), and the third order harmonic distortion (HD3) introduce by the device.
5.3.2: Linearity Analysis of Dual Material Gate FinFETs

In this section the linearity characteristics of DMG AUFETs are analyzed for reliable analog/RF circuit design with minimum intermodulation and higher-order harmonics at the output. The prior analysis enables circuit designers to maintain nominal non-linear HD. The non-linear characteristics of devices vary with variations in the structural parameters and enables designers to minimize reliability concern. In this study, the linearity of the device is evaluated for variations in WF2 and L2 of the DMG AUFETs as a function of the intercept point between the fundamental frequency and the third harmonic output power defined as \( IIP_3 \) [28]. The \( IIP_3 \) of a device is inversely proportional to third order derivative of \( I_{ds} \) [28]. The variation in \( IIP_3 \) with \( \Delta W \) for different L2 of the DMG AUFETs at the point of maximum \( g_m \) for DMG AUFETs is presented in Fig. 5.32.

![Graph](image)

**Fig. 5.32:** Variation in the third order output power point of intercept, \( IIP_3 \) for increasing L2 in DMG AUFETs at maximum \( g_m \) point as a function of work function difference, \( \Delta W = WF1 – WF2 \).

It is observed from Fig. 5.32 that the linearity of DMG AUFETs increase with increasing work function difference, \( \Delta W = (WF1 – WF2) \) however, it degrades with increasing value of L2. This variation in the linearity is elucidated from the \( g_m - I_{ds} \) plots presented in Fig. 5.33.
Fig. 5.33: Transconductance ($g_m$) of DMG AUFETs with drain current ($I_{ds}$) for (a) increasing workfunction of M2 (WF2) with L1=L2 and (b) increasing L2 with WF2 = 4.1, WF1 = 4.53 and fixed $L_{gate}$.

It is observed in Fig. 5.33 (a) and (b) that the widening of the $g_m - I_{ds}$ characteristics, within $V_{gs}$ range of 0 V to 1.5 V, increases with increasing WF2 for fixed WF1 whereas it decreases with increasing L2 for fixed $L_{gate}$. As a result the third order derivative of $I_{ds}$ has lower value for higher WF2 that degrades the linearity of the devices on the other hand, vice versa occurs for larger L2 [28].

Fig. 5.34: Electric potential below oxide and silicon body interface in DMG AUFETs for (a) increasing workfunction of M2 (WF2) with L1=L2 and (b) increasing L2 with WF2 = 4.1, WF1 = 4.53 and fixed $L_{gate}$. 
The reduced widening for decreasing WF2 is physically attributed to step potential profile as shown in Fig. 5.34 that improves the carrier transport and assists rapid enhancement in $g_m$ with $I_{ds}$ [44]. Whereas, for increasing L2 the stepped potential profile remains the same however, the increased value of L2 introduces higher electric field in the channel region as shown in in Fig. 5.35 thus, the region of channel with acoustic phonon scattering limited mobility increases resulting in higher mobility degradation. The higher mobility degradation results in quicker reduction in $g_m$ with $I_{ds}$. In the following section, the influence of this linearity variation is studied on the HD characteristics of the device.

![Electric field below oxide and silicon body interface in DMG AUFETs for (a) increasing workfunction of M2 (WF2) with L1=L2 and (b) increasing L2 with WF2 = 4.1, WF1 = 4.53 and fixed Lgate.](image)

Fig. 5.35: Electric field below oxide and silicon body interface in DMG AUFETs for (a) increasing workfunction of M2 (WF2) with L1=L2 and (b) increasing L2 with WF2 = 4.1, WF1 = 4.53 and fixed Lgate.

### 5.3.2: Harmonic Distortion Analysis of Dual Material Gate FinFETs

The variation in the linearity characteristics of DMG AUFETs modulate the HD introduced in the circuits. The HD introduced decreases with increasing linearity and increases for lower linearity. Thus, it is necessary to analyze the HD of the devices with respect to variations in the device structure. The HD Characteristics of the device is analyzed as function of HD FOMs considering variations in analog parameters $g_m$ and $I_{ds}$. The HD FOMs of DMG AUFETs for variation in $\Delta W$ and L2 for fixed $L_{gate}$ are extracted by implementing IFM [27] on the $I_{ds}$ - $V_{gs}$ characteristics of the device as described earlier. For understanding the variations in the HD characteristics, approximate the same analytical expressions given by Eq. 5.1 and 5.5 are considered for
the HD2 and the HD3 [29]. The amplitude of the input sinusoid, $V_a$ is considered to be very small here as well [29].

The variation of $g_m$ and absolute value of change in $g_m$, $|d g_m/d V_{gs}|$ with $V_{gs}$ for DMG AUFETs as a function of $\Delta W$ and $L_2$ are presented in Fig. 5.36. In Fig. 5.37 the HD2 of DMG AUFETs for variation in $\Delta W$ and $L_2$ as a function of $V_{gs}$ are presented. The THD of devices for the variations is presented in Fig. 5.38. It is observed that the THD of the device follows the HD2 characteristics since, HD2 is major distortion component accounting for ~80% of THD. Thus, both THD and HD2 are described considering Eq. 5.1.

Fig. 5.36: Extracted transconductance of DMG AUFETs as a function of gate voltage, $V_{gs}$ for (a) increasing workfunction of M2 (WF2) with $L_1=L_2$ and (b) increasing $L_2$ with WF2 = 4.1, WF1 = 4.53 and fixed $L_{\text{gate}}$.

It is observed in Fig. 5.36 that both $g_m$ and $|d g_m/d V_{gs}|$ increase rapidly with $V_{gs}$ until $V_{gs} = \sim 0.3$ V thus considering Eq. 5.1 the HD2 of DMG AUFETs remain almost constant as observed in Fig. 5.37. However, the HD2 for lower value of WF2 and larger L2 is slightly lower due to higher $g_m$ that dominates the HD2 characteristics at low $V_{gs}$. When the $V_{gs}$ is increased further a minimum is observed in Fig. 5.37 at $V_{gs} = \sim 0.35$ V in the HD2 characteristics. This minima is due to sharp minima observed in Fig. 5.36 in $|d g_m/d V_{gs}|$ characteristics at $V_{gs} = \sim 0.35$ V and represents point of inflection for channel inversion below M2. At this point, $|d g_m/d V_{gs}|$ is very low and $g_m$ of DMG AUFETs is higher for lower value of WF2 and larger L2 thus, corresponding HD2 values are lower in accordance to Eq. 5.1. As the $V_{gs}$ is increased beyond the minimum, the $g_m$ of DMG
AUFETs keep increasing while $|d_{gm}/dV_{gs}|$ begins to decrease swiftly and reaches minimum value again at $V_{gs} \approx 0.7$ V. This results rapid drop in HD2 as per Eq. 5.1 and a minima is observed at $V_{gs} \approx 0.7$ V as shown in Fig. 5.37. The minima correspond to channel inversion below M1 and since entire channel below $L_{gate}$ is inverted, it represents the point of maximum $g_m$.

![Fig. 5.37: Variation of 2nd order harmonic distortion (HD2) of DMG AUFETs with gate voltage, $V_{gs}$ for (a) increasing workfunction of M2 (WF2) with L1=L2 and (b) increasing L2 with WF2 = 4.1, WF1 = 4.53 and fixed L_{gate}.](image)

It is observed that, with increase in $V_{gs}$ from $\approx 0.35$ V to 0.7 V there is only a slight decrease in HD2 for lower value of WF2 attributed to extremely small increase in $g_m$ once channel below M2 is inverted. However, for larger L2 since the $g_m$ is high due to inverted channel below M2 and low $|d_{gm}/dV_{gs}|$ due to shorter L1, the HD2 of DMG AUFETs is lower considering Eq. 5.1. Also, the minimum for larger L2 is shifted towards lower $V_{gs}$ due to quicker inversion channel below M1 since L1 is shorter. Now, as the $V_{gs}$ is increased again beyond 0.7 V the $g_m$ of DMG AUFETs begin to decrease and $|d_{gm}/dV_{gs}|$ increases as a result considering Eq. 5.1 again the HD2 of devices increase again as shown in Fig. 5.37. However, It observed from Fig. 5.36 (a) that for lower value of WF2 the $g_m$ remains high and $|d_{gm}/dV_{gs}|$ is low due to higher average electron velocity thus, the HD2 is lower as shown in Fig. 5.37 (a) [12]. It also observed from Fig. 5.36 (b) that for larger value of L2 the $g_m$ decreases and $|d_{gm}/dV_{gs}|$ is high due to higher field (Fig. 5.35 (b)) and corresponding mobility degradation below M2 thus, the HD2 is higher considering Eq. 5.1 as shown in Fig. 5.37 (b) [29]. The above analysis for HD2 is
applicable for THD as well since it follows HD2 except at the minima where HD3 become significant. Also, the HD3 of devices trace the variation in various mobility degradation mechanisms [26]. Thus it is necessary to analysis the HD3 characteristics to better understand the physical aspects of carrier transport in DMG AUFETs and impact of structural parameter variations.

In Fig. 5.38 the variation of HD3 as a function of $V_{gs}$ is presented for DMG AUFETs with decreasing value of WF2 and increasing value of L2. The effective carrier mobility ($\mu_{DMG}$) of the DMG AUFETs is specified by the resultant of effective mobility in the underlap ($\mu_{ul}$), the channel region below the gate M1 ($\mu_{ch1}$) and the channel region below the gate M2 ($\mu_{ch2}$). The effective mobility by the Matthiessen’s rule is represented by:

$$\frac{1}{\mu_{ul}} = \frac{1}{\mu_{ul}^{coul}} + \frac{1}{\mu_{ul}^{ph}} + \frac{1}{\mu_{ul}^{sr}}$$

$$\frac{1}{\mu_{ch1}} = \frac{1}{\mu_{ch1}^{coul}} + \frac{1}{\mu_{ch1}^{ph}} + \frac{1}{\mu_{ch1}^{sr}}$$

$$\frac{1}{\mu_{ch2}} = \frac{1}{\mu_{ch2}^{coul}} + \frac{1}{\mu_{ch2}^{ph}} + \frac{1}{\mu_{ch2}^{sr}}$$

All $\mu_{ul}$, $\mu_{ch1}$ and $\mu_{ch2}$ are individually represented by the summation of contributions from coulomb, phonon and surface roughness scattering degradation dependent mobility and are given by below expression as described earlier in Eq. 5.6 and 5.7 for underlap devices:

$$\frac{1}{\mu_{ul}} = \frac{1}{\mu_{ul}^{coul}} + \frac{1}{\mu_{ul}^{ph}} + \frac{1}{\mu_{ul}^{sr}}$$

$$\frac{1}{\mu_{ch1}} = \frac{1}{\mu_{ch1}^{coul}} + \frac{1}{\mu_{ch1}^{ph}} + \frac{1}{\mu_{ch1}^{sr}}$$

$$\frac{1}{\mu_{ch2}} = \frac{1}{\mu_{ch2}^{coul}} + \frac{1}{\mu_{ch2}^{ph}} + \frac{1}{\mu_{ch2}^{sr}}$$
Where, in each component on the right hand side, the subscript represents the degradation dependence and superscript represents the region.

![Diagram of the variation of third order harmonic distortion (HD3) of DMG AUFETs with gate voltage, $V_{gs}$](image)

Fig. 5.39: Variation of third order harmonic distortion (HD3) of DMG AUFETs with gate voltage, $V_{gs}$ for (a) increasing workfunction of M2 (WF2) with $L_1=L_2$ and (b) increasing $L_2$ with $WF_2=4.1$, $WF_1=4.53$ and fixed $L_{gate}$. The insets in the figures present an enlarged view of the third minima.

Now, in the HD3 characteristics of DMG AUFETs, there are four separate minima representing the transition between different mobility degradation mechanisms that were described in earlier sections and are as presented in Table 5.6.

The first minimum in Fig. 5.39 represents the transition from $\mu_{coul}^{ch_2}$ to $\mu_{ph}^{ch_2}$, the second minimum corresponds to transition from $\mu_{coul}^{ch}$ to $\mu_{ph}^{ch}$ at the interface of M1 and M2 where the effective workfunction is $WF = (WF_1 + WF_2)/2$ whereas; the third minimum represents transition from $\mu_{coul}^{ch_1}$ to $\mu_{ph}^{ch_1}$. The fourth minima represent the transition from $\mu_{ph}^{ch_2}$ to $\mu_{sr}^{ch_2}$. It may be noted from Fig. 5.39 that the position of second minima with respect to $V_{gs}$ remains constant since the electric field at the M1 and M2 interface remains constant with respect to structural variations considered thus, it is not focused upon. However the position of first, third and fourth minima are subject of interest as their positions with respect to $V_{gs}$ vary for the structural variations.
TABLE 5.6: POSITION OF MINIMA IN HD3 CHARACTERISTICS

<table>
<thead>
<tr>
<th>Structure Parameter</th>
<th>$V_{gs}$ at 1st minima (V)</th>
<th>$V_{gs}$ at 2nd minima (V)</th>
<th>$V_{gs}$ at 3rd minima (V)</th>
<th>$V_{gs}$ at 4th minima (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>WF1 = 4.53 eV, L1 = L2 = 22.5 nm</td>
<td>WF2 = 4.1 eV</td>
<td>0.3</td>
<td>0.375</td>
<td>0.415</td>
</tr>
<tr>
<td>WF1 = 4.53 eV, WF2 = 4.1 eV, L1 = Lgate – L2</td>
<td>WF2 = 4.1 eV</td>
<td>0.305</td>
<td>0.375</td>
<td>0.41</td>
</tr>
<tr>
<td></td>
<td>WF2 = 4.1 eV</td>
<td>0.31</td>
<td>0.37</td>
<td>0.405</td>
</tr>
<tr>
<td>L2 = 17.5 nm</td>
<td>L2 = 22.5 nm</td>
<td>0.31</td>
<td>0.37</td>
<td>0.405</td>
</tr>
<tr>
<td>L2 = 22.5 nm</td>
<td>L2 = 27.5 nm</td>
<td>0.3</td>
<td>0.375</td>
<td>0.415</td>
</tr>
<tr>
<td>L2 = 27.5 nm</td>
<td></td>
<td>0.24</td>
<td>0.375</td>
<td>0.425</td>
</tr>
</tbody>
</table>

It is observed from Fig. 5.39 (a) and (b) that with decrease in WF2 or with increase in L2 the first minima shifts towards lower $V_{gs}$ whereas the third minima shift towards higher $V_{gs}$; although the shift in third minima is insignificant. The shift in the minima for decreasing value of WF2 and for increasing L2 is described as follows. With decrease in WF2 and for increasing L2 the channel below the gate M2 inverts at a lower value of $V_{gs}$ due to higher effective field as observed in Fig. 5.35 as a result $\mu_{coul}^{ch2}$ to $\mu_{ph}^{ch2}$ transition occurs at lower $V_{gs}$. However, once the channel below the gate M2 is inverted the lateral drain field decreases below the gate M2 and increases slightly below the gate M1 as observed in Fig. 5.40 [45]. This increasing lateral field restricts inversion of the channel below M1 and correspondingly $\mu_{coul}^{ch1}$ to $\mu_{ph}^{ch1}$ transition shifts to higher $V_{gs}$ as observed in Fig. 5.39 (a) and (b). Now, for the fourth minima it is also observed Fig. 5.39 (a) and (b) that with decrease in value of WF2 the position of fourth minimum shifts to higher $V_{gs}$ whereas for increasing L2 it shifts towards lower $V_{gs}$. 

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Fig. 5.40: The lateral electric field in DMG AUFETs as a function of position along the channel for (a) increasing workfunction of M2 (WF2) with L1=L2 and (b) increasing L2 with WF2 = 4.1, WF1 = 4.53 and fixed Lgate.

This variation in position of fourth minimum is attributed to the variation in the average electron velocity. With decreasing WF2 the average electron velocity increases as the steepness of the step in potential profile increases [44]. This causes surface interactions to decrease and results in impeded $\mu_{ph}^{ch2}$ to $\mu_{sr}^{ch2}$ transition. Whereas, for larger value of L2 the steepness of the step in potential profile remains constant and the region of channel with high field increases as shown in Fig. 5.35 (b) causing higher surface interactions. The increased surface interaction facilitates the onset of surface roughness scattering dependent mobility and thus, $\mu_{ph}^{ch2}$ to $\mu_{sr}^{ch2}$ transition is shifted to lower $V_{gs}$.

5.4: CONCLUSION

This chapter presents a detailed analysis of the distortion characteristics of the high-\(k\) spacer UDG-MOSFETs and AUDG-MOSFETS considering the variations in the carrier mobility. Here the influence of the high-\(k\) spacer assisted gate side wall fringing field’s feedback on carrier mobility is examined and subsequently utilized to reason for the distortion characteristics. It is observed that the high-\(k\) spacers in UDG-MOSFETs and AUDG-MOSFET significantly influence the underlap carrier mobility by enhancing fringing fields. The enhanced mobility due to this field improves linearity of $I_{ds}$ and
reduces associated harmonics distortion. It is successfully inferred from above analysis that high-\(k\) spacers subjugate distortion for both UDG-MOSFETs and AUDG-MOSFETs improving reliability for RF applications. The distortion analysis is further extended to Cascode and differential amplifier circuits using the high-\(k\) spacer UDG-MOSFETs and AUDG-MOSFETs. It became evident from the analysis that high-\(k\) spacers not only reduce the circuit distortion but also the dynamic power as the maximum \(g_m\) shifts to a lower \(V_{in}\).

In this chapter the linearity and the distortion characteristics of DMG AUFETs for increase in work function difference and length of low workfunction metal gate M2 at the drain end of the device is also analysed. The analysis suggests that the linearity of the device significantly improves with decreasing values of workfunction, WF2 of M2 when all structural parameters are kept fixed. On the other hand, the linearity of devices degrades with increase in length of M2. The analysis also suggests that the distortion characteristics of the device improve with deceasing WF2 under all \(V_{gs}\). However, for increasing L2, the distortion of DMG AUFETs decreases under low \(V_{gs}\) and increases at higher values of \(V_{gs}\). The study infers that the improvement in linearity and distortion characteristics of DMG AUFETs is attributed to improved carrier transport efficiency as the average carrier velocity increases. Whereas, the degradation is attributed to increased high field induced surface roughness scattering in the channel below M2. Thus, it is concluded from the analysis that for reliable integration of DMG AUFETs for circuit applications, the values of WF2 and L2 for M2 must be optimized for high carrier transport efficiency and minimum surface roughness scattering induced degradation.
REFERENCES:


