CHAPTER 6

LOOK UP TABLE BASED APPROACH FOR RF PARAMETER EXTRACTION
6.1 INTRODUCTION

In this work, a look up table is developed to extract the intrinsic RF parameters of Underlap DG MOSFET including Non Quasi Static (NQS) effect. The look up table based approach proposed; can accurately extract complex RF parameters of UDG-MOSFET under different bias conditions, necessary for RF circuit simulations by an interpolation algorithm. The RF parameters including intrinsic gate to drain capacitance ($C_{gd}$), gate to source capacitance ($C_{gs}$), gate to drain resistance ($R_{gd}$), gate to source resistance ($R_{gs}$), gate to source transconductance ($g_m$), drain to source transconductance ($g_{ds}$), transport delay ($\tau_m$), capacitance due to DIBL ($C_{sdx}$) and inductance due to transport delay ($L_{sd}$), cut-off frequency ($f_T$) and maximum frequency of oscillation ($f_{max}$)are extracted using look up table approach. Parameters extracted using look-up table are compared with simulated data, considering NQS Effect, and are found in good agreement. For RF circuit applications a Low-Noise Amplifier (LNA) is designed, with the UDG-MOSFET, operating at a tuned frequency of 10 GHz.

6.2 LOOK UP TABLE APPROACH

The possibility of efficient scaling of device size in case of multigate MOSFET technology makes it very lucrative for circuit applications. These MOSFETs have also been established suitable for RF application nowadays as their cut-off frequency has reached gigahertz range [1]. This has been achieved because of proper modeling of parasitic elements associated with the device. These models are mainly based on quasi-static (QS) approximations that divide
the terminal currents into a static current function and a time derivative of charge function; both being functions of the input voltages and time. However, the Quasi-static approximations become inappropriate when the device operates close to its cut-off frequency [2]-[4]. The Non Quasi-static (NQS) and Extrinsic effects cannot be ignored in this frequency range. Although models have been proposed to determine the non-quasi-static (NQS) effects in RF range, these models are complicated, less accurate and time consuming with regards to parameter extraction. The requirement of accurate models for all the RF parameters especially parasitic capacitances and inductances further increases the complexity.

The look up table approach (LUT) [5]-[8] is an attractive alternative to the analytical modeling for circuit simulation with advanced device structures. The LUT is based on current and charge tables with large number of pre-extracted data serving as template [9], for accurate parameter extraction at unknown bias points by extrapolation/interpolations. Though, it requires a lot of time for creating such a table; the required effort for the later circuit simulations is greatly reduced. An important issue related to circuit simulation with advanced devices is; the leakage current in the subthreshold region.

This current contributes to significant power dissipation in low power circuits and requires complex models. LUT presents an efficient method for device characterization during circuit simulation in different regions of operation; these are represented by subthreshold, weak and strong inversion regions. It also simplifies switching from one region to another without the complexity of developing accurate models as implemented by Bourenkov et al. [10].

A novel LUT technique has been proposed by Rajesh A. Thaker et al. [11] to extract all the device parameters to an acceptable accuracy. However,
no such LUT has been developed for Underlap DG MOSFET for RF application accounting for NQS effect.

Integration of different interpolation technique in the table model creates a compromise and balance in simulation speed, accuracy and the memory requirements. The AC small signal parameters considered here are specified by intrinsic gate to drain capacitance ($C_{gd}$), gate to source capacitance ($C_{gs}$), gate to drain resistance ($R_{gd}$), gate to source resistance ($R_{gs}$), gate to source transconductance ($g_m$), drain to source transconductance ($g_{ds}$), transport delay ($\tau_m$), inductance due to transport delay ($L_{sd}$), cut-off frequency ($f_T$) and maximum frequency of oscillation ($f_{max}$) have been extracted using look up table approach and compared with simulated data.

The objective of this work is to design a LUT for extracting RF parameters to reduce time complexity of the system for the subsequent circuit simulations. To achieve this goal an Underlap DG MOSFET (UDG-MOSFET) has been designed according to the specification of the ITRS roadmap and simulated using 2D device simulator Sentaurus. AC simulation was performed under a wide range of biasing conditions varying from zero to an optimum bias point. In the following sections the device structure, simulation methodology, AC simulation and RF parameter extraction and LUT formation are described in order.

**6.3 Symmetric Underlap DGFET Device Descriptions**

Fig. 6.1 shows the cross-sectional view of the Symmetric Underlap DGFET (S-UnL). The device has the gate length ($L_{Gate}$) of 45 nm, oxide
thickness ($T_{ox}$) of 1.9 nm and silicon body thickness ($t_{si}$) of 16 nm in accordance with ITRS 2008 for RF and Mixed Signal application [12].

![Cross section of a DG MOSFET with source underlap and drain underlap lengths for UDG-NMOSFET devices.](image)

Fig. 6.1: Cross section of a DG MOSFET with source underlap and drain underlap lengths for UDG-NMOSFET devices.

The S/D–Gate underlap length ($L_{un}$) is 20 nm. The $n^+$ source/drain doping is $1 \times 10^{20} \text{ cm}^{-3}$ and silicon body is kept lightly doped (doping of $1 \times 10^{15} \text{ cm}^{-3}$). The lateral source/drain doping profile into the channel is given by $N_{sd}(x) = N_{peak} \exp(-x^2/\sigma^2)$ where $N_{sd}$ is the source/drain to channel doping concentration, $N_{peak}$ is the source/drain doping concentration, $\sigma$ is the lateral straggle determined by the fabrication procedure and is considered here to be 3 nm and $x$ represents the position from source/drain into the channel.

Molybdenum is used as gate material [13] [14]. In this work all the simulations are performed taking into account the Drift-Diffusion (DD) mode of carrier transport with Aurora mobility model that accounts for ionized impurity scattering and temperature dependency. The quantum corrections are incorporated for the simulation using density gradient quantization model [15]. The details of the entire simulation setup are described elsewhere [14].
Shockley-Read-Hall (SRH) recombination model and incomplete ionization model have been incorporated for determining the active carrier lifetime and density respectively. All the simulations are performed using 2-D device simulator [15] calibrated with the standard experimental data [16]. All the analog/RF parameters are extracted at different biasing points. Devices with various underlap lengths have been simulated and the performances of $I_{on}/I_{off}$ ratio have been measured using TCAD device simulator for optimization [17].

It is observed that the device achieves maximum $I_{on}/I_{off}$ for a symmetric source and drain underlap lengths of 20 nm each. This is due to the fact that when the length is smaller than the 20nm then the increase in $I_{off}$ is much larger than that in $I_{on}$ similarly when the length increases more than the 20nm then the decrease in $I_{off}$ is much smaller than that in $I_{on}$. Thus in the rest of the work 20 nm underlap length has been considered as the optimized length.

The UDG-NMOSFET device can be fabricated by following the steps for fabricating the standard FinFETs [18], with an additional step of introducing the underlap regions on the source and drain sides of the channel using tilt ion implantation technique [19].

Threshold voltage ($V_{th}$) of this device is 0.37V. In the following section we describe in details the steps leading to development of the intrinsic parameter LUT for subsequent circuit analysis. The flow of the work is as presented in Table 6.1.
6.4 AC SMALL SIGNAL PARAMETER EXTRACTION UNDERLAP DGFET

The first step in the process of LUT development is the extraction of the intrinsic parameter RF parameters by using AC small signal equivalent circuit (SSEC) model of the device as presented in Fig. 6.2, including the NQS effect [20]-[21]. The NQS effect, that describes the impact of frequency on the carrier mobility is modeled using inductor $L_{sd}$ and the transport delay dependent current source in the SSEC model of the device [3], [20], [22].
The parameter extraction is performed by Y-parameter analysis of the AC small signal model. Initially, Y-parameters have been extracted from the simulator under zero bias condition. The extrinsic capacitors $C_{gdo}$ and $C_{gs0}$ calculated using these extracted Y-parameters are represented as below.

$$C_{gdo} = -\frac{\text{Im}(Y_{21})}{\omega}$$

$$C_{gs0} = \frac{\text{Im}(Y_{11}) + \text{Im}(Y_{21})}{\omega}$$

The source and the drain extrinsic resistances, ($R_s$) and ($R_d$) are obtained using channel length method [20] and are shown in Fig. 6. 3.LUT is described in the following section.
In order to extract the values of intrinsic components of the device the extrinsic components extracted are de-embedded as described below [20], [23].

\[
[Y] - \begin{bmatrix}
  j\omega C_{gdo} + C_{gs} & - j\omega C_{gdo} \\
- j\omega C_{gdo} & j\omega C_{gdo}
\end{bmatrix} = [Y^{int}]
\]

\[
[Y^{int}] \Rightarrow [Z^{int}]
\]

\[
[Z^{int}] - \begin{bmatrix}
  R_I & R_s \\
  R_I & (R_s + R_I)
\end{bmatrix} = [Z^{int}]
\]

\[
[Z^{int}] \Rightarrow [Y^{int}]
\]

The Y-parameters thus extracted after de-embedding is given by \([Y^{int}]\) representing the intrinsic Y-parameter of the devices, which in details is reported in [20]. The intrinsic AC small signal model parameters in terms of \([Y^{int}]\) are tabulated in the Table 1 of Chapter 4. Utilizing the \([Y^{int}]\), the intrinsic RF parameters of the device are extracted for several, gate and drain, bias voltages. The extracted intrinsic RF parameters for the different bias voltage
are then used as LUT database. The LUT characteristics and the detailed description of extracting intrinsic RF parameters at unknown bias point using the developed

6.5 **LOOK UP TABLE APPROACH FOR RF PARAMETER EXTRACTION**

To understand the data extraction process from the LUT database developed, it is necessary to understand the characteristics of the LUT. The LUT here is basically a three dimensional (3-D) database comprising of three components: a dependent variable, which in this study is the intrinsic RF parameter (P) and two independent variables X and Y. Among the independent variables, the RF parameters are analyzed with respect to the independent variable, X and the extrapolation is carried out with respect to the independent variable, Y. In rest of the work, the plots represent P-X characteristics. Thus, the LUT contains optimally selected Y data, considering low memory requirement and accuracy, along with corresponding P and X data.

The extraction of data form LUT is primarily based on numerical interpolation and extrapolation techniques. The mainstay of the LUT development here is the interpolation technique. Interpolation methods are based on numerical differentiation, integration and PDE (partial differential equations) procedures. These methods include Lagrange Interpolation, Newton Interpolation, Hermite’s Interpolation, Rational Function Interpolation and Spine (Linear, Quadratic and Cubic). These methods establish important theory about polynomials and the accuracy of numerical methods that exhibit excellent techniques for drawing smooth curves. The basic purpose of the
interpolation method is to create data tables from few available data for drawing continuous, accurate curves maintaining the monotonicity of the data rapidly using optimal system memory. Different interpolation techniques that are used include, Linear Interpolation, Quadratic Interpolation and Exponential Interpolation.

Though, the discontinuous first derivatives and relatively large data table requirement for Linear Interpolation is considered as it’s a drawback but it is quite simple to implement. It also preserves the monotonicity of data and its accuracy can be easily controlled by the table density. Quadratic Interpolation is more accurate than linear interpolation due to better control over its first derivative. The accuracy of quadratic interpolation is further enhanced by using optimized LUT data density as higher data density will increase memory requirements. This technique is usually used to fit exponential data that agreeably maintains the monotonicity of exponential data. However, the drawback of this procedure is that it is slower than linear interpolation and there is no guarantee that the generated data by this method will be monotonic. In addition to that it is computationally very expensive, require large memory space and huge time for its calculations, and still there is a chance of having discontinuous first derivative. Depending on the nature of the curve and other requirements such that memory space, computational time, it may be necessary to use one or combined interpolation techniques.

As large number of data is available here, from large number of TCAD simulations, linear interpolation technique is used for parameter extraction from the LUT database. Here, the LUT is designed for the RF parameters of the UDG-MOSFET by Y-parameter analysis as described in Section III. A
good agreement has been found between data extracted from the TCAD simulations and the data extracted using the LUT.

6.6 LUT AND TCAD RESULTS COMPARISON

In this section the RF parameters extracted from the LUT and TCAD simulations are compared and explained in details. In order to understand the extracted characteristics simplified expressions for the conventional undoped symmetric DG-NMOSFETs are considered. The expressions for $g_m$ and the drain conductance ($g_d$) are as given by [24]:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \left( \frac{\mu W}{L_{eff}} \right) \cdot (Q_s - Q_d)$$

$$g_d = \frac{\partial I_{ds}}{\partial V_{gs}} = \left( \frac{\mu W}{L_{eff}} \right) Q_d$$

Where, $Q_s$ and $Q_d$ represent the source and drain end charges, respectively, $\mu$ is the effective mobility of the electrons and $W$ is the width of the device and considered as $Y$ data.
From the Eq. 4 it is evident that transconductance ($g_m$) is increasing with the increase of $Q_d$, hence it can be said that $1/g_d$ or value of output resistance ($r_0$) decreases with $Q_d$. It is observed from Fig. 6.4 that $r_0$ is decreasing with $V_{gs}$. From Eq. 3 it can be seen that becomes almost constant, thus as one move from moderate to strong inversion region, $g_m$ is almost constant. It is also evident from Fig. 6.4 that initially $g_m$ increases rapidly as the difference between source and drain end charge remain high. From the comparative analysis it can be concluded that good match has been found between LUT and simulated TCAD results.
Fig. 6.5: Comparison of LUT and TCAD results of the DG-NMOSFET for the variation of transconductance and output resistance with drain to source voltage at $V_{gs}=1V$, and $W=1\mu m$.

Fig. 6.5 shows the comparison of LUT and TCAD results for the variation of transconductance, $g_m$ and output resistance, $r_0$ with $V_{ds}$, where, device width is kept at $1\mu m$, when gate voltage is fixed at $1V$. It can be seen that $g_m$ and $r_0$ is increasing with $V_{ds}$ as it is function of drain to source voltage. Initially from subthreshold to moderate inversion region it is increasing rapidly and the value is getting almost constant as it reaches to the gate voltage. From Fig. 6.5 it is very clear that LUT results track the simulated TCAD results very closely.
Fig. 6.6: Comparison of LUT and TCAD results of the DG-NMOSFET for the variation of transconductance and output resistance with the width of the device at $V_{gs}=1V$, and $V_{ds}=1V$.

From expressions (3) and (4), it is observed that $g_m$ is directly proportional to the difference in S/D charge. Fig. 6.6 shows the variation of transconductance ($g_m$) and output resistance ($r_o$) with the width of the device ($W$), at $V_{ds} = V_{gs}=1V$ and $V_{gs}$ is considered as $Y$ data. From this plot it is evident that $g_m$ is increasing with $W$. The drain current ($I_D$) increases with $W$, thus $g_m$ increases.
Fig. 6.7: Comparison of LUT and TCAD results of the DG-NMOSFET for the variation of $C_{gs}$ and $C_{gd}$ with $V_{gs}$ at $V_{ds}=1\text{V}$, and $W=1\mu\text{m}$.

Fig. 6.7 shows the variation of $C_{gs}$ and $C_{gd}$ with gate to source voltage respectively where, $V_{ds}$ is considered as Y data. In this figure it is observed that both the capacitances are increasing with the $V_{gs}$ increase and as more charge enhancement is happening at source side for a fixed drain to source voltage and constant device width and there is good match between LUT and simulated results in the plots of Fig. 6.7.
In Fig. 6.8, the comparison of LUT and simulated TCAD result for variation of $C_{gs}$ and $C_{gd}$ with $V_{ds}$ at $V_{gs}=1V$, and $W=1\mu m$ is presented. In both the cases capacitance is decreasing with drain to source voltage as drain to source voltage is decreasing the inversion charge, hence, the capacitance is also decreasing. It is also evident that $C_{gs}$ is higher than $C_{gd}$ as charge accumulation is higher at source side. From the Fig. 6.8, it is evident that LUT results tracks TCAD results closely where, percentage of error is less than 3.
Fig. 6.9. Comparison of LUT and TCAD results of the DG-NMOSFET for the variation of $C_{gs}$ and $C_{gd}$ with $W$ at $V_{gs}=1V$, and $V_{ds}=1V$.

Fig. 6.9 shows the comparison between LUT and simulated TCAD result for variation of $C_{gs}$ and $C_{gd}$ with width of the device ($W$) respectively at $V_{gs}=V_{ds}=1V$. The Y data considered here is $V_{gs}$ and a good match between compared data is obtained. It is observed that with the variation of $W$, both the capacitances are as overlapped area is increasing and always the value of gate to source capacitance value is higher compared to the gate to drain capacitance as the inversion charge at the source side is higher and the capacitance is proportional to the charge. The cut-off frequency, $f_T$ and maximum frequency of oscillation, $f_{max}$ of the device extracted using the LUT are presented in Fig. 6.10(a) and (b) respectively. Here $W$ is the Y data and parameters are extracted at $W$ of 0.6$\mu$m. A close match between the LUT and TCAD simulated data is found with an error less than 0.5%.
Fig. 6.10. Comparison of LUT and TCAD simulated results of the DG-NMOSFET for the variation of (a) $f_T$ and (b) $f_{max}$ with $V_{gs}$. 
6.7 Low Noise Amplifier Design

For understanding the ease of using lookup table for circuit analysis a single-ended Low Noise Amplifier (LNA) [25] is designed here using the AC Small-Signal model of the UDG-MOSFET. The schematic diagram of the LNA circuit is shown in Fig. 6.11.

![Schematic view of the single-ended Low Noise Amplifier](image)

In the circuit, the UDG-MOSFET $M_3$ has a width of 0.2µm, whereas $M_2$ and $M_1$ have a width of 2µm. The source resistance, $R_S$ used for the circuits is 50 Ω. The gate inductor quality factor of 4.5 is selected so that it is independent of operating frequency variations. The UDG-MOSFET has been established as a power efficient architecture as it has its peak $f_T$ at a lower drain current [26]. For our LNA the operating frequency is fixed at 10GHz with a bias current of (1.2 mA) with optimum power budget for low power circuits at supply voltage, $V_{dd}$= 0.5V. The degenerating inductance $L_S$ is set to a value such that the real
Fig. 6.12: The variation of (a) Gain and (b) Noise Figure for LNA designed using the device as a function of frequency.

part of the output impedance remains at same value of 50 Ω for the circuit at the $f_T$ corresponding to fixed $I_d$ using Eqn. (5). Also, the gate inductance $L_g$ for the circuit is chosen from Eqn. (6) in a manner that the tuning frequency $F_0$ of the circuit is maintained at 10 GHz in accordance to the capacitance $C_{gs}$ of UDG-MOSFET $M_1$. Similarly, for the purpose of maintaining $F_0$ of 10 GHz,
the drain inductance $L_d$ has been fixed to 25 nH chosen according to the load capacitance $C_{load}$ of 10fF for all the circuits. The two resistances $R_{REF}$ and $R_{BIAS}$ are considered as 1 kΩ and 2 kΩ respectively.

$$L_S = R_S/(2\pi f_T)$$  \hspace{1cm} (5)  

$$L_g = 1/(2\pi F_O) - L_S$$  \hspace{1cm} (6)  

Now, the gain of the tuned LNA designed is extracted using the LUT and analyzed varying the $F_O$. The gain of the LNA circuit with UDG-MOSFET is as presented in Fig. 6.12(a). It is observed that the gain in maximum at the tuned frequency that decreases rapidly on increasing or decreasing the $F_O$ beyond $f_T$.

The LNA is subsequently analyzed for the minimum noise figure, $NF_{min}$ using Eq. (7). The values of the parameter $\gamma$, gate noise coefficient $\delta$ and correlation factor $\rho$ are selected as 2, 4 and 0.395 for short channel devices as suggested in [25].

$$NF_{min} \approx 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma \delta (1 - |c|^2)}$$  \hspace{1cm} (7)  

The cut-off frequency of the devices extracted using LUT is varied and the $NF_{min}$ for the circuit is obtained. The $NF_{min}$ for the circuit with UDG-MOSFET is shown in Fig. 6.12 (b) and it is observed that the $NF_{min}$ is least at the tuned frequency of the designed LNA that is fixed at 10GHz.
6.8 Conclusion

In this work a LUT for the UDG-MOSFET is developed considering NQS effect and a simplified LNA circuit is analysed using the developed LUT. It is evident from the analysis that the performance parameters extracted using the LUT matches the data from TCAD simulation with error less than 2% with maximum error of 7% for higher $V_{ds}$. It is also demonstrated that the LUT developed is effective for analyzing RF device performance considering NQS effect swiftly. Only the initial LUT development time is higher due to large number of required simulation to select the optimal data points for accurate interpolation of the unknown nodes. However, the circuit performance analysis using the LUT is limited by number of transistor as the error produced during the interpolation multiplies with every MOSFET stage decreasing the reliability of the circuit output. This error in the LUT data with regards to simulated data arise primarily due to mobility variation, carrier scattering and hot electron effects in the device, that can only be modelled by well-established transport models and are not considered by any interpolation algorithm. The LUT method described here is fast and efficient in comparing performance of devices without existing models.
6.9 REFERENCES


