4.1 INTRODUCTION

This work presents a systematic comparative study on effect of asymmetric spacer, on Analog/RF performance of Asymmetric Underlap (ASYM-UDL) Dual Material Gate (DMG) DG NMOSFETs. The asymmetric spacer in ASYM-UDL DMG DG NMOSFETs is proposed for the first time and the performance improvement of the device is compared with the Symmetry Underlap (SYM-UDL) DMG DG NMOSFET having symmetric spacer.

The performance of the devices is compared in relation to the analog/RF parameters, the on current ($I_{on}$), the transconductance ($g_m$), the transconductance generation factor ($g_m/I_d$), the intrinsic gain ($g_mR_o$), the intrinsic capacitances, the intrinsic resistances, the transport delay and the inductance. The analysis suggested that the average $I_{on}$, $g_m$, and $g_mR_o$, increases by 62.150%, 53.113% and 30.837% respectively compared to the SYM-UDL DMG DG NMOSFET.

4.2 ASYMMETRY UNDERLAP DMG DG NMOSFETS

There is an increasing demand for higher speed and lower power CMOS integrated circuits (IC) for system on chip applications. An important device in this regards is the Double Gate (DG) MOSFET. The DG-MOSFET device has also become lucrative for subthreshold analog/RF application because of low power consumption [1] [2].
Due to the exponential nature of the drain current \( (I_d) \) in the subthreshold region, the transconductance \( (g_m) \) is higher resulting in superior transconductance generation factor \( (g_m/I_d) \) and intrinsic gain \( (g_mR_o) \). Higher \( g_m \), \( g_m/I_d \) and \( g_mR_o \) improve analog amplifier performance with respect to power requirements. However, when DG-MOSFET device is rigorously downscaled, it suffers from short channel effects (SCE) [3] and drain induced barrier lowering (DIBL) [4].

To overcome the SCE and to reduce the DIBL in DG MOSFET an underlap is introduced. However, the underlap structure in DG MOSFETs increases the source to drain series resistance, \( (R_{SD}) \) [3] which results in lower on current \( (I_{on}) \). As the symmetry underlap (SYM-UDL) [5] reduces the \( I_{on} \) of the device, the asymmetry underlap (ASYM-UDL) is selected to reduce \( R_{SD} \) with only the drain side underlap.

The increase in \( R_{SD} \) is minimized further by the use of high k spacer material that enhances the fringing in the source/drain underlap region [6]. For further \( I_{on} \) improvement the dual material gate (DMG) is considered [1], [3], [4] and [7]. In the DMG structure source side metal \( (M_1) \) and the drain side metal \( (M_2) \) having different metal work-function are considered such that the work-function of \( M_1 \) is greater than \( M_2 \). Due to DMG structure, a step function [8] is formed in the potential along the channel which causes the average electron velocity to increase [9] [10], as the electrons are accelerated more rapidly.

In this work, analog/RF performances of ASYMU-DMG DG NMOSFET are studied for the first time for spacer k variation. The drain side underlap region has been optimized to be 20 nm and the spacer dielectric k is considered to be varying from \( k = 3.9 \) to \( k = 22.5 \). The source side spacer
dielectric, k is fixed at k = 7.5. The work function of M₁ is fixed at 4.7eV and for M₂ it is varied from 4.1eV to 4.5eV.

For analysis the analog parameters considered are the $I_{on}$, the transconductance ($g_m$), the transconductance generation factor ($g_m/I_d$), the intrinsic gain ($g_m R_o$). RF parameters are extracted using non-quasi-static (NQS) small signal equivalent circuit [11].have been extracted and compared with a similar SYMU DMG DG NMOSFET where good agreement has been observed. The channel doping profiles of a 45 nm U-DMG-DG NMOSFETs are optimized with the help of 2D numerical tool Sentaurus TCAD [12].

Different parameters such as the on current ($I_{on}$), the transconductance ($g_m$), the gain per unit current ($g_m/I_d$), the intrinsic gain ($g_m R_o$), the intrinsic capacitance, the intrinsic resistance, the transport delay, the inductance have been analyzed, which play major role in RF performance. Average $I_{on}$, $g_m$ and $g_m R_o$, have increased by 62.150%, 53.113% and 30.837% respectively, compared to the similar SYM-UDL DMG DG NMOSFET which suggests that it will be an ultralow power and superior device to work in RF domain.

4.3 DEVICE DESCRIPTION OF ASYM-UDL DMG DG NMOSFETS

The structure of SYM-UDL and ASYM-UDL DMG DG NMOSFET are shown in Fig. 4. 1(a) and (b) respectively. The technology parameters of the device have been chosen according to the ITRS 2008 for RF and Mixed Signal application [13]. For both SYM-UDL and ASYM-UDL DMG DG NMOSFETs the gate length ($L_g$), oxide thickness ($T_{ox}$) and silicon body thickness ($t_{si}$) have been chosen 45 nm, 1.9 nm and 16 nm respectively.
For SYM-UDL DMG DG NMOSFET both side underlap length ($L_{un}$) is 20 nm and for ASYM-UDL DMG DG NMOSFET drain side underlap length is 20 nm. The lightly doped silicon body is p-type with doping concentration of $10^{15}$ cm$^3$.

![Diagram](image)

**Fig. 4.1:** Cross section of a U-DMG-DG-NMOSFET with source underlap and drain underlap.

The source/drain doping is $10^{20}$ cm$^{-3}$ and to have a Gaussian profile in the channel, the lateral source/drain doping profile in the channel is given by $N_{sd}(x) = N_{\text{peak}} \exp \left( -x^2/\sigma^2 \right)$. Here, $x$ and $N_{sd}$ signifies the position from the source/drain into the channel and the doping concentration at point $x$ respectively, as shown in the Fig. 4.2. $N_{\text{peak}}$ is the source/drain doping concentration, $\sigma$, the lateral straggle, determined by the fabrication procedure is equal to 3 nm.

The simulations are performed considering Aurora mobility [12] model that incorporates ionized impurity scattering and temperature dependency. The quantum corrections are incorporated for the simulation using the density gradient quantization model.
Fig. 4.2: Gaussian doping profiles along the channel of the device in Fig. 4.1.

For determining active carrier lifetime Shockley-Read-Hall (SRH) recombination model has been incorporated. For the simulations, 2D device simulator Synopsys TCAD [12] has been used and calibrated with the standard experimental data [14]. To optimize the device performance, ASYM-UDL DMG-DG NMOSFET is compared with a SYM-UDL DMG-DG NMOSFET for analog performance. At the time of comparison between symmetry and asymmetry devices, nitride spacer has been used with gate work functions of $M_1=4.7\text{eV}$ and $M_2=4.1\text{eV}$.

Analog parameter has been extracted at different values of $V_{gs}$ and $V_{ds}$ accordance to ITRS 2008 [13]. For the RF performance of different ASYM-UDL DMG-DG NMOSFETs have been compared for different metal workfunctions of $M_2$, varying from $M_2=4.1\text{eV}$ to $M_2=4.5\text{eV}$, whereas $M_1$ is fixed at $4.7\text{eV}$ and the frequency is varied up to 100 GHz.

The optimized spacer material nitride, having $k=7.5$ has been used in the source side [15] and the drain side is varied with different spacer materials. For
the drain side typical spacer materials considered are SiO$_2$ with $k=3.9$, nitride with $k=7.5$ and HfO$_2$ with $k=22.5$. The ASYM-UDL DMG-DG NMOSFET device can be fabricated by the standard Fin-FETs [16] fabrication procedure with an additional step for the underlap regions using the tilt ion implantation technique [17]. The practicability of the device structure is being shown in [18].

4.4 Analog Performance of ASYM-UDL DMG DG NMOSFETs

The analog performances of the SYM-UDL and ASYM-UDL DMG-DG NMOSFETs have been compared and presented in this section. For the enhancement of the device performance, the analog parameters $I_d$, $g_m$, $g_m/I_d$ and $g_mR_o$ have been analyzed here. To figure out the effect of asymmetry underlap structure in DMG DG NMOSFET, the electron density and the electrostatic potential along the channel of the devices are being presented in Fig. 4.3 (a) and (b) respectively, at $V_{gs}$ of 0.55 V and 0.10 V.

It is clearly seen from the Fig. 4.3 (a) that the electron density is spread over the more regions along the channel along the X-axis for the ASYM-UDL device structure, because of not having the underlap region in the source side. It is also observed from the Fig. 4.3(b) that for the ASY-UDL DMG-DG NMOSFET device, an improvement in potential position along the channel in the X-axis. It is also observed that a step potential is being created along the channel at the interface of two different gate metal work-functions.
Fig. 4.3: Comparison of (a) Electron Density, (b) Electrostatics Potential along the channel of a 45-nm SYM-UDL DMGDG and ASY-UDL DMG-DG NMOSFETs, at $V_{ds}=0.10\text{V}$ and $V_{gs}=0.55\text{V}$. 
As shown in the Fig. 4.4, there is an increase of potential position along the channel for the ASY-UDL device, the drain current has been improved significantly both in the subthreshold and in the strong inversion region. The drain current has been increased by 62.150% in the strong inversion region.

![Comparison of the I\textsubscript{ds} for SYM-UDL DMGDG and ASY-UDL DMG-DG NMOSFETs as a function of V\textsubscript{gs}, at V\textsubscript{ds}=0.55V.](image)

The absence of source underlap region in ASY-UDL device reduces the on resistance that in turn improves the drain current of the device. As a result of improved drain current the transconductance, g\textsubscript{m} is rising both in the subthreshold region and in the strong inversion as observed from the Fig. 4.5. The transconductance has improved by 12.776% in the strong inversion. A small reduction in transconductance generation factor, g\textsubscript{m}/I\textsubscript{d}, is about 13.103% in the subthreshold regime at gate voltage is 0.15V is shown in the Fig. 4.5.

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Fig. 4.5: Comparison of the Transconductance, \(g_m\) and Transconductance Generation Factor, \(g_m/I_d\) for SYM-UDL DMGDG and ASY-UDL DMG-DG NMOSFETs as a function of \(V_{gs}\), at \(V_{ds}=0.55\)V.

However, it is the performance degradation of the device, still it shall not affect much as the power consumption is very less in this regime. It is observed from the Fig. 4.6 that intrinsic gain, \(g_mR_o\) has been increased by 47.659% at the gate voltage is 0.2V due to increased transconductance.

Hence, it is evident that ASYM-UDL DMG DG NMOSFET device’s performance gives remarkable improvement in the sub-threshold regime. For rest of the work, the different ASYM-UDL DMG-DG NMOSFETs have been compared for metal work-function \(M_1=4.7\)eV and \(M_2=4.1\)eV. At the same time source side spacer material, \(k\) is fixed at 7.5, whereas, the drain side spacer material is varied with SiO\(_2\), nitride and HfO\(_2\).
Fig. 4.6: Comparison of the Gain for SYM-UDL DMGDG and ASY-UDL DMG-DG NMOSFETs as a function of $V_{gs}$, at $V_{ds}=0.55\text{V}$.

Fig. 4.7: Comparison of the Gain and Output Impedance for ASY-UDL DMG-DG NMOSFETs as a function of $V_{gs}$, at $V_{ds}=1.0\text{V}$.
Fig. 4.8: Variation of Drain Current, \( I_d \) of the ASY-UDL DMG-DG NMOSFETs as a function of spacer dielectric \( k \), varying from \( k = 3.9 \) to \( k = 22.5 \) at \( V_{ds} = 0.55 \) V, \( V_{gs} = 1.1 \) V and frequency, \( f = 100 \) GHz.

It is observed from the Fig. 4.7 that due to the increase of the value of spacer dielectric, from \( k = 3.9 \) to \( k = 22.5 \), the intrinsic resistance increases as a result of improving the intrinsic gain of the device.

In this section, three different ASYM-UDL DMG DG NMOSFETs have been compared and the analog performances have been analysed in Fig. 4.8, Fig. 4.9 and Fig. 4.10. It is evident that the drain current is increasing with spacer dielectric, \( k \) and with the lower value of metal work-function \( M_2 \).
Fig. 4.9: Comparison of the Transconductance and Transconductance Generation Factor for ASYM-UDL DMG DG NMOSFETs as a function spacer dielectric $k$, varying from \( k = 3.9 \) to \( k = 22.5 \) at \( V_{ds} = 0.55 \text{ V}, V_{gs} = 1.10 \text{ V} \).

Due to the increase in the value of \( k \), \( I_{ds} \) of the device increases as drain side fringing field density through the high-\( k \) spacer material. As a result of high fringing field density, the potential barrier in that region reduces and it enhances the charge accumulation, this in turn improves \( g_m \) and \( g_m/I_{ds} \) [23].

It is also evident from the Fig. 4.8 that for the lower value of metal work-function \( M_2 \), the drain current enhances more as it increases the steepness of the step potential created in the conduction band along the channel.
Fig. 6.10: Comparison of the Gain and Output Impedance for ASY-UDL DMG-DGNMOSFETs as a function spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$ at $V_{ds} = 1.0$ V, $V_{gs} = 1.0$ V.

It is observed from the Fig. 4.9 that $g_m/I_{ds}$ is also improving in the strong inversion region with the variation of spacer dielectric $k$ as the improvement of $g_m$ is higher compared with $I_{ds}$. In the Fig. 4.10, the output resistance and the intrinsic gain are plotted as a function of $k$.

It is observed that as one move towards the higher $k$, the output resistance is decreasing and intrinsic gain is found to be increasing. With the increase of $k$, more charge enhancement takes place, therefore, source to drain conductance increases and output resistance decreases.
4.5 **AC SMALL-SIGNAL EQUIVALENT CIRCUITS**

Non Quasi Static (NQS) effect has been considered at the time of designing the small signal equivalent circuit for the proposed device shown in the Fig. 4.11[19]. The RF parameters have been extracted from the Y-parameter analysis of the AC small signal model. From the simulator, Y-parameters have been extracted at zero biased condition.

![AC Small-Signal Equivalnt Circuits](image)

**Fig. 4.11: AC Small-Signal Equivalent Circuits for ASY-UDL DMG-DG NMOSFET.**

The extrinsic gate-to-source/drain capacitances, $C_{gso}$ and $C_{gdo}$ have been calculated from the extracted Y-parameters at zero biased condition.

$$
C_{gdo} = -\frac{\text{Im}(Y_{11})}{\omega} \quad (3)
$$

$$
C_{gso} = \frac{\text{Im}(Y_{11}) + \text{Im}(Y_{21})}{\omega} \quad (4)
$$

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From the channel length method [19], the source and the drain resistances (R_s and R_d) have been extracted and the de-embedding step [19]-[22] has been followed as specified the step below.

\[
[Y] - \begin{bmatrix}
  j\omega (C_{gds} + C_{gs}) & - j\omega C_{gds} \\
  - j\omega C_{gds} & j\omega C_{gds}
\end{bmatrix} = [Y^{in}]
\]

\[
[Y^{in}] \Rightarrow [Z^{in}]
\]

\[
[Z^{in}] - \begin{bmatrix}
  R_p & R_s \\
  R_p & (R_s + R_p)
\end{bmatrix} = [Z^{int}]
\]

\[
[Z^{int}] \Rightarrow [Y^{int}]
\]

The Y-parameters thus extracted after de-embedding is given by [Y^{int}] which in details is reported in [19]. The intrinsic AC small signal model parameters have been represented in terms of [Y^{int}] in the TABLE 3.1 in chapter 3.

4.6 RF PERFORMANCE OF ASYM-UDL DMG DG NMOSFETS

In order to study the RF performance of the devices, the different RF parameters of have been compared between SYM-UDL and ASYM-UDL DMG-DG NMOSFETs. The intrinsic capacitances, the intrinsic resistances, the transport delay and the intrinsic inductance have been analyzed with the frequency. In the Fig. 4.12, the intrinsic gate to source resistance and gate to drain resistance have been plotted.
Fig. 4.12: Comparison of Intrinsic Resistance for SYM-UDL DMGDG and ASY-UDL DMG-DG NMOSFETs as a function of frequency, at $V_{ds}=0.55$V and $V_{gs}=0.55$V.

Fig. 4.12 shows that for the ASYM-UDL device both the intrinsic gate to source resistance and gate to drain resistance is lowered. It is also evident that from the Fig. 4.12 that because of absence of underlap region in the source side of the ASYM-UDL device, these devices inherit lower resistance.
It is observed from the Fig. 4.13 that the intrinsic gate to source capacitance, $C_{gs}$ of the ASYM-UDL device is higher compared to the SYM-UDL device. In the asymmetry structure of the ASYM-UDL device, the relative position of the gate has been shifted towards the left side because of not having underlap region in the source side. Therefore, $C_{gs}$ has been increased in the ASY-UDL device. Whereas, charge density has been reduced in the gate to drain side, hence, $C_{gd}$ has decreased compared to the SYM-UDL device. It is also observed that both the intrinsic resistances and capacitances are remaining constant with the frequency.
Fig. 4.14: Comparison of transport delay, $\tau_m$ and $L_{sd}$ for SYM-UDL DMG DG and ASYM-UDL DMG DG NMOSFETs as a function of frequency, at $V_{ds}=0.55\text{V}$ and $V_{gs}=0.55\text{V}$.

In the Fig. 4.14 a comparison of transport delay, $\tau_m$ and $L_{sd}$ between the SYM-UDL DMG DG and the ASYM-UDL DMG DG NMOSFETs as a function of frequency have been presented. Results show that for ASYM-UDL both the $\tau_m$ and $L_{sd}$ are lesser due to the low intrinsic gate to source resistance.

In this section, a comparison of intrinsic capacitances, resistances and transport delay have been represented with the spacer dielectric, $k$. Results show in Fig. 4.15 that the intrinsic gate to source capacitance, $C_{gs}$ is constant with $k$ as the source side spacer is kept fixed as nitride. Whereas, the gate to drain capacitance, $C_{gd}$ is increasing with $k$, as the enhancement of charge in the drain side underlap region is more for higher fringing field.
Fig. 4.15: Variation of Intrinsic Capacitance, $C_{gs}$ and $C_{gd}$ of the asymmetric ASY-UDL DMG-DG NMOSFETs as a function of spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$ at $V_{ds} = 0.55$ V, $V_{gs} = 1.1$V and frequency, $(f) = 100$GHz.

It is also evident from Fig. 4.15 that intrinsic capacitance of the device increases with the increase of work-function difference between $M_1$ and $M_2$. This leads to the increase in the conductivity of the channel, as a result, the intrinsic gate to drain resistance, $R_{gd}$ decreases significantly, as shown in the Fig. 4.16 and the intrinsic gate to source resistance, $R_{gs}$ remains unchanged.
Fig. 4.16: Variation of Intrinsic Resistance, $R_{gs}$ and $R_{gd}$ of the asymmetric ASY-UDL DMG-DG NMOSFETs as a function of spacer dielectric $k$, varying from $k = 3.9$ to $k = 22.5$ at $V_{ds} = 0.55$ V, $V_{gs} = 1.1$ V and frequency, $(f) = 100$GHz.

4.7 CONCLUSION

The influences of the asymmetric underlap on the subthreshold analog/RF performance on 45nm gate length ASYM-UDL DMG DG NMOSFETs have been analysed. This study shows that an enhancement in the FOMs of the devices including $I_{on}$, $g_m$, and $g_{mR_o}$, are enhanced by 62.150%, 53.113% and 30.837% respectively, compared to similar SYM-UDL DMG DG NMOSFET. ASYM-UDL DMG DG NMOSFETs device is providing low intrinsic resistances which leads to the low transport delay and the high
intrinsic capacitances. The value of $C_{gs}$ has been increased by 55.731% whereas, the value of $C_{gd}$, $R_{gs}$, $R_{gd}$, $\tau_m$ and $L_{sd}$ have been decreased by 50.310%, 59.681%, 13.891%, 22.749% and 3.885% respectively, compared with the SYM-UDL DMG DG NMOSFET. In case ASYM-UDL DMG DG NMOSFETs device, the intrinsic resistance and transport delay get reduced with the spacer dielectric. It suggests that it should be an ultralow power and superior device to work in the RF domain. Asymmetry structure is showing good agreement for the analog/RF application, still it may be bad for digital application for its asymmetry underlap, but it will be a promising low power device for SRAM memory application for relaxing the conflict between read stability and writability in 6T SRAM [24].


