CHAPTER 3

SYMMETRY UNDERLAP DUAL MATERIAL GATE DG-FET


3.1 **INTRODUCTION**

This work presents a systematic comparative study of Analog/RF performance for underlap dual material gate (U-DMG) DG NMOSFET. In previous works, improved device performances have been achieved by use of high dielectric constant (k) spacer material. Although high-$k$ spacers improve device performance, the intrinsic gain of the device reduces. For the analog circuits applications intrinsic gain is an important parameter. Hence, an optimized spacer material having dielectric constant, $k=7.5$ has been used in this study and the gain is improved further by dual-material gate (DMG) technology.

In this work we have also studied the effect of gate material having different work function on the U-DMG DG NMOSFETs. This device exploits a step function type channel potential created by DMG for performance improvement. Different parameters such as the transconductance ($g_m$), the gain per unit current ($g_m/I_{ds}$), the intrinsic gain ($g_mR_o$), the intrinsic capacitance, the intrinsic resistance, the transport delay and, the inductance of the device have been analyzed for analog and RF performance analysis. Analysis suggested that the average intrinsic gain, $g_{m}/I_d$ and $g_{m}$ are increase by 22.988%, 16.10% and 27.871% respectively compared to the underlap single-material gate U-DG NMOSFET.

3.2 **DUAL MATERIAL GATE DG-FET**

With growth in the field of communication, the use of higher frequencies has become mandatory as the lower frequency bands have been rapidly
occupied. Thus, the devices used in the field of communication are required to have high frequency handling capability that extends up to several giga hertz (GHz). Consequently, the need for RF devices with low power consumption has increased substantially. Several structures have been proposed for the double gate (DG) NMOSFET [1] to reduce the power consumption and, for improved performance of the device. To mitigate the power consumption of the device in analog circuits, the subthreshold region operation offers an enormous scope [2]-[5]. In the subthreshold region, drain current changes exponentially hence, the transconductance and the gain of the device is very high [2].

The concept of underlap double gate (U-DG) NMOSFET has been suggested previously [1- 4] to reduce the SCE by bias dependent effective channel length (L_{eff}>L_{gate}) and L_{eff}=L_{gate}+2L_{eSDr} [1], [3] and [7]. Where, L_{eff} is the effective channel length, L_{gate} is the gate length and L_{eSDr} is the effective source drain underlap length of the device. U-DG NMOSFET structures are also immune to the gate induced drain leakage (GIDL), the fringing capacitance and the gate-source/drain tunneling currents [3], [8], [9]. The device performance is also acceptable from the perspective of device speed, with low dynamic power consumption for digital circuits [10]. As a result U-DG NMOSFETs have become very popular in digital as well as analog/RF mixed signal applications for system-on-chip (SOC) technology.

Among the possible solutions to overcome the SCEs in conventional DG MOSFETs underlap regions have been incorporated but these underlap regions resulting extra on resistance in the device. This extra resistance reduces the on current of the analog device and therefore the analog performance degrades significantly. The reduction of on current (I_{on}) and increased source/drain resistance [1] due to the extended underlap regions, are major drawbacks of the
conventional U-DG NMOSFETs. Previously, these problems have been addressed by optimizing the underlap lengths, $L_{un}$ and by use of high k spacer material in U-DG NMOSFETs. Use of high k spacers in U-DG NMOSFETs increase the on current, $I_{on}$ however, for very high values of spacer dielectric the intrinsic gain of the device reduces. Hence, optimization of the spacer dielectric is essential for SOC application.

In this work, for the first time analog and RF performance of underlap dual material gate (U-DMG) DG NMOSFET have been investigated. In the U-DMG-DG NMOSFET, the surface potential is characterized by a step function [11], due to this potential profile the drain voltage is screened, reducing the drain induced barrier lowering (DIBL). The step potential profile is achieved by the use of different gate materials.

Higher work-function material near the drain side lowers the DIBL, whereas lower work-function material near the drain side increases on current of the device. It has been seen that SCE and DIBL have been minimized by underlap regions, however, the underlap regions added some extra resistances in the device, which in turn lowering the on current of the device. Therefore, the lower work-function material in the drain side has been used here to increase the current of the device.

The use of DMG in U-DG NMOSFET also increases the carrier transport efficiency [12] and in turn increases the $I_{on}$ of the device. In the U-DMG-DG NMOSFET, gate metal 1 is close to the source end, named $M_1$, and metal 2 is close to the drain end, named $M_2$. In conventional single metal gate device, the electric field near the source is lowest and reaches the peak value at the drain end. Due to this reason, the hot electron injection [13], [14] between the gate
and drain makes the device unreliable, and reduces its lifetime. Thus, the primary intention is to keep the peak electric field under the gate, and not near the drain end, without degrading the \( I_{on} \). Hence, U-DMG architecture is implemented in the DG NMOSFET device for which the carriers will be accelerated more rapidly and the hot electron injection problem is also avoided. This architecture will thus improve the average carrier velocity [15] which in turn enhances the \( I_{on} \). The improvement in \( I_{on} \) and DIBL suppression is achieved for lower work-function metal near the drain side (\( M_1 > M_2 \)).

The U-DMG-DG NMOSFET architecture having optimized underlap length of 20 nm and, spacer material of dielectric constant, \( k = 7.5 \). To improve shortcomings of the conventional U-DG NMOSFETs, metal work-functions \( M_1 \) and \( M_2 \) have been varied such that \( M_1 \) is always greater than \( M_2 \). The Analog performance of the devices is compared with conventional U-DG NMOSFET having matched threshold voltage of 0.366V. The parameters considered for the comparison are the transconductance (\( g_m \)), the gain per unit current (\( g_m/I_d \)) and the intrinsic gain (\( g_m r_o \)). For RF performance analysis the extraction of RF parameters are performed by considering non-quasi-static (NQS) small signal equivalent circuit [16].

The objective of this work is to analyzed the improvement in \( g_m \), \( g_m/I_d \), \( g_m r_o \), \( I_{on} \) and RF parameters by using different work functions for \( M_1 \) and \( M_2 \) for ultralow-power, high gain analog/RF circuits. The underlap lengths of the 45 nm U-DMG-DG NMOSFETs are optimized with the help of 2-D numerical tool Sentaurus TCAD [17] and a comparison is performed between these devices.
3.3 TCAD SIMULATION OF DUAL MATERIAL GATE DG-FET

The cross-sectional view of the symmetric U-DMG-DG NMOSFET is shown in Fig. 3.1. The technology parameter of the device is adjusted such that the gate length \( L_g \) is of 45 nm, the oxide thickness \( T_{ox} \) is of 1.9 nm and the silicon body thickness \( t_{si} \) is of 16 nm according to the ITRS 2008 for RF and Mixed Signal application [18]. The optimized underlap length \( L_{un} \) is 20 nm and the \( n^+ \) source/drain doping is \( 10^{20} \) cm\(^{-3}\). The silicon body is kept lightly doped, with p-type doping of \( 10^{15} \) cm\(^{-3}\).

![Cross section of a U-DMG-DG NMOSFET with source underlap and drain underlap.](image)

The lateral source/drain doping profile into the channel is given by \( N_{sd}(x) = N_{peak} \exp \left( -x^2/\sigma^2 \right) \) where, \( x \) signifies the position from source/drain (S/D) into the channel, \( N_{sd} \) is the doping concentration at point \( x \). \( N_{peak} \) is the maximum S/D doping concentration, \( \sigma \) is the lateral straggle parameter determined by the fabrication procedure and is considered here to be 3 nm. In this work, all the simulations are performed considering density gradient model for carrier
transport with Aurora mobility model [19] that accounts for ionized impurity scattering and temperature dependency. Shockley-Read-Hall (SRH) recombination model and incomplete ionization models are incorporated for determining the active carrier lifetime and density respectively. The gate metal is segmented equally into M₁ and M₂. All the simulations are performed using 2-D device simulator [17] calibrated with the standard experimental data [20].

![Image](image.png)

**Fig. 3.2:** Variation of $I_{on}$ and $I_{off}$ ratio with source underlap and drain underlap lengths for U-DMG-DG NMOSFET devices.

The analog/RF parameters are extracted at different gate to source biasing voltage, $V_{gs}$ and drain to source biasing voltage, $V_{ds}$. Devices with various underlap lengths are simulated and the performances of $I_{on}/I_{off}$ ratio is measured using TCAD device simulator for optimization. The plot for $I_{on}/I_{off}$ against the source underlap length and drain underlap length is shown in Fig.3.2.
It is observed from Fig. 3.2 that the device achieves maximum $I_{on}/I_{off}$ for a symmetric source and drain underlap lengths of 20 nm each. This is because of the decrease in $I_{off}$ which is more prominent as the larger underlap lengths due to increase in channel resistance. Thus, in the rest of the work 20 nm underlap length has been considered as the optimized length. For RF performance analysis the U-DMG-DG NMOSFET device with metal gate work functions fixed at $M_1=4.7eV$, $M_2=4.3eV$ and threshold matched U-DG NMOSFET device, having single gate, with gate work-function fixed at 4.655eV are considered. The devices have threshold voltage of 0.36V. At the time of RF parameter extraction the $V_{ds}$ is fixed at 0.55V accordance with to ITRS 2008 [18], the $V_{gs}$ is fixed at 1.0V and the frequency is varied up to 100 GHz. The U-DMG-DG NMOSFET device can be fabricated by following the steps for fabricating the standard Fin-FETs [21], with an additional step of introducing the underlap regions on the source and drain sides of the channel using the tilt ion implantation technique [22]. The feasibility of the structure is illustrated in [23]. The device spacer material $k$ is fixed at 7.5. Optimized grid spacing for the structure has been achieved by following the guidelines as suggested in [24].

### 3.4 Analog Performance of Dual Material Gate DG-FETs

The analog performance of the device with respect to conventional U-DG NMOSFET is presented in this section. The analog parameters analyzed for studying the improvement are $I_d$, $g_m$ and $g_{mr_o}$. For understanding the
significance of using DMG in U-DG NMOSFET the conduction band diagram of the devices is presented in Fig. 3.3 at $V_{gs}$ of 0.55 V and 0.3 V.

![Fig. 3.3: Comparison of conduction band energy along the channel of a 45-nm U-DMG-DG and U-DG NMOSFETs, at $V_{ds}=0.55V$ with different gate voltage bias of $V_{gs}=0.55V$ and $V_{gs}=0.3V$.]

It is observed from the Fig. 3.3 by comparison, of conduction band energy along the channel, between U-DMG-DG and U-DG NMOSFET device that the conduction band along the channel decreases abruptly owing lower value of $M_2$ creating a step potential profile along the channel in the U-DMG-DG device. This increases the average electron velocity in the channel which in-turn increase the drain current ($I_{ds}$) of the device as shown in the Fig. 3.4.
It is also observed from Fig. 3.5 that $g_m$ increases both in the strong inversion and the subthreshold region for U-DMG-DG device as a result of improved $I_{ds}$, owing to less effective threshold voltage [25].

The $g_m r_o$ for the U-DMG-DG device is presented in Fig. 3.6. Since, the U-DMG-DG NMOSFET provides a huge increase of potential due to step change at the interface of $M_1$ and $M_2$, the major portion of the channel is shielded from the $V_{ds}$ change, in comparison to U-DG NMOSFET. This improves the output resistance ($r_o$) of the device and hence, a large improvement in the intrinsic gain is attained, as shown in the Fig. 3.6.
Fig. 3.5: Comparison of the transconductance ($g_m$) for U-DMG-DG and U-DGNMOSFETs as a function of $V_{gs}$ at $V_{ds}=0.55V$.

Fig. 3.6: Comparison of the ($g_{mr}$) for U-DMG-DG and U-DGNMOSFETs as a function of $V_{gs}$, at $V_{ds}=0.55V$. 
The cause of improvement in \( r_o \) is described as follows. The early voltage for the U-DMG-DG device shifts to a higher \( V_{ds} \) as the \( V_{ds} \) required for channel pinch off, for U-DMG-DG device, is higher. The shift in pinch-off point is illustrated in Fig. 3.7. This shift results in lower drain conductance \((1/r_o)\) causing \( r_o \) of the device to decrease. This also emphasizes that U-DMG-DG device has less SCE and is thus more scalable.

![Fig. 3.7: Comparison of the \( I_{ds} \) for U-DMG-DG and U-DG NMOSFETs as a function of \( V_{ds} \), at \( V_{gs}=0.3 \) V.](image)
Fig. 3.8: Comparison of the $g_m/I_d$ for U-DMG-DG and U-DG NMOSFETs as a function of $V_{gs}$, at $V_{ds}=0.55V$.

Fig. 3.8 shows the comparison of the $g_m/I_d$, for U-DMG-DG and U-DG NMOSFETs as a function of $V_{gs}$. It is observed that, there is a slight reduction (<6%) in the value of $g_m/I_d$ in the subthreshold regime. However, the performance degradation is not significant as the power dissipation is very less and the intrinsic gain is very high due to improved $r_o$ described earlier in the section. The $g_m/I_d$ of the device however improves at higher $V_{gs}$ which is about 9.24% at $V_{gs}=1.0V$.

### 3.5 RF PERFORMANCE OF DUAL MATERIAL GATE DG-FETS

To study RF performance work functions of gate metals ($M_1$ and $M_2$) are varied for three different U-DMG-DG devices to understand the device
characteristics. Fig. 3.9 shows the variation of the conduction band energy along the channel for three U-DMG-DG NMOSFETs with channel length 45 nm and different gate metal work-function values. The work-function combinations used for the different devices are (M₁=4.7eV, M₂=4.1eV); (M₁=4.7eV, M₂=4.3eV); (M₁=4.7eV, M₂=4.5 eV).

**Fig. 3.9:** Variation of conduction band energy along the channel of 45-nm U-DMG-DG NMOSFETs for different values of metal work-functions, at V_{gs} = V_{ds} = 0.55 V.

The I_{ds} for the U-DMG-DG NMOSFET with the different gate metal work-function combinations is shown in Fig. 3.10. It is observed from Fig. 3.10 that the I_{ds} for lower value of M₂ significantly increase. This is due to increase in the carrier transport efficiency which improves for larger M₂ and M₁ work-function difference where, M₁ is greater than M₂. Also, low work-function values of M₂ improve the drain bias screening and hence, the device has better immunity to SCE.
Fig. 3.10: Variation of drain current of 45-nm U-DMG-DGNMOSFETs as a function of $V_{gs}$, for different values of $M_1$ and $M_2$ work-functions at $V_{ds} = 0.55$ V.

The RF performance of the device is analyzed using small signal equivalent circuit of the device with the NQS effect. The small signal equivalent circuit of the device under investigation is given in [16]. The RF parameter extraction is performed by $Y$-parameter analysis of the AC small signal model. The first step during parameter extraction is to extract $Y$-parameters from the simulator under zero biased condition. Then the extrinsic gate-to-S/D capacitances, $C_{gso}$ and $C_{gdo}$ are calculated from the extracted $Y$-parameters.

$$C_{gdo} = -\frac{\text{Im}(Y_{21})}{\omega} \quad (1)$$

$$C_{gso} = \frac{\text{Im}(Y_{11}) + \text{Im}(Y_{21})}{\omega} \quad (2)$$
The source and drain resistance (R_s and R_d) are extracted using the channel length method [16] and are found to be 8.3 ohm. Before starting the intrinsic RF parameter analysis as in [16], the de-embedding step as described in [16] and [26]-[28], has to be performed, as represented by following steps.

\[
[Y] - \begin{bmatrix}
  j\omega(C_{gds} + C_{gso}) & -j\omega C_{gdo} \\
  -j\omega C_{gdo} & j\omega C_{gdo}
\end{bmatrix} = [Y^{in}]
\]

\[
[Y^{in}] \rightarrow [Z^{in}]
\]

\[
[Z^{in}] - \begin{bmatrix}
  R_D & R_S \\
  R_D & (R_S + R_D)
\end{bmatrix} = [Z^{int}]
\]

\[
[Z^{int}] \rightarrow [Y^{int}]
\]

The Y-parameters thus extracted after de-embedding are given by \([Y^{int}]\), details of which is reported in [16]. The intrinsic AC small signal model parameters in terms of \([Y^{int}]\) are tabulated as below. In this study, the RF performance parameters, such as the intrinsic capacitances, the intrinsic resistances, the transport delay and the intrinsic inductance are analyzed for different work-function values of M_2 and a fixed value of 4.7eV for M_1. It is observed that the intrinsic parameters remain constant with frequency.
### TABLE 3.1: SUMMARY OF EQUATIONS USED FOR SMALL SIGNAL PARAMETERS CALCULATION

<table>
<thead>
<tr>
<th>NAME OF THE PARAMETER</th>
<th>EQUIVALENTS EXPRESSION WITH Y PARAMETER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intrinsic gate to drain capacitance ($C_{gd}$)</td>
<td>$\text{Im}(Y_{12}^{\text{int}})$</td>
</tr>
<tr>
<td>Intrinsic gate to source capacitance ($C_{gs}$)</td>
<td>$\frac{\text{Im}(Y_{11}^{\text{int}}) + \text{Im}(Y_{12}^{\text{int}})}{\omega}$</td>
</tr>
<tr>
<td>Intrinsic gate to drain resistance ($R_{gd}$)</td>
<td>$-\frac{\text{Re}(Y_{12}^{\text{int}})}{\omega^2 C_{gd}}$</td>
</tr>
<tr>
<td>Intrinsic gate to source resistance ($R_{gs}$)</td>
<td>$\frac{1}{C_{gs}^2} \left[ \frac{\text{Re}(Y_{11}^{\text{int}})}{\omega^2} - R_{gs} C_{gd}^2 \right]$</td>
</tr>
<tr>
<td>Gate to source Transconductance ($g_m$)</td>
<td>$\text{Re}(Y_{11}^{\text{int}})\big</td>
</tr>
<tr>
<td>Drain to source Transconductance ($g_{ds}$)</td>
<td>$\text{Re}(Y_{22}^{\text{int}})\big</td>
</tr>
<tr>
<td>Transport delay ($\tau_m$)</td>
<td>$\frac{1}{g_m} \left[ -\frac{\text{Im}(Y_{21}^{\text{int}})}{\omega} - C_{gd} \right]$</td>
</tr>
<tr>
<td>Inductance ($L_{sd}$)</td>
<td>$\frac{\tau_m}{g_{ds}}$</td>
</tr>
</tbody>
</table>
In Fig. 3.11 the intrinsic capacitance of the device is presented with respect to frequency for different $M_2$ work-function values. It is observed that the Intrinsic gate to drain capacitance, $C_{gd}$ is lesser compared to the intrinsic gate to source capacitance, $C_{gs}$ for the same device, as the drain side inversion charge in is lesser than the source side inversion charge.

![Intrinsic Capacitance Diagram]

**Fig. 3.11:** Variation of $C_{gs}$ and $C_{gd}$ as a function of frequency for 45-nm U-DMG-DG NMOSFET for different metal work-functions, at $V_{gs}=1$V and $V_{ds}=0.55$ V.

It is also evident from the Fig. 3.11 that, the $C_{gd}$ increases with increase in $M_1$ and $M_2$ gate metal work-function difference while, the $C_{gs}$ decreases. This is due to uneven distribution of total inversion charge in the channel, described as following. The total inversion charge in the channel for a particular gate bias is constant. However, the inversion charge under $M_2$ is more due to low work-
function and less under $M_1$ due to higher work-function resulting in lower value of $C_{gs}$ and higher value of $C_{gd}$. For a fixed work-function of $M_1$ when the value of work function of $M_2$ is reduced, the difference between the work-function increases. This causes the inversion charge concentration on the gate to drain side to increase even more and, the abruptness of the step potential profile also increases as in Fig. 3.9. Thus, as the gate work-function difference increases $C_{gs}$ decreases further whereas, $C_{gd}$ increases more as in Fig. 3.11.

![Graph showing variation of $R_{gs}$ and $R_{gd}$ with frequency for 45-nm U DMG-DG NMOSFET for different metal work-functions, at $V_{gs}=1$V and $V_{ds} = 0.55$ V.]

**Fig.3.12:** Variation of $R_{gd}$ and $R_{gd}$ as a function of frequency for 45-nm U DMG-DG NMOSFET for different metal work-functions, at $V_{gs}=1$V and $V_{ds} = 0.55$ V.

The variation of intrinsic resistance of the device with frequency is shown in Fig. 3.12 which decreases for lower work-function $M_2$. This can be explained as follows. As the abruptness of the step potential profile increase due to the increase in the work-function difference, as described earlier in the section, the carrier mobility increases as the carrier transport efficiency is
enhanced. This leads to the reduction of the intrinsic resistances of the device with the increase of work-function difference between M₁ and M₂ as shown in Fig. 3.12.

Fig. 3.13 shows that the transport delay of the device that decreases with the increase of work-function difference as a result of reduces intrinsic resistance as depicted in Fig. 3.12. Thus, due to the low transport delay, the gate charging times, $R_{gs}C_{gs}$ and $R_{gd}C_{gd}$, also decrease.

![Graph showing variation of transport delay and inductance with frequency](image)

Fig. 3.13: Variation of $\tau_m$ and $L_{sd}$ as a function of frequency for 45-nm U-DMG-DG NMOSFET for different metal work-functions, at $V_{gs}$=1V and $V_{ds}$= 0.55 V.

The cut-off frequency ($f_T$) and maximum frequency ($f_{MAX}$) for the device are presented in Fig. 3.14 (a) and (b) respectively. It is found that the $f_T$ and $f_{MAX}$ increases for higher M₁ and M₂ work-function difference owing to increase in $I_{ds}$. 
Fig. 3.14: Variation of (a) cutoff frequency ($f_T$) and (b) maximum frequency ($f_{\text{MAX}}$), as a function of $I_{\text{ds}}$ for 45-nm U-DMG-DG NMOSFET for different metal work-functions, at $V_{\text{gs}}=1.0\,\text{V}$ and $V_{\text{ds}} = 0.55\,\text{V}$. 
3.6 CONCLUSION

The influence of dual material gate on subthreshold analog/RF performance of U-DGNMOSFET is presented in this analysis. The performance is analysed for different dual material gate work-functions of U-DMG-DG NMOSFET. The analog performance of the device is analysed in subthreshold regime and a significant improvement is observed with regards to conventional U-DG NMOSFET. The study shows that an improvement of 22.988 % for $I_{ds}$, 16.10 % for $g_m$ and 27.871% for $g_m r_o$, at $V_{gs}$=0.3V is obtained with U-DMG-DG NMOSFET, configured at $M_1$=4.7 eV and $M_2$=4.1 eV, with regards to U-DG NMOSFET.

It is also demonstrated by studying the intrinsic RF parameters that the RF performance of U-DMG-DG NMOSFET is best for lowest value of $M_2$ when $M_1$ is kept fixed. The RF parameter $R_{gd}$ and $C_{gs}$ decreases by 4.153 % and 13.210 % respectively, for $M_2$= 4.1eV with respect to $M_2$= 4.3 eV, at $V_{gs}$=1.0 V and $V_{ds}$=0.55 V reducing source side transport delay. Also, for same configuration and bias condition, $R_{gd}$ and $C_{gd}$ decreases by 36.208% and increases by 59.472% respectively, since $R_{ds}$ is very less the drain side transport delay is also significantly reduced. The total transport delay is effectively reduces by 14.463% for the lower work-function $M_2$. 

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3.7 REFERENCES


