CHAPTER-IV

EXPERIMENTAL AND SIMULATION PROGRAM

4.0 INTRODUCTION

This chapter covers in detail the experimental set up of proposed Z source Matrix (ZSMC) based UPFC and compares with a lab scale model of Conventional Voltage Source Converter (VSC-UPFC) based UPFC. The experimental results have been verified with the simulation results developed in MATLAB-Simulink. The study is aimed at identifying better performance. This chapter covers the experimental test programs in the following sections as following.

Section 4.1 Simulation and Analysis of a 3 Ph conventional VSC-UPFC in IEEE 5 bus test system using MATLAB-Simulink.

Section 4.2 Construction of a 1 Ph, 2 bus Lab Scale Model of conventional VSC-UPFC.

Section 4.3 Simulation and Analysis of a 1 Ph ZSMC in PSPICE environment.

Section 4.4 Simulation and Analysis of a 1 Ph 2 bus ZSMC as UPFC in MATLAB-Simulink.

Section 4.5 Construction of a 1 Ph, 2 bus Lab Scale Model of the proposed ZSMC-UPFC.

Section 4.6 Summary and discussion on the experimental and simulation results.
4.1 MATLAB -SIMULINK MODEL OF CONVENTIONAL VSC - UPFC

A standard IEEE 5 bus test system [Stagg and El-Abiad 1968] is modeled and simulated in MATLAB-Simulink consisting of two generator buses and three load buses with UPFC installed in the line 7 between buses 4 and 5 is depicted clearly in the Fig 4.1 and Fig 4.2.

The generators, transmission lines and the loads are rated at 1.8 KV (Peak 2.5 KV). A three phase UPFC with two voltage source converters to serve as STATCOM and SSSC is developed using MOSFETS as switching devices at power line frequency, 50 HZ. The dc link capacitor rated at 200 mF and the two transformers shunt and series at 1800 V/230 V are connected to the transmission line.

The bus data and line data along with the simulation parameters of UPFC are tabulated in Tables 4.1, 4.2 and 4.3. The actual values of voltage, current, real power and reactive power at all buses are obtained using VI and PQ Simulink Blocks. This is similar to measurements taken using PMU’s and RTU’s for state estimation. Voltage magnitude, voltage angle, and real and reactive current are measured by PMU while the injection and flow of real and reactive power are monitored through RTU. The power injection and flow measurements are employed to obtain the control parameters of FACTS controllers in a very short time span, and, therefore, avoid conventional state estimation procedures for arriving at the control
settings of the UPFC under a given operating condition, while satisfying a specified control objective [Phadke, 1993].

Table 4.1 Bus Data

<table>
<thead>
<tr>
<th>S.No</th>
<th>Bus Type</th>
<th>V (p.u)</th>
<th>Pd (MW)</th>
<th>Qd (MVAR)</th>
<th>Pg (MW)</th>
<th>Qg (MVAR)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Slack bus 1</td>
<td>1.0</td>
<td>0</td>
<td>0</td>
<td>6.0</td>
<td>5.0</td>
</tr>
<tr>
<td>2</td>
<td>Genr bus 2</td>
<td>1.0</td>
<td>0</td>
<td>0</td>
<td>6.5</td>
<td>6.0</td>
</tr>
<tr>
<td>3</td>
<td>Load bus 3</td>
<td>1.0</td>
<td>6.75</td>
<td>3.25</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>Load bus 4</td>
<td>1.0</td>
<td>0.50</td>
<td>2.0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>5</td>
<td>Load bus 5</td>
<td>1.0</td>
<td>1.70</td>
<td>2.0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 4.2 Line Data

<table>
<thead>
<tr>
<th>Transmission line</th>
<th>Nl</th>
<th>Nr</th>
<th>R(p.u)</th>
<th>X(p.u)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>2</td>
<td>0.02</td>
<td>0.06</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
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<td>0.02</td>
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<tr>
<td>3</td>
<td>2</td>
<td>3</td>
<td>0.024</td>
<td>0.18</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>4</td>
<td>0.024</td>
<td>0.18</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>5</td>
<td>0.02</td>
<td>0.12</td>
</tr>
<tr>
<td>6</td>
<td>3</td>
<td>4</td>
<td>0.02</td>
<td>0.03</td>
</tr>
<tr>
<td>7</td>
<td>4</td>
<td>5</td>
<td>0.02</td>
<td>0.24</td>
</tr>
</tbody>
</table>

**BUS DATA**

Base MVA : 100MVA

Base KV    : 1.8KV
Table 4.3 Simulation Parameters of UPFC

<table>
<thead>
<tr>
<th>S.No</th>
<th>Component</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Shunt Transformer</td>
<td>1800/230 V</td>
</tr>
<tr>
<td>2.</td>
<td>Series Transformer</td>
<td>230/1800 V</td>
</tr>
<tr>
<td>3.</td>
<td>DC Link Capacitor</td>
<td>200 $mF$</td>
</tr>
<tr>
<td>4.</td>
<td>Converter Switches - MOSFETs</td>
<td>$V_{dss} = 240V$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Operating frequency - 50 Hz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Switching frequency - 1MHz</td>
</tr>
<tr>
<td>5.</td>
<td>PI Controller</td>
<td>$K_p = 2$, $K_i = 200$</td>
</tr>
</tbody>
</table>

Fig 4.1 MATLAB-Simulink Model of UPFC
Fig 4.2 IEEE 5 Test Bus with UPFC - Simulink Block Diagram
4.1.1 Control Scheme of VSC-UPFC

A closed loop control using a PI controller is incorporated to operate at the shunt end as STATCOM in the reactive control mode and at the series end as SSSC in automatic power flow control mode by controlling the magnitude and angle of the series injected voltage. Refer Fig 4.3. The three phase voltages and currents are sensed and transformed into two phase quantities using Parks Transformation which gives d-q current and voltage to the controller. The actual real and reactive power values are fed into the controller from PQ blocks. The reference inputs $P_{\text{ref}}$ and $Q_{\text{ref}}$ fed into the controller are compared with the actual values. A phase locked loop (PLL) is used to determine the instantaneous angle of the line voltage. The current component $I_d$ and $I_q$ is used to determine the relative phase angle with respect to the voltage.

**At the SSSC end**

SSSC is operated in Automatic Power Flow Mode at the series end by controlling the magnitude and angle of the series injected voltage. Hence at the series end SSSC, real power mismatch and reactive power is compensated. The reference power inputs are fed into the controller. The actual line voltage, current, real power and reactive power are measured using VI and PQ blocks. These actual powers are compared with the reference powers.

$P/2$ is added or subtracted to injected voltage with respect to line current emulates inductive or capacitive compensation whichever
is required at SSSC end. This actually decreases/increases the magnitude of the bus voltage at that point, thereby compensating the reactive power.

As for real power mismatch, phase shift control which controls the phase angle of the injected voltage is applied.

For extra real and reactive power, voltage magnitude is increased by pulse width modulation technique.

The SSSC pulse generator thus generates the compensating voltage.

**At the STATCOM end**

The STATCOM controller at the shunt end generates the required output voltage magnitude and phase angle in synchronism with the ac sinusoidal system. The reactive power mismatch is adjusted through this control. The reactive current reference $I_q$ is set to zero for unity power factor. The real current reference $I_d$ is set with respect to instantaneous real power reference, $P = 3/2 V_d I_d$. For additional reactive power, the STATCOM controller increases the modulation index.
Fig 4.3 Simulation circuit of PI Controller and dq Transformation Block
4.1.2 Simulation Results of Conventional VSC-UPFC

A power flow study is conducted on the 5 bus test system. The loads are applied at three load buses and the actual values of voltage and power at all buses (similar to power flow like results). Based on bus voltage magnitude obtained from the above measured results, bus 4 is identified as the most critical bus. The UPFC is chosen to be located between bus 4 and bus 5 on line 7. Similar load study is conducted with UPFC to illustrate its superior performance.

To illustrate the results further, a load variation study with UPFC is carried out at bus 4. For studying the UPFC’s effect on transient stability, a sudden peak load of 148% i.e. 0.75 MW active load and 2.96 MVAR reactive load are applied at 0.2 seconds through a circuit breaker. The actual value of voltage and power at all buses for peak load is tabulated in Table 4.4. The output voltage obtained at STATCOM and SSSS are shown in Fig 4.4 and 4.5. A small phase angle difference is noted between the line voltage and current at the shunt end as shown in the power factor angle diagram Fig 4.6. Thus the line current is nearly in phase with the input voltage (p.f 0.95 lead) clearly illustrates the STATCOM’s role as a reactive power compensator. The STATCOM has absorbed a small amount of real power from the ac transmission line system. The series injected voltage by SSSC is almost in quadrature lag with the transmission line current operated in capacitive mode as shown in Fig 4.7.
The transmission supply voltage is seen to have decreased to 0.66 p.u i.e. 1.26 kV (Peak Volt 1.78 kV) as shown in the Table 4.4 and Fig 4.8 with application of peak load. The three phase line currents are almost in phase with supply voltage after UPFC is connected as shown in Fig 4.9. This has confirmed that the UPFC has the capability of transient stability.

The results clearly illustrate the superior performance of UPFC with respect to voltage enhancement, followed by increase in real power and reactive power flow at bus 4.
Fig 4.5 SSSC (Inverter) Output Voltage

Fig 4.6 At STATCOM end - Power Factor
Fig 4.7 SSSC Injected Voltage and Line Current (Capacitive mode)

Fig 4.8 Transmission Line Voltage during Peak Load without UPFC
Table 4.4 Bus Voltage and Power - VI and PQ Simulink Blocks

<table>
<thead>
<tr>
<th>Bus No</th>
<th>Type of Bus</th>
<th>Without UPFC</th>
<th>With UPFC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V (pu)</td>
<td>P (MW)</td>
<td>Q (MVAR)</td>
</tr>
<tr>
<td>1</td>
<td>Slack bus</td>
<td>1</td>
<td>3.94</td>
</tr>
<tr>
<td>2</td>
<td>Generator Bus</td>
<td>0.95</td>
<td>6.5</td>
</tr>
<tr>
<td>3</td>
<td>Load Bus</td>
<td>0.85</td>
<td>6.75</td>
</tr>
<tr>
<td>4</td>
<td>Load Bus</td>
<td><strong>0.66</strong></td>
<td><strong>0.75</strong></td>
</tr>
<tr>
<td>5</td>
<td>Load Bus</td>
<td>0.86</td>
<td>1.7</td>
</tr>
</tbody>
</table>
4.1.3 Summary and Discussion

1) Enhanced voltage profile at all buses is observed with UPFC installed.

2) The real power generation at bus 1 has shown an increase to meet the increased peak load at bus 4.

3) The reactive power generation at bus 1 and bus 2 has shown a decrease clearly demonstrating that UPFC has generated the required reactive power based on its VA rating to meet the increased peak load at bus 4.

4) The real power in the line 4-5 with UPFC connected has shown a two fold increase from 0.2 MW to 0.4 MW.

5) The reactive power in the line 4-5 with UPFC has increased from 1 MVAR to 2 MVAR.

4.2 EXPERIMENTAL MODEL OF CONVENTIONAL VSC - UPFC.

A conventional experimental model of single phase UPFC is constructed using two voltage source converters connected through a dc link capacitor with a shunt transformer and a series transformer inserted at the two ends of the transmission line. The hardware specifications for the prototype model are tabulated in Table 4.5. MOSFETS are used as switching devices. A resistor and an inductor coil rated at 15 ohms and 3.33 ohms is used to represent a radial distribution like line of X/R ratio 0.22. A 24 V voltage source is connected at the sending end through a step down transformer 230/24V. An induction motor rated at 24V, 1.2A is connected at the
load for studying the effect of UPFC. The capacitor is usually designed for 10% of the nominal voltage. The SSSC converter at the other end injects the synchronized voltage through the series transformer with the required phase shift into the line.

The Programmable Interface Controller (PIC) is programmed to generate PWM signals to trigger the MOSFETS through the gate driver circuit. The comparator provides a reference signal to generate trigger signals in synchronization with the supply voltage. The program starts triggering when the zero crossing of the ac supply is detected through ZCD. The program generates a pulsed signal at 50 HZ. A delay is obtained at the output of the inverter by adding a delay instruction before the start of the trigger. As the phase shift $\theta$ is increased introducing the time delay, the output voltage shifts with respect to supply voltage. Filters are added to get a smooth sinusoidal voltage to synchronize with ac input voltage. The photo shot of the entire hardware set up along with the block diagram is shown in Fig 4.10 and Fig 4.11
4.2.1 Experimental Results of Conventional VSC-UPFC

The experimental results at the STATCOM, SSSC, and the final output voltage of UPFC synchronized with input voltage at 24 V through series step up transformer are as shown in Fig 4.12 to Fig 4.15.
Fig 4.12 Rectifier Module (STATCOM) Output-CRO

Fig 4.13 Inverter Module (SSSC) Output-CRO

Fig 4.14 Output voltage without UPFC-CRO
Table 4.5 Conventional VSC-UPFC -Hardware Specifications

<table>
<thead>
<tr>
<th>S.No</th>
<th>Name of Component</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Transmission line</td>
<td>Input = 230/24V, R = 15 ohms, X = 3.33 ohms&lt;br&gt;Load = 1 Ph Induction Motor, 24V, 1.2A&lt;br&gt;Step Down Transformer = 230/24V</td>
</tr>
<tr>
<td>2</td>
<td>Shunt transformer</td>
<td>230/24V</td>
</tr>
<tr>
<td>3</td>
<td>Series transformer</td>
<td>24/230V</td>
</tr>
<tr>
<td>4</td>
<td>Converter Power Circuit</td>
<td>MOSFET IRF 460</td>
</tr>
<tr>
<td>5</td>
<td>Driver circuit</td>
<td>Transistor (2N222A, CK100)</td>
</tr>
<tr>
<td>6</td>
<td>Micro Controller</td>
<td>PIC 16F877A</td>
</tr>
<tr>
<td>7</td>
<td>DC Link Capacitor</td>
<td>10 mF</td>
</tr>
</tbody>
</table>

4.3 PROPOSED ZSMC BASED UPFC.

This chapter explains the design, control strategy and the transfer voltage gain of the prototype Z source Matrix Converter based UPFC model (ZSMC) verified by simulation analysis in PSPICE and MATLAB-Simulink environment. PSPICE (Simulation Program with Integrated Circuit Emphasis) is a general purpose program suitable
for simulating electronic circuits. Till recently PSPICE is compatible only on main frame computers. Hence the operation modes, its output voltages at different amplitudes and frequency are simulated in PSPICE. The limitations of PSPICE are the program statements have to be edited for every change of component value.

Hence a power flow study for different variations of load using UPFC has been simulated in the powerful MATLAB-Simulink environment. An investigation of its capabilities and characteristics as a unified power flow controller (UPFC) is presented in detail.

The novel model is obtained by coupling the Z source network with the PWM based matrix converter. This ac to ac converter can buck and boost voltage with step changed frequency. The pulse width modulation strategy provides the near sinusoidal voltage waveform with the required phase shift.

The Z source topology provides the extra open circuit zero state when all the switches are turned off and the output terminals of the Z source are open circuited. This attributes for the unique buck boost capability.

4.3.1 PSPICE Simulation Model of ZSMC

In order to study the principle and mode of operation of ZSMC a single phase matrix converter with Z source circuit, fed to a resistive load is simulated in PSPICE for different frequencies and different voltage magnitude bucked and boosted. It has a bridge type configuration with four MOSFET switches and combination of diodes
connected in anti parallel for facilitating independent control of current in both directions as depicted in Fig 4.16. The Z source topology and the triggering pulse circuit are as shown in Fig 4.17A and Fig 4.17B.

At the input side of the matrix converter, LC input filter, one buck boost MOSFET bidirectional switch, and the Z source impedance circuit are employed. The LC filter is used to reduce the ripples in the input current. The Z source impedance is a combination of two inductors L1 and L2 and two capacitors C1 and C2 serving as energy storage elements. The simulation parameters are given in detail in Table 4.6. Since the switching frequency 1 kHz in the Z source circuit is much higher than the matrix converter frequency 50 Hz, the size of inductors and capacitors is very small.

The amplitude of the output voltage is controlled by duty ratio of the matrix converter switches and the boost factor in the Z source circuit. The boost factor is controlled by the duty cycle of the shoot through state over the non shoot through active state. During the shoot through state, only zero voltage is impressed on the matrix converter. The output frequency is changed by the switching strategy.
Fig 4.16 Matrix Converter simulated in PSPICE

Fig 4.17A Z Source Network Simulated in PSPICE
**Fig 4.17B PSPICE Simulation of Triggering Pulse Circuit**

**Table 4.6 PSICE Simulation Parameters of ZSMC**

<table>
<thead>
<tr>
<th>S.No</th>
<th>Components</th>
<th>Ratings</th>
</tr>
</thead>
</table>
| 1    | Triggering Pulse Circuit for 4 switches | Voltage - V1,V2,V3,V4 = 12 V  
|      |                                     | Resistance - R1,R2,R3,R4 = 1k ohm           |
| 2    | Z source Network                    | Input side                                   |
|      |                                     | Input Voltage = 230 Volts                   |
|      |                                     | Inductance L1,L2,L3 = 10 µH                  |
|      |                                     | Capacitance C1,C2 = 10 µF, C3 = 0.0001 µF     |
|      | **Buck-Boost Switch side**          | MOSFET - 1 No                                |
|      |                                     | Switching Frequency = 1 kHz                  |
|      |                                     | Trigger voltage = 24V                       |
|      |                                     | TR - Rise Time = 1 ns                        |
|      |                                     | TF - Fall Time = 1 ns                        |
| 3    | 1 PH Matrix Converter               | MOSFETs = 4 Nos                             |
|      |                                     | Diode = 4 Nos                               |
|      |                                     | Pulse width = 20 ms (50 HZ)                 |
|      |                                     | Resistance load = 500 K ohms                |
|      |                                     | Inductance load = 10 mH                     |
4.3.1.1 Modes of Operations of Matrix Converter

In this mode D1, GM1, D4, load R1, D14, GM4, D18 conduct. The input voltage appears across the load as output.

In this mode D10, GM3, D12, load R1, D6, GM2, D7 conduct. The polarity of the output voltage is just opposite to the output obtained in the previous mode.
In this mode D5, GM2, D8, load R1, D9, GM3, D13 conduct. The polarity of the output voltage is just opposite to the output obtained in the previous mode.

In this mode D15, GM4, D19, load R1, D2, GM1, D3 conduct. The polarity of the output voltage is just opposite to the output obtained in the previous mode.
4.3.2 **PSPICE Simulation Results - ZSMC**

The simulation results illustrate that the ZSMC is capable of producing output voltages at different amplitudes.
- bucking input voltage 230V to 64V as shown in Fig 4.22.
- boosting input voltage 230V to 340V as shown in Fig 4.23
- producing output voltage 230V at unity voltage transfer ratio as shown in Fig 4.24

A frequency changer is inherently a phase shifter. Hence the unique capability to provide output voltages at different frequencies is also demonstrated.

Fig 4.25 shows Matrix output voltage at 50 Hz frequency.
Fig 4.26 shows matrix output voltage at 30 Hz frequency.
Fig 4.27 shows Matrix Output Voltage at 100 Hz frequency.

### 4.3.2.1 Matrix Output Voltage at Various Amplitudes

![Matrix Output Voltage at Various Amplitudes](image)

**Fig 4.22 Buck Voltage- 64 V**
4.3.2.2 Matrix Output Voltage at Various Frequencies

Fig 4.25 Matrix Output Voltage at 50 Hz frequency
A simple two bus single phase equivalent is chosen as the power system for investigating the performance of proposed ZSMC based UPFC. A generator of 210 kV (peak 300 kV) with a short circuit capacity of 15,000MVA is connected to bus 1. A transmission line rated at 210 KV and X/R ratio 9 is constructed. The ZSMC is connected to this transmission line through shunt and series transformers rated at 150 MVA. A single phase dual configuration based matrix converter with four switches is coupled to Z source.
impedance circuit consisting of two inductors and two capacitors. This configuration is equivalent to two VSC’s connected without the dc link capacitor and coupled to the Z source impedance. The entire simulink block diagram representing the above configuration and set up is clearly depicted in the Fig 4.28.

4.4.1 Control Strategy of ZSMC based UPFC

The trigger inputs to the MOSFETS are provided by a PI controller in a closed loop control. The gating pulses are obtained by pulse width modulation. The control schematic diagram is as shown in Fig 4.29.

**The SSSC part** or output of the matrix converter is operated in the Automatic Power Flow Control Mode. The SSSC injects a single phase ac voltage of controllable voltage magnitude and phase angle in series with the transmission line voltage.

The actual values of line voltage, line current, real power and reactive power are measured using VI and PQ Simulink Blocks. The desired values of the real and reactive power at the output end of the matrix converter are given as the reference values. The mismatch of real and reactive power obtained from the comparator is corrected in the PI controller. The controller generates the control inputs.

The output voltage range is decided by \( m \) and \( \rho \). The boost factor \( \rho \) is controlled by the duty cycle of the zero state and non shoot through active state. During the shoot through zero state, only zero voltage is
impressed on the converter. The remaining active period is determined by the modulation index. A modulation index for the required voltage transfer ratio is set as initial reference which determines the on/off periods of the trigger signal.

The reactive power mismatch produces the required displacement angle $\beta$. A phase locked loop (PLL) is used to determine the instantaneous relative phase angle $\theta$ of the line voltage and the current. For reactive power compensation, the injected voltage is given a phase angle shift with $\pi/2$ added leading or lagging to transmission line current emulating capacitive or inductive mode.

The **STATCOM part** or input to the matrix converter is responsible for regulation of the voltage at its point of coupling to the line. The STATCOM is operated in the Automatic Voltage Regulation Mode. The bus voltage magnitude is set as the reference and the actual value from the VI block is fed into the PI controller. The error signal produces the control signal to the STATCOM generator. The reactive power flow is due to the voltage difference across the transformer leakage reactance. Unity power factor is assumed on the input side of the matrix converter. Hence no reactive power exchange takes place on this side.
Fig. 4.28 Simulink Block Diagram of 1 Ph Dual Bridge Configured ZSMC based UPFC
Fig 4.29 Control Strategy of ZSMC based UPFC
4.4.2 MATLAB-Simulink Results of ZSMC based UPFC

A load of 50 MW, 20 MVAR is connected initially to bus 2. The load is then varied in steps. For different load variations there is a reduction in supply voltage and the line currents are found lagging. The UPFC is then connected to the line. A sudden peak load of 148% peak i.e. 74 MW and 30 MVAR is applied at 0.3 seconds through a circuit breaker.

The transmission line voltage and current during peak load and without UPFC connected are shown in the **Fig 4.30**. During peak load it is noted that the supply currents has risen in magnitude and lagging. The line voltage shows decrease in voltage magnitude.

After UPFC is connected, the voltage is restored to 300 KV peak as shown in **Fig 4.31**. A uniform profile of in phase voltage and current has been observed. The SSSC injected voltage is in phase with line voltage and lags the transmission line current at quadrature i.e. operating in capacitive mode is shown in **Fig 4.32**. The output voltage obtained at the matrix converter without using LC filter is as shown in **Fig 4.33A and Fig 4.33B**.

At the input end of the matrix converter the power factor measured is found to be 0.99 as shown in the power factor diagram **Fig 4.34**. Hence it is proved that the storage elements of the Z source impedance has compensated for the switching losses. It is to be emphasized here that for the conventional UPFC, the power factor is found to be 0.96.
Fig. 4.30 Transmission Line Voltage and Current during Peak Load condition

Fig. 4.31 Transmission Line Voltage and Current in phase with UPFC
Fig. 4.32 Injected SSSC Voltage and Transmission Line Current

Fig 4.33A ZSMC UPFC Output Voltage
Fig 4.33B ZSMC Output voltage with Trigger Pulses

Fig 4.34 Input Power Factor Diagram
4.5 LAB SCALE MODEL – PROPOSED ZSMC BASED UPFC

The complete block diagram of the experimental set up is illustrated in the Fig 4.35. A simple 2 bus single phase model has been chosen as the sample power system. A line is constructed with an impedance of X/R ratio 0.22, similar to a radial distribution line. A single phase voltage source of 24V, 100 VA is connected to the bus 1. A single phase induction motor rated at 24V, 1.2A is loaded to see the effect of matrix converter as UPFC. The input end of the matrix converter has been assumed at unity power factor. The output voltage from the matrix converter is synchronized to the input voltage at 24 V, 50 Hz at unity voltage transfer ratio, with varied phase shift

4.5.1 Construction and Hardware Wiring Circuit Diagram.

The matrix converter circuit is constructed using 4 MOSFET switches and anti parallel diodes. The Z source circuit consists of two inductors, two capacitors and one buck–boost MOFET switch. The switching frequency in the Z source circuit is several times more than the operating frequency. Hence the inductors and capacitors is very small size.

The complete hardware wiring diagram with matrix converter circuit, Z source circuit, driver circuit, zero detector circuit, power circuit and the microcontroller circuit is illustrated in the Fig 4.35. The hardware specifications are detailed in the Table 4.7.

The 8 bit microcontroller AT89C51 is programmed to generate
PWM signals to trigger 4 MOSFETS in the matrix converter and one number MOSFET in the Z source network through the gate driver circuit. The comparator provides a reference signal to generate trigger signals in synchronization with the supply voltage. The zero crossing of the ac supply is detected through ZCD. The program generates a pulsed signal at 50 HZ.

The magnitude of the injected voltage is varied by the modulation index in the matrix converter. A delay is obtained at the output of the matrix converter by adding a delay instruction before the start of the trigger. As the phase shift $\theta$ is increased introducing the time delay, the output voltage shifts with respect to supply voltage. LC components are used to obtain a smooth sinusoidal voltage to synchronize with ac input voltage.

![Hardware Block Diagram of ZSMC based UPFC](image)

**Fig 4.35 Hardware Block Diagram of ZSMC based UPFC**
4.5.2 Triggering Pulses – Algorithm

1. Start the program
2. Initialize port 1 as output
3. Initialize port 0 as input
4. Initialize ZCD output as interrupt
5. Initialize Port 3 for timer operation
6. Read the interrupt
7. Read the input
8. If input is positive, then send the positive triggering code to the output port
9. Set the time delay by time operation
10. Read Input
11. If the input is negative, then send negative triggering code to the output port
12. Set the time delay by time operation
13. Repeat the process for continuous pulses
14. End program
Fig. 4.36 Hardware Wiring Diagram – Power Circuit & Control Circuit of ZSMC
4.5.3 Experimental Results of ZSMC-UPFC

The complete experimental set up is depicted in the photo shot shown in Fig 4.37. The voltage at the output of matrix converter obtained in the CRO without using LC filters at 24V is shown in Fig 4.38. Using LC components the output voltage at the matrix converter is synchronised with the input voltage 24V, 50 Hz as depicted in Fig 4.39.

Fig. 4.37 Experimental Setup of ZSMC based UPFC

Fig. 4.38 ZSMC Output Voltage 24V at CRO
Fig. 4.39 ZSMC Output Voltage synchronized with Supply Voltage 24V

Table 4.7 ZSMC based UPFC Hardware Specifications

<table>
<thead>
<tr>
<th>Sl.No</th>
<th>Name of Component</th>
<th>Rating</th>
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| 1     | Transmission line | Input  = 24V  
R ohms, X = 3.33 ohms  
Step down Transformer = 230/24 V  
Load = 1 Ph induction Motor, 24V, 1.2A |
| 2     | Power circuit     | 1. Uncontrolled Rectifier Ckt (Diodes) = IN4007  
2. Supply voltage to Driver circuit, Opto Coupler circuit and ZCD = 240/15 V  
3. Supply voltage to Microcontroller = 230V/6V Trf |
| 3     | Z source Circuit  | Input voltage = 230/24V  
LC filter = Inductor – L1-10 µH  
Capacitor- C1- 22 pF  
Buck-Boost Switch = MOSFET IRF840-500 V, 10 A  
Switching Diode IN4500  
Z source circuit = L2,L3 - 10µH  
C2,C3-0.33 pF |
| 4     | 1 PH Matrix Converter UPFC | MOSFET = IRF840, 500V, 8A  
Switching Diodes = IN4500  
Shunt Step down Transformer = 230V/24V.  
Series Step up Transformer = 24V/230 V |
| 5     | Gate Driver circuit | IR2110 - 12 V |
| 6     | Micro Controller  | AT89C51- 8 bit |
| 7     | Isolation Circuit | Optocoupler-MCT2E |
| 8     | Zero Crossing detector (ZCD) with Comparator | LM 339(2 OR gates + 1 edge detector). |
4.6 SUMMARY OF SIMULATION AND EXPERIMENTAL RESULTS

The capability of ZSMC to boost input voltage 230 V to 340V, buck to 64V and attain unity voltage transfer ratio at 230V has been demonstrated in the PSPICE simulation results. A frequency changer is inherently a phase shifter and ZSMC has also illustrated its capability to link power systems at different frequencies. The results have shown output voltage at different frequencies 30 Hz, 100 Hz and 50 Hz.

The MATLAB-Simulink results have demonstrated the capabilities of the ZSMC as UPFC connected to the transmission line. The compensated voltage shows good synchronization with the line voltage.

Also the near unity power factor obtained at the input or STATCOM side of the matrix converter has proved that no real power is drawn by the converter. The storage elements of Z source have given the boost effect to the voltage transfer ratio. Thus the proposed ZSMC based UPFC model has the capability to compensate for the real power loss associated with converters switching, without drawing from the transmission line unlike in the case of traditional VSC and conventional Matrix Converter based UPFC.

The experimental results have illustrated synchronization of the output voltage at unity voltage transfer ratio with the 24V input voltage at the required phase shift. Thus a good correlation between the experimental results and the simulation results has been observed.