CHAPTER 3

Efficiency Improvement Using Flexible Output SSPA for Space Use

3.1 Objective:
The SSPAs used so far in satellite communication are with fixed output power with efficiency of the order of 30% at specified output power (fixed). But when operated at back-off, the efficiency reduces to around 20% so a large amount of DC power is wasted as a heat leading to degrade thermal management.

Depending upon coverage area and user requirement, the power amplifier is selected for satellite transponder design. A common practice is to design a payload with state-of-the-art sub-systems available in the market. For example, 100 watt SSPAs for UHF-band, 40 watt SSPAs for L-band and 15 watt SSPAs for C-band are available off-the-shelf with space heritage design. They are commonly selected for satellite transponder design. Anything different from the off-the-shelf space heritage product needs new design and new qualification leads to impact on cost and schedule.

The following examples show the applications where flexible output power SSPAs are needed.
(i) Depending upon the output power requirement, SSPAs with different output power are designed.
(ii) The Direct to Home (DTH) Television reception is highly distorted and sometimes the Television reception is fully lost due to rain fading of the signal (especially when the communication is at Ku and Ka Band).
(iii) Similarly in the low traffic regions such as above sea or low populated areas and multi-carrier operations the SSPAs are operated at back-off.

In all these applications, the efficiency is very low at back-off. Suppose in future, there is a requirement of higher output power from the payload, one cannot increase the power by any means in the so far designed SSPAs.
Table 3.1.1 SSPA Efficiency under Back-off

Table 3.1.1 shows the relationship between the input back-off with the DC power consumption and Power Added Efficiency (PAE, $\eta_{\text{add}}$) of 20 Watt GaAs FET SSPA developed for space applications. DC power consumption does not reduce at the same rate as output power. So efficiency reduces drastically at every 3 dB output power back-off. To improve the efficiency under back-off condition the DC power consumption has to be reduced. This leads to need for Flexible output power SSPA.

**Target Specifications of Flexible output power SSPA:**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>20 watt GaAs FET SSPA</th>
<th>200 watt GaN HFET SSPA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>3700-3900 MHz</td>
<td>1250-1350 MHz</td>
</tr>
<tr>
<td>Gain @ 2 dB GCP</td>
<td>12 dB</td>
<td>14 dB</td>
</tr>
<tr>
<td>P_{out}</td>
<td>40 dBm (10 watt)</td>
<td>53 dBm (200 watt)</td>
</tr>
<tr>
<td>PAE at nominal P_{out}</td>
<td>40 %</td>
<td>55 %</td>
</tr>
<tr>
<td>Improvement in PAE at 3 dB B/O</td>
<td>5 %</td>
<td>5 %</td>
</tr>
</tbody>
</table>

Table 3.1.2 Targeted Specifications of flexible output power SSPA

Two types of the SSPAs were designed for demonstration of this concept. Initially the SSPA was designed using Gallium Arsenide (GaAs) MESFET device delivering 20 Watt RF output power and later another amplifier was designed using state of the art technology Gallium Nitride (GaN) HFET device delivering 200 watt RF output power. The power added efficiency degradation at 3 dB output back off was of the order of 14 % and 10 % for 20 Watt and 200 Watt device respectively. Based on the theoretical analysis, the target specification for efficiency improvement was set for 5 % at 3 dB back off. Table 4.1.2 gives the detail of major targeted specifications of 20 Watt as well as 200 Watt SSPAs.
3.2 Theoretical Background:

The different classes of operation of amplifiers are A, B, AB, C, D, E and F. For satellite applications class AB is preferred for optimum performance in terms of better linearity and efficiency. The following explanation demonstrates the relation of the efficiency at saturation and at back off for fixed drain voltage. [1]

Under ideal fixed voltage class B operation, the DC input power or DC power consumption (P_{dc}), defined by product of drain current (I_{ds}) and drain voltage (V_{ds}) is a function of the drain current amplitude and the drain voltage is given by

$$P_{dc} = \frac{\Delta I}{\pi} \cdot V_D$$  \hfill (1)

The RF output power is given by

$$P_{out} = R_L \cdot \frac{\Delta I^2}{8}$$  \hfill (2)

Where R_L is the class B load resistance at any given drive level an optimal drain voltage exists that maximizes the output power, such that

$$V_D = \sqrt{2 \cdot R_L \cdot P_{out}} + V_k$$  \hfill (3)

Where V_K is the knee voltage. The Knee Voltage is not the fixed value commonly determined from a curve tracer measurement.

From Equation (1), (2) & (3), the drain efficiency of the ideal class B amplifier under Back-off, with fixed drain bias becomes

$$\eta_{d}^{fixed} = \frac{\pi}{4} \cdot \left( \frac{1 - \alpha}{1 + \alpha} \right) \cdot \sqrt{\beta}$$  \hfill (4)

Where \( \alpha = \frac{V_k}{V_{bk} - V_{po}} \) and represents the FET “ideally factor” and \( \beta = \frac{P_{out}}{P_{out} \ max} \), the back-off ratio.

For the same amplifier with optimal variable drain bias,

$$\eta_{d}^{var} = \frac{\pi}{4} \cdot \frac{1}{\frac{2\alpha}{1 + \frac{2\alpha}{(1 - \alpha) \sqrt{\beta}}} \right)$$  \hfill (5)

The ratio of drain efficiency of the two operating modes is now given by
\[
\frac{\eta_d^{Var}}{\eta_d^{fixed}} = \frac{1 + \alpha}{(1 - \alpha) \cdot \sqrt{\beta} + 2\alpha}
\] (6)

For an ideal device (\(\alpha = 0\)), the ratio is always greater than 1 indicating higher efficiency under “extended saturation” operation. Thus above discussion shows that the SSPA offers higher efficiency at saturation as compared to the back-off condition. The amount of saturation is defined by the term Gain Compression which is an amount of the gain reduction from the back-off to nominal operating condition. Thus the efficiency at back off is lower as compared to the saturation. [2-5]

The DC power consumption of the devices can be changed by either changing the Drain voltage \(V_{ds}\) or by changing the Drain Current \(I_{ds}\). The drain current can be changed by changing gate-to source voltage \(V_{gs}\). Changing the gate voltage changes the gain of the amplifier which needs additional gain adjustment circuit which is not advisable for space hardware. Hence, drain voltage is varied in most cases which require critical design challenges to ensure the amplifier’s unconditional stability. The Electronic Power Conditioner (EPC) has been designed according to the required drain voltages which is described in [6-7]. In the successive section, high power amplifier has been described in detail using Automated Design Software (ADS).

3.3 Design, Optimization and Simulation

In order to demonstrate the concept, two types of the devices (1) GaAs MESFET (2) GaN HEMT were selected for designs. Out of these two, design of a high power amplifier using GaN HEMT has been presented here whereas only results of GaAs MESFET amplifier are listed.

The concept of flexible output power SSPA has been demonstrated in the following steps.
1. Selection of Power device (GaN, GaAs or MOSFET)
2. Design of an amplifier with conjugate match and load pull match using Harmonic Balance
3. Characterization of amplifier under for dynamic biasing
4. Collection of data (look up table) for programming into storage device
5. Testing and results

For Power amplifiers, GaAs semiconductor materials were widely used so far but due to lower band gap energy, they could not be operated beyond 9 volts. Hence many of them were used in parallel to get higher power resulting in lower efficiency.

Si based RF MOSFETs were also used for power amplifications as they could be operated at 28 volts but due to limitations of Si, they could not be used beyond 2 GHz.
This called for innovation of a newer material with wider bandgap energy which can be operated at higher frequencies.

With innovations of Gallium Nitride (GaN) semiconductor, it has now become possible to design and develop high power amplifier with excellent performance.

3.4 Power Amplifier Design using GaN:

The active device used in this amplifier is 180W Gallium Nitride based High Electron Mobility GaN-HEMT Transistor from Cree (CGH40180), a large signal model and has following features.

- 28 V to 32 V Operation
- Up to 2.4 GHz operation availability
- Small signal gain of 16 dB at 2.0 GHz
- Saturated Power of 180 W and 60 % Efficiency at this level

Thanks to wide bandgap of GaN, power density of the material is 10 to 20 times higher than GaAs-based devices. Hence the GaN components are much smaller and exhibiting low capacitance characteristics.

The Amplifier is designed with the help of non-linear model of the device on Advanced Design Software (ADS) platform. The following steps were performed but only load pull design is explained in detail.

1. Biasing the device
2. Stability Analysis
3. Selection of Load and Source Impedances
4. Design of matching network to check performance of device when it is conjugate matched
5. Using Load Pull Technique to find the optimum load impedance.
6. Design of Matching Network after finding the optimum load impedances.
7. Combining the two sides of the Amplifier.
8. Fabrication and measurement.
9. Practically measured results.

3.5 Finding optimum impedance through Load Pull

In the load-pull measurement, the performance of the device is tracked through varying source and/or load impedances. Impedance values are varied by the means of either manual or automatic tuners which are controlled by a computer. The computer then fits the measured performance parameters on a gamma source or gamma load plane. Appropriate impedances for source and load are then determined so that the matching networks can be designed. In
this project the load pull measurements were carried out by using the design guide given in the ADS 2008 with the help of the nonlinear model.

Load pull simulations can be done in ADS using HB1Tone_LoadPull design guide with a large-signal/non-linear model of transistor. For this work, a large signal model of 120 watt GaN HFET is used. This device is used for the load pull analysis as this device has the same characteristics as that of 200 watt GaN HFET, the only difference is that two 120 watt devices are combined to make 200 watt device. Fig 3.5.1 shows the simulation setup from this design guide and resulting load-pull contours for output power and PAE as a function of load impedance. Figure 3.5.2 shows the chart for the process of this harmonic balance simulation.

In Fig 3.5.3 each contours indicates the set of impedances corresponding to a constant output power or PAE.

Fig 3.5.1: Setup for Load Pull Analysis

The below load-pull circuit uses harmonic balance simulation in ADS. This iterative simulation calculates the response of large signal circuits driven by either single or multiple sources and tries to find a stationary solution for the non-linear system in the frequency domain.
Fig 3.5.2 Flow Chart of Harmonic Balance Simulation

The output power from the power match condition at 2dB compression point obtained through the load pull technique. The impedance was found to be (3.063 – j*0.940) Ω. The matching network was designed to transform the source and load impedance to the 50Ω line using Smith chart, found to be (1.058 – j*3.454) Ω and (3.063 – j*0.940) Ω respectively.
3.6 Combining the two sides of the amplifier:

The two sides of the amplifier can be combined either by using the Wilkinson power divider. The two input sides are fed power in phase through a 3dB equal power divider & the output power from the two output sides are combined with the help of the combiner that was matched to the 50Ω line. The gain was found satisfactory however the input return loss was not good. In order to improve the return loss extra 90° line was added to the input and the output to make the amplifier work in the balanced configuration. The Electromagnetic-Circuit co-simulation feature enables to combine EM and circuit simulations from the schematic. After this configuration the output power achieved at 1dB and 2dB compression point as shown in fig 3.6.1 by markers (m5 & m6) and (m51 & m53) respectively. At one 1dB compress the output power is 51.957 dBm (156W) however at 2dB compression point we are able to achieve 53.0 dBm (199.897W) which is close to 200Watts. Fig 3.6.2 shows the large signal gain at 1dB and 2 dB Compression points. The amplifier has a flat gain for small signals and decreases as the compression is increased.
(i) Power Added Efficiency (PAE):

Fig 3.6.3 gives the PAE at 1dB& 2dB compression point which clearly shows the improvement in the power added efficiency from 52.7% to 58.4% as one move into compression. It shows that the PAE increases as the input power increases then reaches at the peak point and then degrades when further the input power is increased which is obvious because at the saturation the output power will not increase but the D.C power and the applied input power will keep on increasing.

![Graph showing Power Added Efficiency (PAE)](image)

(ii) AM-PM Conversion and Tone IMD Test:

Another parameter of interest is AM/PM conversion, which is a prime factor in determining Bit Error Rate (BER). Ideally output phase should be independent of input power. But, as device is operated in non-linear region, output phase changes with change in input power. From the above Fig.3.6.3 it follows that the AM-PM Conversion is 0.516°/dB at 1 dB compression. As shows the 3rd order Inter Modulation Products (IMD) for 1dB compression point at very closely spaced frequencies which are 1.3GHz & 1.299GHz.

3.7 ADS Layout

After obtaining the simulation results the input and the layout of the input and output matching networks were realized in the ADS. Layout of the high power stage is shown below in Fig. 3.8.
3.8 Fabrication:
The layout was exported as Gerber files from ADS and it was milled on a printed circuit board known as PCB. The test box was prepared so that the device can be mounted properly and the heat generated can be dissipated fast.

![Fig.3.8 Layout of the Power Amplifier](image)

3.9 Measured results:
The response of the amplifier was measured with the help of PNA-X and was found to be closely matching with the simulated values. The amplifier was tested for different drain voltage and different gain settings to collect the data to store in EEPROM controller. The results are mentioned in the following tables in the next section. Important observations are as follows.

When the device is operated at back-off, it suffers from the following disadvantages.
- Efficiency of the device is decreasing.
- Chanel temperature is increasing that is affecting the reliability of the device
- The device gain has increased that affects the overall system gain.
- The device has come out of the compression, making the output of the amplifier change with the slight change in the input applied to the amplifier.

So in order to improve the performance of the device simultaneously not affecting the overall system gain of the amplifier the device again needs to be operated at the compression. This can either be done either by reducing the device bias voltage either the drain voltage or the gate voltage.

By reducing the bias voltage, following advantages are obtained:
- Power dissipation has reduced which in turn has resulted in the improvement of the device channel temperature.
• As the channel temperature has decreased, it means that the reliability of the device has improved.
• The gain of the amplifier is constant, so the overall system gain is same even at the back-off.
• The device is again running in the compression so the fluctuation is the output power is less with the fluctuation in the input drive level.

3.10 Dynamic (Adaptive) Bias approach:
Some sort of controller is required which will vary the drain voltage in accordance with input power back-off. This has been realized as follows.
The RF input power was monitored using a coupler and this coupled power was converted into DC voltage using RF detector. This detected signal was used for reference signal for the dynamic biasing controller. The dynamic biasing controller consists of A/D converters, PROMs, a PROM controller and D/A converters, which provide control voltage for drain.
The block diagram of SSPA with Dynamic Bias approach is shown in Fig 3.10.

![Block diagram of SSPA with dynamic bias approach](image)

3.11 Realization and testing of Amplifier with EEPROM controller
As compared to the ground application, selection of the components with space qualification and Radiation Hardening (Rad-Hard) is critical and hence very limited choice is available. Two types of amplifiers (1) 20 watt GaAs MESFET amplifier and (2) 200 watt GaN HFET amplifier were tested and results are presented below. Table 3.11.1 presents look up table required to be burn-in into the EEPROM controller for different RF input drive levels for 20-watt amplifier and Table 3.11.2 presents the DC power consumption and efficiency improvement for different drive levels.
Table 3.11.1 Typical look up table for 20 watt GaAs MESFET amplifier (for EEPROM controller).

<table>
<thead>
<tr>
<th>Output of ADC (volt)</th>
<th>Input to DAC (volt)</th>
<th>RF Input power level</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>9.0</td>
<td>Nominal RF input</td>
</tr>
<tr>
<td>3.5</td>
<td>7.73</td>
<td>1 dB input back-off</td>
</tr>
<tr>
<td>3.0</td>
<td>6.96</td>
<td>2 dB input back-off</td>
</tr>
<tr>
<td>2.5</td>
<td>6.25</td>
<td>3 dB input back-off</td>
</tr>
<tr>
<td>2.0</td>
<td>5.74</td>
<td>4 dB input back-off</td>
</tr>
<tr>
<td>1.5</td>
<td>5.40</td>
<td>5 dB input back-off</td>
</tr>
</tbody>
</table>

Table 3.11.2 Improvement in Efficiency and power consumption for 20-watt device

<table>
<thead>
<tr>
<th>Pin (dBm)</th>
<th>Efficiency improvement (%)</th>
<th>DC power improvement (watt)</th>
</tr>
</thead>
<tbody>
<tr>
<td>18 (Nominal)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>17</td>
<td>1.49</td>
<td>2.19</td>
</tr>
<tr>
<td>16</td>
<td>5.19</td>
<td>4.64</td>
</tr>
<tr>
<td>15</td>
<td>6.91</td>
<td>5.52</td>
</tr>
<tr>
<td>14</td>
<td>6.80</td>
<td>5.66</td>
</tr>
<tr>
<td>13</td>
<td>6.22</td>
<td>5.63</td>
</tr>
</tbody>
</table>

The DC power saving of about 5 Watt at 3 dB input back-off (7 % efficiency improvement) for 20 watt SSPA is quite considerable for on-board applications.

Similar concept when applied to higher power SSPA where the drain voltage of the driver stage of the final stage can also be varied in addition to that of final device, the improvement number is of the order is 10 %.

The GaN amplifier (200 watt) designed above was tested and the amount of DC power saving is shown in the following Tables 3.11.3 and 3.11.4.

Table 3.11.3 Test data for 200 watt GaN Device without dynamic bias

<table>
<thead>
<tr>
<th>$P_{in}$ (dBm)</th>
<th>$P_{out}$ (dBm)</th>
<th>IRF (Amp)</th>
<th>VDC (volt)</th>
<th>$P_{dc}$ (watt)</th>
<th>$P_{out}$ (watt)</th>
<th>$\eta$(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>39</td>
<td>53.0</td>
<td>11.7</td>
<td>28</td>
<td>327.6</td>
<td>200</td>
<td>58.5</td>
</tr>
<tr>
<td>38</td>
<td>52.6</td>
<td>11.1</td>
<td>28</td>
<td>310.8</td>
<td>182</td>
<td>56.3</td>
</tr>
<tr>
<td>37</td>
<td>52.0</td>
<td>10.3</td>
<td>28</td>
<td>288.4</td>
<td>156</td>
<td>52.7</td>
</tr>
<tr>
<td>36</td>
<td>51.2</td>
<td>9.4</td>
<td>28</td>
<td>263.2</td>
<td>132</td>
<td>48.2</td>
</tr>
</tbody>
</table>

Table 3.11.4 Test data for 200 watt GaN Device with dynamic bias
As seen from above tables, for a single stage high power amplifier the efficiency improvement is about 7 % for 3 dB output back-off. When the same concept is applied to its driver stage (in this case it is 20 Watt device), additional improvement of the order of 3 % is achieved resulting an overall improvement of 10 % at 3 dB back off. This will allow the SSPA designer to compete the TWTA in terms of efficiency in addition to mass, volume and cost and replace the TWTA.

**Comparison between targeted and achieved performance with dynamic biasing:**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Target Specifications</th>
<th>Achieved performance</th>
</tr>
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<tr>
<td>Frequency</td>
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</tr>
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<tr>
<td>PAE at nominal Pout</td>
<td>40 %</td>
<td>42 %</td>
</tr>
<tr>
<td>Improvement in PAE at 3 dB B/O</td>
<td>5 %</td>
<td>7 %</td>
</tr>
</tbody>
</table>

Table 3.11.5 Targeted versus achieved performance for 20 watt GaAs Device with dynamic bias

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Target Specifications</th>
<th>Achieved performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>1250-1350 MHz</td>
<td>1250-1350 MHz</td>
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<tr>
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<td>14 dB</td>
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<td>$P_{\text{out}}$</td>
<td>53 dBm (200 watt)</td>
<td>53 dBm (200 watt)</td>
</tr>
<tr>
<td>PAE at nominal Pout</td>
<td>50 %</td>
<td>58 %</td>
</tr>
<tr>
<td>Improvement in PAE at 3 dB B/O</td>
<td>5 %</td>
<td>7 %</td>
</tr>
</tbody>
</table>

Table 3.11.6 Targeted versus achieved performance for 200 watt GaN Device with dynamic bias

The above Tables 3.11.5 and 3.11.6 compare the achieved performance with the targeted specifications and can be seen from the tables that the achieved performance is better than the expected for efficiency improvement at 3 dB back off.

Similar work, “Flexible S-Band SSPAs for Space Applications” has been reported by A. Darbandi. In this work only conceptual block schematic and measured results are presented.
but do not give any design detail regarding the technique by which the flexibility is achieved. The reported improvement in efficiency is 7% whereas in present case, the improvement is 7% only for the final stage, which is 10% when the same technique is applied to it’s driver stage.
3.12 Conclusion
The concept of the flexible output power SSPA has been demonstrated using GaAs and GaN devices with hardware realization for on-board space applications. The overall efficiency improvement achieved is 10 % which is higher than the reported number of 7 %. It can be seen from the measured results that a considerable amount of DC power, 5 Watt in 20 watt SSPA and 90 Watt in 200 watt SSPA, at 3dB input back-off can be saved using this approach. This will result in saving of DC power generation on-board and hence the launching cost. Using this SSPA the satellite transmit power can be varied automatically to meet the losses due to atmosphere and rain fading. The reliability of the device also can be improved by reducing its drain voltage and channel temperature. This is considered as a remarkable power saving for space application and also the significant technique to improve the link availability for DTH application. In addition to efficiency improvement, it provides flexibility in terms of output power which will help the satellite users to update themselves with the rapidly changing technology.