The ULN2803A is a high-voltage, high-current Darlington transistor array. The device consists of eight npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be connected in parallel for higher current capability.

Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>TA</th>
<th>PACKAGE</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40°C to 85°C</td>
<td>PDIP (N)</td>
<td>ULN2803AN</td>
<td>ULN2803AN</td>
</tr>
<tr>
<td></td>
<td>SOIC (DW)</td>
<td>ULN2803ADW</td>
<td>ULN2803A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reel of 2000</td>
<td></td>
</tr>
</tbody>
</table>

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

- Collector-emitter voltage: 50 V
- Input voltage (see Note 1): 30 V
- Continuous collector current: 500 mA
- Output clamp diode current: 500 mA
- Total substrate-terminal current: -2.5 A
- Package thermal impedance, θJA (see Notes 2 and 3): TBD°C/W
- Operating virtual junction temperature, Tj: 150°C
- Storage temperature range, Tstg: -65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal GND.
2. Maximum power dissipation is a function of Tj(max), θJA, and TA. The maximum allowable power dissipation at any allowable ambient temperature is PD = (Tj(max) - TA)θJA. Operating at the absolute maximum Tj of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICEX</td>
<td>Collector cutoff current</td>
<td>VCE = 50 V, l</td>
<td>= 0, See Figure 1</td>
<td>50</td>
<td>pA</td>
</tr>
<tr>
<td>I(off)</td>
<td>Off-state input current</td>
<td>VCE = 50 V, TA = 70°C, I(c) = 500 µA, See Figure 2</td>
<td>50</td>
<td>65</td>
<td>µA</td>
</tr>
<tr>
<td>I(on)</td>
<td>Input current</td>
<td>VCE = 2 V, See Figure 3</td>
<td>0.93</td>
<td>1.35</td>
<td>mA</td>
</tr>
<tr>
<td>V(on)</td>
<td>On-state input voltage</td>
<td>VCE = 2 V, See Figure 4</td>
<td>I(c) = 200 mA</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td>VCE(sat)</td>
<td>Collector-emitter saturation voltage</td>
<td>l</td>
<td>= 250 µA, See Figure 5</td>
<td>I(c) = 100 mA</td>
<td>0.9</td>
</tr>
<tr>
<td>IRL</td>
<td>Clamp diode reverse current</td>
<td>VR = 50 V, See Figure 6</td>
<td>50</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>VF</td>
<td>Clamp diode forward voltage</td>
<td>IF = 350 mA, See Figure 7</td>
<td>1.7</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>CI</td>
<td>Input capacitance</td>
<td>VCE = 0 V, f = 1 MHz</td>
<td>15</td>
<td>25</td>
<td>pF</td>
</tr>
</tbody>
</table>

switching characteristics at 25°C free-air temperature

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IpLH</td>
<td>Propagation delay time, low- to high-level output</td>
<td>VG = 50 V, RL = 163 Ω, See Figure 8</td>
<td>130</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>IpHL</td>
<td>Propagation delay time, high- to low-level output</td>
<td>CG = 15 pF, See Figure 8</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>VOH</td>
<td>High-level output voltage after switching</td>
<td>VG = 50 V, IO = 300 mA, See Figure 9</td>
<td>VG - 20</td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

TEXAS INSTRUMENTS
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PARAMETER MEASUREMENT INFORMATION

Figure 1. $I_{CEX}$ Test Circuit

Figure 2. $I_{(off)}$ Test Circuit

Figure 3. $I_{I(on)}$ Test Circuit

Figure 4. $V_{(on)}$ Test Circuit

Figure 5. $h_{FE}$, $V_{CE(sat)}$ Test Circuit

Figure 6. $I_{R}$ Test Circuit
PARAMETER MEASUREMENT INFORMATION

Figure 7. $V_F$ Test Circuit

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_0 = 50 \Omega$
B. $C_L$ includes probe and jig capacitance.
C. $V_{IH} = 3 \text{ V}$

Figure 8. Propagation Delay Times
PARAMETER MEASUREMENT INFORMATION

Test Circuit

Voltage Waveforms

NOTES:
A. The pulse generator has the following characteristics: PRR = 12.5 KHz, Z₀ = 50 Ω.
B. Cᵢ includes probe and jig capacitance.
C. VᵢH = 3 V

Figure 9. Latch-Up Test
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
D. Falls within JEDEC MS-013 variation AB.
<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ULN2803ADW</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>18</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU Level-2-260C-1YEAR</td>
<td></td>
</tr>
<tr>
<td>ULN2803ADWR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>18</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU Level-2-260C-1YEAR</td>
<td></td>
</tr>
<tr>
<td>ULN2803AN</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>18</td>
<td>20</td>
<td>Pb-Free (RoHS)</td>
<td>CU NIPDAU Level-NC-NC-NC</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
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Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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MECHANICAL DATA

PLASTIC DUAL-IN-LINE PACKAGE

N (R-PDIP-T**)

16 PINS SHOWN

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.
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<th>Applications</th>
</tr>
</thead>
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<td>Audio</td>
</tr>
<tr>
<td>Data Converters</td>
<td>Dataconverter.ti.com</td>
<td>Automotive</td>
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<tr>
<td>DSP</td>
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<td>Broadband</td>
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<td>Logic</td>
<td>logic.ti.com</td>
<td>Military</td>
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<td>Power Mgmt</td>
<td>power.ti.com</td>
<td>Optical Networking</td>
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<tr>
<td>Microcontrollers</td>
<td>microcontroller.ti.com</td>
<td>Security</td>
</tr>
</tbody>
</table>

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