3.1 Introduction

The methodology of this research work is divided into two sections one is hardware implementation and the other is software implementation. The hardware implementation consists of the development of ARM cortex-m3 processor based control and interlock system.

ARM cortex-m3 is a low-power processor that features low gate count, low interrupt latency, and low-cost debug intended for deeply embedded applications that requires fast interrupt response features. ARM cortex-m3 is with ARMv7-M architecture [1]. The 32-bit (Cortex-Mx based) device architecture delivers the art implementations for FPGAs and SoCs. With the improved Thumb2 instruction set, cortex-m3 microcontrollers support a 4GB address space, provide bit-addressing (bit-banding), and interrupts with at least 8 interrupt priority levels. The inbuilt ethernet controller is used to send and receive the data or commands from embedded target board to a personal computer.

The subsequent paragraphs provide information on transmitter amplifier sensors functional details and interfacing of sensors output to ARM board and finally with centralized monitoring and control system connected through the web.

The software implementation is focused on web page design with the help of ASP.Net, background TCP/IP programming with C#, ARM processor web server and I/O controls programming with embedded C, card logic using Keil-4 IDE embedded ‘C’ [2]. The meticulous description of software implementation is presented in chapter 4.
3.2 ARM Cortex-M3 System Hardware Design

ARM cortex-m3 microcontroller acts like the brain of web based remote monitor and controller system for MST radar transmitters. The heart of monitoring and controlling of the safety interlock system is sensors network in transmitters. The ARM cortex microcontroller embedded target board interfaces between the radar transmitters and remote computer system for safe monitoring of transmitter’s health condition of the remote web server. The web based centralized system monitors the status of all 32 transmitters remotely. Recording of all sensor data at remote computer’s database by using MS-SQL database system [4] through web server running on the personal computer ensures proper functioning of the control and interlock system in transmitters for safety. It provides correct number of transmitter’s availability and their power level that is very essential for radar experiments as per radar equation, ‘Power transmitted (Pt)’. Central computer monitors 32 high power triodes based transmitter’s health status, by using 400-sensors data through ethernet and provides total transmitted power (P_t) data to scientists.

Figure 3.1: Block diagram of the Web based Radar Transmitters
Figure 3.1 gives the overall structure of control and monitoring system for transmitters. The MST radar technical details have been presented in chapter 1 and further hardware description related to sensors for control and interlock are discussed with subtitle “Transmitter Hardware Interface”.

**ARM Cortex-M3 Processor:** LM3S9B96 is an ARM Cortex-M3 based microcontroller with a high level integration and low power consumption having portability and optimized architecture for small-footprint embedded applications. Its small size and sufficient output ports and multiple ADC channels, ethernet communication compatibility can be programmed and reprogrammed easily using a JTAG debugger.

LM3S9B96 is widely available with development tools, System-on-Chip (SoC) infrastructure. Microcontroller uses ARM Thumb compatible and Thumb-2 instruction set to reduce memory requirements. LM3S9B96 microcontroller is code-compatible with all members of the extensive Stellaris family [5]. Texas Instruments offers a complete solution with evaluation and development boards, application notes, easy-to-use peripheral driver library, and support. Figure 3.2 provides all functional blocks of the LM3S9B96 microcontroller. The detailed description of functional blocks follows the block diagram.
Figure 3.2: LM3S9B96 Microcontroller Block diagram
3.2.1 General Purpose Input/Outputs (GPIOs)

The GPIO module is composed of nine physical GPIO blocks, each corresponding to an individual GPIO port (Port A, Port B, Port C, Port D, Port E, Port F, Port G, Port H, Port J). Each GPIO port is a separate hardware instantiation of the same physical block, all pins need not be implemented on every block; some GPIO pins can function as I/O signals for the on-chip peripheral modules. The GPIO module supports up to 65 programmable input/output pins depending on the peripherals being used. The highly flexible pin-muxing allows a pin as GPIO or one of several peripheral functions. The input configuration is 5v tolerant and has a fast toggle capable of a change in every two clock cycles. There are two port accesses that are Advanced High Performance Bus (AHB) with a better back-to-back accessible performance and Advanced Peripheral Bus (APB) for the backwards compatibility with existing code. The bit masking performs read and write operations through address lines. GPIOs also used to initiate an ADC sample sequence; and pins configured as Schmitt-triggered digital inputs.

The programmable control for GPIO, pad configurations are the weak pull-up or pull-down resistors. The current 2-mA, 4-mA, and 8-mA pad drive for digital communication up to four pads can sink 18-mA for high-current applications. The slew rate is controlled for 8-mA drives.

Figure 3.3 provides the schematic of Microcontroller GPIOs used for sensors in the transmitter. The ADC0 to ADC15 are used for getting analog sensors data from the transmitter. The PJ5, PJ7, PH5, PF4, PF0, PE0, PWM6 and PWM7 pins are configured as a general purpose outputs used for controlling the Anode supplies, Tx ON/OFF and RF ON/OFF switching. The OSC0 is the main oscillator crystal input or
an external clock reference input and OSC1 main oscillator crystal output. The XTALNPHY and XTALPPHY oscillator crystal is used for ethernet purpose.

**Figure 3.3:** Schematic diagram of LM3S9B96 microcontroller

### 3.2.1.1 Functionality of GPIOs

The GPIO signals have analog and digital alternate hardware functions. The AINx and VREFA analog signals are goes through an isolation circuit before reaching their circuitry. These signals are configured by clearing the corresponding DEN bit in the GPIO Digital Enable (GPIODEN) register and setting the corresponding AMSEL bit in the GPIO Analog Mode Select (GPIOAMSEL) register. The 5V tolerant analog signals are connected directly to their circuitry are configured by clearing the DEN bit in the GPIO Digital Enable (GPIODEN) register. All GPIO signals are 5V tolerant, when configured as inputs except for PB0 and PB1 which are limited to 3.6V. The
digital alternate hardware functions are enabled by setting the appropriate bit in the GPIO Alternate Function Select (GPIOAFSEL) and GPIODEN registers. While configuring the PMCx bit field in the GPIO Port Control (GPIOPCTL) register, each pin has been programmed individually [5].

The data control registers allow software to configure the operational modes of the GPIOs. GPIO Direction (GPIODIR) register is the data direction register. Setting a bit in the GPIODIR register configures the corresponding pin to be an output while clearing a bit configures the corresponding pin to be an input. All bits are cleared by a reset, which means all GPIO pins are inputs by default.

**Data Register Operation:** In software control mode, values written in the data register GPIO DATA are transferred onto the GPIO port pins if the respective pins have been configured as outputs through the GPIO Direction (GPIODIR). The GPIO ports allow the modification of individual bits in the GPIO Data (GPIO DATA) register by using bits [9:2] of the address bus as a mask. In this manner, software drivers can modify individual GPIO pins in a single instruction without affecting the state of the other pins. This method is more efficient than the conventional method of performing a read-modify-write operation to set or clear an individual GPIO pin. To implement this feature, the GPIO DATA register covers 256 locations in memory map. During a write operation, if the address bit is associated with the data bit that is set, the value of the GPIO DATA register is altered. If the address bit is cleared, the data bit is left unchanged.
3.2.1.2 GPIO Interrupt Control

The interrupt capabilities of each GPIO port are controlled by a set of seven registers. The source of the interrupt using these seven registers is selected with its polarity and edge properties. When one or more GPIO inputs cause an interrupt, a single interrupt output is sent to the interrupt controller for the entire GPIO port. For edge-triggered interrupts, software must clear the interrupt to enable any further interrupts. For a level-sensitive interrupt, the external source must hold the level constant for the interrupt to be recognized by the controller.

Three registers are used to define the edge or sense that causes GPIO interrupts; Interrupt Sense (GPIOIS) register, GPIO Interrupt Both Edges (GPIOIBE) register, and GPIO Interrupt Event (GPIOIEV) register. The interrupts are enabled or disabled via GPIO Interrupt Mask (GPIOIM) register. When an interrupt condition occurs, the state of the interrupt signal can be viewed in two locations that are, GPIO Raw Interrupt Status (GPIORSIS) and GPIO Masked Interrupt Status (GPIOMIS) registers. As the name implies, the GPIOMIS register only shows interrupt conditions that are allowed to be passed to the interrupt controller. The GPIORSIS register indicates that a GPIO pin meets the conditions for an interrupt, but has not necessarily been sent to the interrupt controller. Interrupts are cleared by writing 1 to the appropriate bit of the GPIO Interrupt Clear (GPIOICR) register.

When programming the interrupt control registers (GPIOIS, GPIOIBE, or GPIOIEV), the interrupts should be masked (GPIOIM cleared). Writing any value to an interrupt control register can generate a spurious interrupt if the corresponding bits are enabled.
**Trigger Source at ADC:** The port B (PB4) can also be used as an external trigger for the ADC. If PB4 is configured as a non-masked interrupt pin (the appropriate bit of GPIOIM is set), an interrupt for Port B is generated, and then an external trigger signal is sent to the ADC. If the ADC Event Multiplexer Select (ADCEMUX) register is configured to use the external trigger, an ADC conversion is initiated. If no other Port B pins are being used to generate interrupts, the Interrupt 0-31 is Set Enable (EN0). The register can disable the Port B interrupts, and the ADC interrupt can be used to read back the converted data. Otherwise, the Port B interrupt handler must ignore and clear interrupts on PB4 and wait for the ADC interrupt, or the ADC interrupt must be disabled in the EN0 register and Port B. The interrupt handler must poll the ADC registers until the conversion is completed.

### 3.2.1.3 GPIO Mode Control

The GPIO pins are controlled by either software or hardware. Software control is default for most of the signals and corresponds to the GPIO mode where the GPIODATA register is used to read or write the corresponding pins. When hardware control is enabled via GPIO Alternate Function Select (GPIOAFSEL) register, the pin state is controlled by its alternate function (that is, the peripheral). Further, pin MUX options are provided through the GPIO Port Control (GPIOPCTL) register which selects one of several peripheral functions for each GPIO for information on the configuration options.

### 3.2.1.4 GPIO Commit Control

The commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. The protection is provided for the NMI pin (PB7) and the four JTAG/SWD pins (PC [3:0]). It writes to protected bits of the
GPIO Alternate Function Select (GPIOAFSEL) register. The GPIO Pull-Up Select (GPIOPUR) register, GPIO Pull-Down Select (GPIOPDR) register, and GPIO Digital Enable (GPIODEN) register are not committed to storage.

3.2.1.5 GPIOs Initialization and Configuration

The GPIO modules can be accessed via two different memory apertures. The legacy aperture, the Advanced Peripheral Bus (APB) are backwards-compatible with previous Stellaris parts. The other aperture, the Advanced High-Performance Bus (AHB), offers the same register map but it provides better back-to-back access performance than the APB bus. These apertures are mutually exclusive; the aperture enabled for a given GPIO port is controlled by the appropriate bit in the GPIOHBCTL register. To use these pins in a particular GPIO port, the clock for the port must be enabled by setting the appropriate GPIO Port bit field (GPIOn) in the RCGC2 register and the internal POR signal is asserted until or configured. All GPIO pins are configured to be un-driven (Tristate): GPIOAFSEL=0, GPIODEN=0, GPIOPDR=0, and GPIOPUR=0, except for the pins in all possible configurations. The GPIO pads and the control register settings required to achieve them.

3.2.2 Ethernet Port

In the OSI reference system, ethernet is at the Data Link layer. Systems are communicating over ethernet divide a stream of data into individual packets called frames. Each frame contains source and destination addresses and error-checking data so that damaged data can be detected and re-transmitted. Figure 3.3 also presents the ethernet internal signals of the ARM processor.

LM3S9B96 microcontroller has an inbuilt MAC and PHY feature so that it can be connected directly to appropriate pins of the RJ45 jack for ethernet.
communication [7]. Isolation transformers, LEDs and termination resistors are integrated with RJ45 connector.

### 3.2.2.1 Ethernet Controller Signals

**LED Indicators:** Two LED signals are available in ethernet controller are used to indicate various states of operation. These pins are configured default GPIO signals PF3 and PF2. These signals are mapped with the LED0 and LED1 pins. For the ethernet controller, to drive these signals, they must be reconfigured to their hardware function. The functions of these pins are programmable using the ethernet MAC LED Encoding (MACLED) register.

**Physical Layer Operation:** Ethernet controller includes Physical Layer (PHY), integrated with ENDECs, scrambler/descrambler, dual-speed clock recovery, and full-featured auto-negotiation functions. The transmitter includes an on-chip pulse shaper and a low-power line driver. It has an adaptive equalizer and a baseline restoration circuit, required for accurate clock and data recovery. The transceiver interfaces to category-5 unshielded twisted pair (Cat-5 UTP) cabling for 100BASE-TX applications. The ethernet controller is connected to the line media via dual 1:1 isolation transformers. External filters are not required.

**Selection of Clock:** Ethernet controller can be clocked from an on-chip crystal oscillator which can also be driven by an external oscillator. The on-chip crystal oscillator is of 25MHz frequency and it should be connected between the XTALPPHY and XTALNPHY pins. Ethernet oscillator is powered down when the EPHY0 bit in Run Mode Clock Gating Control Register 2 (RCGC2) register is cleared. After setting the EPHY0 bit, software must wait 3.5 ms before accessing any
of the MII Management registers. A 12.4kΩ 1% tolerance resistor should be connected between the ERBIAS and ground in close proximity to the ERBIAS pin.

The "Pin MUX/Pin Assignment" is the GPIO pin placement for the LED signals. The AFSEL bit in the GPIO Alternate Function Select (GPIOAFSEL) register should be set to choose the LED function. The number in parentheses PF3 (1) and PF2 (1) act as encoding that must be programmed into the PMCn field in the GPIO Port Control (GPIOPCTL) register to assign the LED0 and LED1 signals to the specified GPIO port pins as shown in Figure 3.5. The remaining signals (with the word "fixed" in the Pin MUX/Pin Assignment column) have a fixed pin assignment and function.

Figure 3.4: Ethernet internal signals of the ARM processor
Figure 3.5: Schematic diagram of Ethernet connector (RJ-45)

The microcontroller board connector CN4 is provided for LAN cable attachment from the switch for remotely monitoring and controlling Tx modules. Figure 3.5 provides pin connection of the RJ-45 connector from the microcontroller. This connector is used to connect ethernet based systems for communication.
Table 3.5 shows the lists of external signals of Ethernet controller and describes the function of each signal.

**Table 3.1: Ethernet Controller Signals**

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin-MUX/Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Connection to</th>
</tr>
</thead>
<tbody>
<tr>
<td>LED 0</td>
<td>59</td>
<td>PF3 (1)</td>
<td>O</td>
<td>TTL</td>
<td>Ethernet LED 0</td>
</tr>
<tr>
<td>LED 1</td>
<td>60</td>
<td>PF2 (1)</td>
<td>O</td>
<td>TTL</td>
<td>Ethernet LED 1</td>
</tr>
<tr>
<td>MDIO</td>
<td>58</td>
<td>FIXED</td>
<td>I/O</td>
<td>OD</td>
<td>MDIO of Ethernet PHY</td>
</tr>
<tr>
<td>TXOP</td>
<td>43</td>
<td>FIXED</td>
<td>O</td>
<td>TTL</td>
<td>TXOP of Ethernet PHY</td>
</tr>
<tr>
<td>TXON</td>
<td>46</td>
<td>FIXED</td>
<td>O</td>
<td>TTL</td>
<td>TXON of Ethernet PHY</td>
</tr>
<tr>
<td>RXIP</td>
<td>40</td>
<td>FIXED</td>
<td>I</td>
<td>Analog</td>
<td>RXIP of Ethernet PHY</td>
</tr>
<tr>
<td>RXIN</td>
<td>37</td>
<td>FIXED</td>
<td>I</td>
<td>Analog</td>
<td>RXIN of Ethernet PHY</td>
</tr>
<tr>
<td>XTALNPHY</td>
<td>17</td>
<td>FIXED</td>
<td>O</td>
<td>Analog</td>
<td>Ethernet PHY XTALN 25-MHz oscillator crystal output.</td>
</tr>
<tr>
<td>XTALPPHY</td>
<td>16</td>
<td>FIXED</td>
<td>O</td>
<td>Analog</td>
<td>Ethernet PHY XTALP 25-MHz oscillator crystal output.</td>
</tr>
<tr>
<td>ERBIAS</td>
<td>33</td>
<td>FIXED</td>
<td>O</td>
<td>Analog</td>
<td>12.4-kΩ resistor (1% precision) used internally for Ethernet PHY.</td>
</tr>
</tbody>
</table>
The functional description of the ethernet controller is divided into the following sections:

### 3.2.2.2 MAC Operation

The operation of the MAC layer includes an overview of the ethernet frame format, MAC layer FIFOs, ethernet transmission and reception options, packet timestamps, and LED indicators.

**Frame format:** The frames are transmitted from left to right in the seven fields. The bits within the frame are transmitted from least to most significant bit.

#### Table 3.2: Ethernet frame

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preamble (7 Byte)</td>
<td>The Preamble field is used to synchronize with the received frame’s timing. The preamble is 7 octets long.</td>
</tr>
<tr>
<td>SFD (1 Byte)</td>
<td>Start Frame Delimiter (SFD): The SFD field follows the preamble pattern and indicates the start of the frame. Its value is 10101011.</td>
</tr>
<tr>
<td>Destination Address (6 Byte)</td>
<td>Destination Address (DA): This field specifies destination addresses for which the frame is intended. The LSB (bit 16 of DA octets 1 in the frame), of the DA determines whether the address is an individual (0), or group/multicast (1) address.</td>
</tr>
<tr>
<td>Source Address (6 Byte)</td>
<td>Source Address (SA): The source address field identifies the station from which the frame was initiated.</td>
</tr>
<tr>
<td>Length / Type (2 Byte)</td>
<td>Length / Type Field: Meaning of this field depends on its numeric value and it can be interpreted as the length or type code. The maximum length of the field data is 1500 octets. If the value of the Length/Type field is less than or equal to 1500</td>
</tr>
<tr>
<td>Data 46-1500 Bytes</td>
<td>FCS</td>
</tr>
</tbody>
</table>
decimal, it indicates the number of MAC client data octets. And if the value of this field is greater than or equal to 1536 decimal, then it encodes the type interpretation. The meaning of the Length/Type field when the value is between 1500 and 1536 decimal, it is unspecified by the IEEE 802.3 standard. However, the ethernet controller assumes type interpretation if the value of the Length/Type field is greater than 1500 decimal. The definition of the Type field is specified in the IEEE 802.3 standard. The first of the two octets in this field is most significant.

- **Data:** Data field is a sequence of octets that is at least 46 bytes in length and up to 1500 bytes in length. The full data transparency is provided, so any value can appear in this field. A minimum frame size of 46 octets is required to meet the IEEE standard. If the frame size is too small, the Ethernet controller automatically appends extra bits (a pad), thus, the pad can have a size of 0 to 46 octets. The data padding can be disabled by clearing the PADEN bit in the ethernet MAC Transmit Control (MACTCTL) register. For the ethernet controller, the data sent/received can be larger than 1500 bytes without causing a Frame Too Long error. Instead, a FIFO overrun error is reported using the FOV bit in the ethernet MAC Raw Interrupt Status (MACRIS) register when the frame received is too large to fit into the ethernet controller’s 2KB RAM.

- **Frame Check Sequence (FCS):** The frame check sequence carries the cyclic redundancy check (CRC) value. It has been computed over the destination address, source address, length/type, and data (including pad) fields using the CRC-32 algorithm. The ethernet controller computes the FCS value one nibble at a time. For transmitted frames, this field is automatically inserted by the MAC layer unless disabled by clearing the CRC bit in the MACTCTL register. And for receiving frames, this field is automatically checked. If the FCS does not pass, the frame is not
placed in the RX FIFO, unless the FCS check is disabled by clearing the BADCRC bit in the MACRCTL register.

**MAC Layer FIFOs:** Ethernet controller is capable of simultaneous transmission and reception. This feature is enabled by setting the DUPLEX bit in the MACTCTL register. Ethernet frame transmission, a 2-KB transmit FIFO is provided that can be used to store a single frame. The specification limits of IEEE 802.3 for the size of an ethernet frame's payload section is 1500 Bytes. The ethernet controller places no such limit. The full buffer can be used for a payload of up to 2032 bytes (as the first 16 bytes in the FIFO are reserved for the destination address, source address and length/type information). For ethernet frame reception, a 2-KB receive FIFO is provided that can be used to store multiple frames, up to a maximum of 31 frames. If a frame is received, and there is an insufficient space in the RX FIFO, an overflow error is indicated using the FOV bit in the MACRIS register.

The TX and RX FIFO layout for the TX FIFO, the Data Length field in the first FIFO word refers to the ethernet frame data payload as shown in the 5th to Nth FIFO positions. The RX FIFO frame length field is the total length of the received ethernet frame including the Length/Type bytes and the FCS bits. If FCS generation is disabled by clearing the CRC bit in the MACTCTL register, the last word in the TX FIFO must contain the FCS bytes for the frame that has been written to the FIFO. Also note that if the length of the data payload section is not a multiple of 4, the FCS field is not aligned on a word boundary in the FIFO. However, for the RX FIFO, the beginning of the next frame is always on a word boundary.

**Transmission options:** In the MAC layer, the transmitter can be configured for both full-duplex and half-duplex operation by using DUPLEX bit in the MACTCTL
register. Note that in 10BASE-T half-duplex mode, the transmitted data are loop
backed on the receive path. The ethernet controller automatically generates and inserts
the Frame Check Sequence (FCS) at the end of the transmit frame when the CRC bit
in the MACTCTL register is set. However, for test purposes, this feature can be
disabled in order to generate a frame with an invalid CRC by clearing the CRC bit.
The IEEE 802.3 specification requires that the ethernet frame payload section be a
minimum of 46 bytes. The ethernet controller automatically pads the data section if
the payload data section loaded into the FIFO is less than the minimum 46 bytes when
the PADEN bit in the MACTCTL register is set. This feature can be disabled by
clearing the PADEN bit. The transmitter must be enabled by setting the TXEN bit in
the MACTCTL register.

Reception Options: The ethernet controller RX FIFO should be cleared during
software initialization. The receiver should first be disabled by clearing the RXEN bit
in the ethernet MAC receive control (MACRCTL) register, then the FIFO can be
cleared by setting the RSTFIFO bit in the MACRCTL register. The receiver
automatically rejects frames that contain the bad CRC values in FCS field. In this
case, a Receive Error interrupt is generated and the receive data is lost. To accept all
frames, clear the BADCRC bit in the MACRCTL register.

In normal operating mode, the receiver accepts only those frames that have a
destination address that matches the address programmed in the ethernet MAC
Individual Address 0 (MACIA0) and ethernet MAC Individual Address 1 (MACIA1)
registers. However, the ethernet receiver can also be configured for promiscuous and
multicast modes by setting the PRMS and AMUL bits in the MACRCTL register.
**Packet Timestamps:** Applications require a very precise clock for time stamping samples or triggering events. The IEEE Precision Time Protocol (PTP) or IEEE-1588 provides a mechanism for synchronizing clocks across an ethernet to sub-microsecond precision. The accuracy of the PTP clock depends greatly upon the accuracy of timestamps of the PTP ethernet packets. The software only has a PTP solution and there is a small irregular movement in the ethernet packet timestamps, resulting in a less precise PTP clock on the target. In some of these devices, General Purpose Timer 3 (GPT3) can be used in conjunction with the ethernet MAC Timer Support (MACTS) register, to provide more accurate timestamp for ethernet packets. This feature is enabled by setting the TSEN bit in the MACTS register.

When this feature is enabled, the general purpose timer 3 must be dedicated to the ethernet controller. This must be configured as 16-bit edge capture mode, Timer-A of GPT3 stores the transmit time, and Timer B stores the receive time. Another General Purpose Timer can be set up as 16-bit free-running timer to synchronize the receiver and transmitter timers and provide a timestamp with which to compare the timestamps stored in GPT3.

**Auto-negotiation:** Ethernet controller supports the auto-negotiation functions of clause 28 of the IEEE 802.3 standard for 10/100 Mbps operation over copper wiring and it can be controlled via registry settings. This function is turned ON by default, and the ANEGEN bit in the ethernet PHY Management Register 0 - Control (MR0) is set after reset. The software can disable the auto-negotiation function by clearing the ANEGEN bit. The contents of the ethernet PHY Management Register - Auto-Negotiation Advertisement (MR4) are reflected to the ethernet controller link partner during auto-negotiation via fast-link pulse coding. Once auto-negotiation is completed, the SPEED bit in the ethernet PHY management register 31 – PHY
Special Control/Status (MR31) register reflects the actual speed. The AUTODONE bit in MR31 is set to indicate that auto-negotiation is complete. Setting the RANEG bit in the MR0 register also causes auto-negotiation to restart.

**Ethernet Polarity Correction:** Ethernet controller is capable of automatic polarity reversal for 10BASE-T and auto-negotiation functions. The XPOL bit in the ethernet PHY Management Register 27 is a special control/status (MR27) register and is set to indicate that the polarity has automatically been reversed.

**Configuration of MDI/MDI-X:** The MDI/MDI-X configuration is defined in IEEE 802.3-2002 specification through software assistance. The MDI/MDI-X configuration eliminates the need for crossover cables when connecting to another device, such as, a hub. Software can implement the MDI/MDI-X configuration using a function outlined by the pseudo code. This code should be called periodically using one of the available timer resources on the Stellaris microcontroller such as the System Tick Timer or one of the General Purpose timers.

**Power Saving Modes:** The PHY has two power-saving modes one is Power-Down and Energy Detect Power-Down mode. The power-down mode is activated by setting the PWRDN bit in the MR0 register. When the PHY is in power-down mode, it consumes minimum power. When the PWRDN bit is cleared, the PHY power up and it automatically resets. When setting the EDPD bit in the MR17 register or the energy power-down mode, it is activated. In this mode of operation when no energy is present on the line, the PHY is powered down except for the management interface, the SQUELCH circuit and the ENERGYON logic. The logic ENERGYON is used to detect the presence of valid energy from transmission speeds 100BASE-T, 10BASE-T, or auto-negotiation signals. While the PHY is powered down, nothing is
transmitted. When linking pulses or packets are received, the PHY is powered-up. The PHY automatically resets itself into the state it had prior to power down and the EONIS bit is set in the MR29 register. The first and possibly the second packet to activate the mode ENERGYON may be lost.

3.2.2.3 Interrupt Generation

The following are the interrupts for one or more conditions generated by ethernet controller:

a. A frame has been received into an empty RX FIFO
b. A frame transmission error has occurred
c. A frame has been transmitted successfully
d. A frame has been received with inadequate room in the RX FIFO (overrun)
e. A frame has been received with one or more error conditions (for example, FCS failed)
f. An MII management transaction between the MAC and PHY layers has completed.

One or more of the following PHY layer conditions occur:

i. Auto-Negotiate Complete
ii. Remote Fault
iii. Link Partner Acknowledge
iv. Parallel Detect Fault
v. Page Received
3.2.2.4 DMA Operation

The peripheral provides request signals to the μDMA controller and has a dedicated channel for transmitting and one for receiving. The request is a single type of both channels. The burst requests are not supported. The RX channel request is asserted when a packet is received while the TX channel request is asserted when the transmit FIFO becomes empty. No need for special configuration to enable the ethernet peripheral to use with the μDMA controller. Because of this, received packet size is not known until the header is examined. It is best to set up the initial μDMA transfer to copy the first 4 words including the packet length plus the ethernet header from the RX FIFO when the RX request occurs.

The μDMA causes an interrupt when this transfer is complete. Upon entering the interrupt handler, the packet length in the FIFO and the ethernet header are in a buffer and can be examined. Once the packet length is known, another μDMA transfer can be set up to transfer the remaining received packet payload from the FIFO into a buffer. This transfer should be initiated by software and another interrupt occurs when this transfer is done. Even though the TX channel generates a TX empty request, the recommended way to handle μDMA transfers for transmitting packets is to set up the transfer from the buffer. It contains the packet to the transmit FIFO, and then to initiate the transfer with a software request. An interrupt occurs when this transfer is complete. In both channels, the "auto-request" transfer mode should be used.

3.2.2.5 Ethernet Software Configuration

To use the ethernet controller, it must be enabled by setting the EPHY0 and EMAC0 bits in the RCGC2 register. In addition, the clock to the appropriate GPIO module must be enabled via RCGC2 register in the system control module. To find
out which GPIO port is to be enabled, the configuration of the PMCn fields in the GPIOPCTL register is done to assign the ethernet signals to the appropriate pins.

The following steps are used to configure the ethernet controller for basic operation:

a. Program the MACDIV register to obtain 2.5 MHz clock (or less) on the internal MII. Assuming a 20-MHz system clock, the MACDIV value should be 0x03 or greater.

b. Program the MACIA0 and MACIA1 register for address filtering.

c. Program the MACTCTL register for Auto CRC generations, padding, and full-duplex operation using a value of 0x16.

d. Program the MACRCTL register to flush the receive FIFO and reject frames with a bad FCS using the value of 0x18.

e. To enable the both Transmit and Receive by setting the LSB in both the MACTCTL and MACRCTL register.

f. To transmit a frame, write the frame into the TX FIFO using the ethernet MAC Data register (MACDATA). Then set the NEWTX bit in the register ethernet Mac Transmission Request (MACTR) to initiate the transmit process. When the NEWTX bit has been cleared, the TX FIFO is available for the next transmit frame.

g. To receive a frame, wait for the NPR field in the ethernet MAC Number of Packets register (MACNP) to be non-zero. Then begin reading the frame from the RX FIFO by using the MACDATA register. To ensure that the entire packet is received, either use the Driver Lib Ethernet Packet Get() API or compare the number of bytes received in the “Length” field of the frame to determine when the packet has been completely read.
3.2.3 Analog to Digital Converter

An analog-to-digital converter (ADC) is an electronic device that converts an input analog voltage to a digital number proportional to the magnitude of the voltage. LM3S9B96 microcontroller has two 10-bit ADCs with 16 input capabilities. The ADC module contains four programmable sequencers and allows the sampling of multiple analog input sources without the intervention of the microcontroller. Each sample sequencer provides a flexible programming with fully configurable input source, trigger events, interrupt generation, and sequencer priority.

3.2.3.1 ADC Functionality

A digital comparator function allows the conversion value to be diverted to one of the two ADC modules that is provided with eight digital comparators; each one evaluates the ADC conversion value against its two user-defined values to determine the operational range of the signal. The trigger source for ADC0 and ADC1 may be independent or may operate from the same trigger source and operate on the alike or different inputs. A phase shifter can delay the start of sampling by a specified phase angle. If the converters are running at the same sample rate, they may be configured to start the conversions coincidentally or with one of 15 different discrete phase’s relative to each other. Using the ADC Sample Phase Control (ADCSPCS) register, the sample time can be delayed from the standard time in 22.5° increments up to 337.5°. Figure 3.6 shows how the two modules ADC0 and ADC1 are connected to analog inputs and the system bus.
The ADC signals are analog functions for some of GPIO signals. The “Pin MUX/Pin Assignment” column in the Table 3.3 lists the GPIO pin place for the ADC signals. The AINx and VREFA analog signals are not 5V tolerant, and goes through an isolation circuit before reaching their circuitry. These signals are configured by clearing the corresponding DEN bit in the GPIO Digital Enable (GPIODEN) register and setting the AMSEL bit in the GPIO Analog Mode Select (GPIOAMSEL) register. Table 3.3 also lists out the external signals of the ADC module and describes the functionality of each signal.
Figure 3.7 provides the resistor divider that uses two 10k ohm resistors. The total of 16 input channels circuitry is available for connecting the sensors in transmitter. The ADCs collect the sample data by using a programmable sequence based approach instead of traditional single or double sampling approach found in many ADC modules. Each sample sequence is fully programmed series of consecutive samples. It allows the ADC to collect data from multiple input sources without having to be re-configured or serviced by the microcontroller. The μDMA can be used more efficiently to move data from sample sequencers without CPU intervention.
Table 3.3: ADC Input Signals

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Pin MUX/Pin Assignment</th>
<th>Type of Pin</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AIN 0</td>
<td>1</td>
<td>PE 7</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 0</td>
</tr>
<tr>
<td>AIN 1</td>
<td>2</td>
<td>PE 6</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 1</td>
</tr>
<tr>
<td>AIN 2</td>
<td>5</td>
<td>PE 5</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 2</td>
</tr>
<tr>
<td>AIN 3</td>
<td>6</td>
<td>PE 4</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 3</td>
</tr>
<tr>
<td>AIN 4</td>
<td>100</td>
<td>PD 7</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 4</td>
</tr>
<tr>
<td>AIN 5</td>
<td>99</td>
<td>PD 6</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 5</td>
</tr>
<tr>
<td>AIN 6</td>
<td>98</td>
<td>PD 5</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 6</td>
</tr>
<tr>
<td>AIN 7</td>
<td>97</td>
<td>PD 4</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 7</td>
</tr>
<tr>
<td>AIN 8</td>
<td>96</td>
<td>PE 3</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 8</td>
</tr>
<tr>
<td>AIN 9</td>
<td>95</td>
<td>PE 2</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 9</td>
</tr>
<tr>
<td>AIN 10</td>
<td>92</td>
<td>PB 4</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 10</td>
</tr>
<tr>
<td>AIN 11</td>
<td>91</td>
<td>PB 5</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 11</td>
</tr>
<tr>
<td>AIN 12</td>
<td>13</td>
<td>PD 3</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 12</td>
</tr>
<tr>
<td>AIN 13</td>
<td>12</td>
<td>PD 2</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 13</td>
</tr>
<tr>
<td>AIN 14</td>
<td>11</td>
<td>PD 1</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 14</td>
</tr>
<tr>
<td>AIN 15</td>
<td>10</td>
<td>PD 0</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 15</td>
</tr>
<tr>
<td>VREFA</td>
<td>90</td>
<td>PB 6</td>
<td>I</td>
<td>Analog</td>
<td>This input provides a reference voltage used to specify the input voltage at which the ADC converts to a maximum value. In other words, the voltage that is applied to VREFA is the voltage with which an AINn signal is converted to 1023. The VREFA external voltage reference for the ADC is minimum 2.97 volts to 3.03 volts.</td>
</tr>
</tbody>
</table>
3.2.3.2 Sample Sequencers

All sequencers are identical in implementation except for the number of samples that can be captured and the depth of the FIFO. Each of the samples is captured and stored in the FIFO. In this implementation, each FIFO entry is a 32-bit word, with the lower 10 bits containing the conversion result. Table 3.4 shows the sampling and depth of sequencers of the FIFO. The control and data capture is handled by the sample sequencers.

Table 3.4: Samples and FIFO depth of Sequencers

<table>
<thead>
<tr>
<th>Sequencer</th>
<th>Number of samples</th>
<th>Depth of FIFO</th>
</tr>
</thead>
<tbody>
<tr>
<td>SS3</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SS2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>SS1</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>SS0</td>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

Then each sample is defined by bit fields in ADCSSMUXn (ADC Sample Sequence Input Multiplexer Select) and ADCSSCTLn (ADC Sample Sequence Control) registers, where "n" corresponds with the sequence number. The ADCSSMUXn fields select the input pin, while the ADCSSCTLn fields contain the sample control bits corresponding to the parameters such as temperature sensor selection, interrupt enable, end of the sequence, and differential input mode. Sample sequencers are enabled by setting the respective ASENn bit in the ADC Active Sample Sequencer (ADCACTSS) register. And it should be configured before being enabled. Sampling is then initiated by setting the SSn bit in the ADC Processor Sample Sequence Initiate (ADCPSSI) register. The sample sequences may be initiated on multiple ADC modules simultaneously using the GSYNC and SYNCWAIT bits in the ADCPSSI register during the configuration of each ADC module. The ADC
Processor Sample Sequence Initiator (ADCPSSI) has an offset of 0x028. This register provides a mechanism for application software to initiate sampling in the sample sequencers. It can be initiated individually or in any combination. When the multiple sequences are triggered simultaneously, the priority encoding in ADCSSPRI dictates the execution order. In the ADCSSCTLn register, the IEn bits can be set in any combination of samples, allowing interrupts to be generated after every sample in the sequence. Further, the END bit can be set at any point within a sample sequence.

3.2.3.3 Conversion Method

The ADC module uses Successive Approximation Register (SAR) architecture to deliver a 10-bit, low-power, high-precision conversion value. SAR algorithm uses a current mode D/A converter to achieve lower settling time, resulting in higher conversion speeds for the A/D converter. In addition, built-in sample-and-hold circuitry with offset-calibration circuitry improves conversion accuracy. The ADC must run from the PLL or a 14 MHz to 18 MHz clock source. ADC operates from both the 3.3V analog and 1.2V digital power supplies. The clock can be configured to reduce the power consumption when ADC conversions are not required. The analog inputs are connected to the ADC through pads and specially balanced input paths to minimize the distortion of the inputs. The main advantage of SAR ADC is a good ratio of speed to power, a compact design compared to flash ADC. The physical limitation of SAR ADC is that it has only one comparator throughout the entire conversation process. If there is any offset error in the comparator, it reflects on all conversion bits. The gain error in DAC and static parameter errors do not affect the dynamic behavior of SAR ADC. Furthermore, at the higher speeds it is difficult to obtain the dynamic behavior of ADC. One solution is to use time-interleaved converters [12].
3.2.3.4 Internal Voltage Reference

The band-gap circuitry generates an internal 3.0V reference that can be used by the ADC to produce a conversion value from the selected analog input and its range value is from 0x000 to 0x3FF. This configuration results in a resolution of approximately 2.9 mV per ADC code. Analog input pads can handle voltages beyond this range. The ADC conversions are saturated in under-voltage and in the over-voltage case.

3.2.3.5 External Voltage Reference

The ADC can use an external voltage reference to produce the conversion value from the selected analog input by setting the VREF bit in the ADC Control (ADCCTL) register. The VREF bit specifies whether to use the internal or external reference. While the range of the conversion value remains the same (0x000 to 0x3FF). The analog voltage is associated with the value 0x3FF that corresponds to the value of the voltage.

The ground is always being used as the reference level for the minimum conversion value. The analog input voltages above the external voltage reference are saturated to 0x3FF value. The VREFA specification defines the useful range for the external voltage reference. The external voltage reference can be more accurate than the internal reference by using a high-precision source or trimming the source.

3.2.3.6 Output Functionalities

ADC conversions can either be stored in the ADC Sample Sequence FIFOs or compared using the digital comparator resources as defined by the SnDCOP bits in ADC Sample Sequence Operation (ADCSSOPn) register. Those selected ADC conversions are used by their respective digital comparator to watch the external
signal. Each comparator has two possible output functions that are processor interrupts and triggers. Each output function has its own state machine to track the monitored signal. The interrupt and trigger functions are enabled individually or both at the same time and the same conversion data is used by each function.

**Interrupts:** The digital comparator interrupts function is enabled by setting the CIE bit in the ADC Digital Comparator Control (ADCDCTLn) register. This bit enables the interrupt function state machine to start monitoring incoming ADC conversions. When the appropriate set of conditions is met, and the DCONSSx bit is set in the ADCIM register, an interrupt is sent to the interrupt controller.

**Triggers:** By setting the CTE bit in the ADCDCCTLn register, the digital comparator trigger function is enabled. The CTE bit enables the trigger function state machine to start monitoring the incoming ADC conversions. When the appropriate set of conditions is met, the corresponding digital comparator trigger to the PWM module is asserted.

### 3.2.3.7 Modes of Operation

The four operational modes are provided to support a broad range of applications and multiple possible signaling requirements; Always, Once, Hysteresis Always, and Hysteresis Once. The operational mode is selected using the CIM or CTM field in the ADCDCCTLn register.

**Always Mode:** The associated interrupt or trigger is asserted whenever the ADC conversion value meets its comparison criteria. The result is a string of assertions on the interrupt or trigger while the conversions are within the appropriate range.
**Once Mode:** The associated interrupt or trigger is asserted whenever the ADC conversion value meets its comparison criteria, and the previous ADC conversion value did not meet the comparison criteria. The result is a single assertion of the interrupt or trigger when the conversions are within the appropriate range.

**Hysteresis-Always Mode:** This mode is to be used in conjunction with the low-band or high-band regions because the mid-band region must be crossed and the opposite region entered to clear the hysteresis condition. The associated interrupt or trigger is asserted in the following cases 1) the ADC conversion value meets its comparison criteria or 2) a previous ADC conversion value has met the comparison criteria and the hysteresis condition has not been cleared by entering the opposite region. The result is a string of assertions on the interrupt or trigger that continue until the opposite region is entered.

**Hysteresis-Once Mode:** The associated interrupt or trigger is asserted only when the ADC conversion value meets its comparison criteria. The hysteresis condition is clear and the previous ADC conversion did not meet the comparison criteria. The result is a single assertion on the trigger or the interrupt.

### 3.2.3.8 Initialization and Configuration

Using ADC the PLL must be enabled and programmed to a supported crystal frequency in the Run-Mode Clock Configuration (RCC) where the offset is 0x060. Bits using in this register to configure the system clock and oscillators, using unsupported frequencies can cause faulty operation in the ADC module.

**ADC Module Initialization:** The initialization of the ADC module is a simple process with very few steps: enabling the clock to the ADC, disabling the analog
isolation circuit associated with all inputs that are to be used, and reconfiguring the sample sequencer priorities.

The following steps are the initialization sequence of the ADC module:

1. By using RCGC0 register enable the ADC clock.
2. Enable the clock to the appropriate GPIO modules via the RCGC2 register and to find out which GPIO ports used to enable signal.
3. Set the GPIO AFSEL bits of the ADC input pins to determine which GPIOs to configure.
4. Configure the AINx and VREFA signals to be analog inputs by clearing the corresponding DEN bit in the GPIO Digital Enable (GPIODEN) register.
5. Disable the analog isolation circuit for all ADC input pins that are to be used by writing 1 to the appropriate bits of the GPIOAMSEL register in the associated GPIO block.
6. If required by the application, reconfigure the sample sequencer priorities in the ADCSSPRI register. The default configuration has Sample Sequencer 0 with the highest priority and Sample Sequencer 3 as the lowest priority.

**Configuration of Sample Sequencer:** Configuration of the sample sequencers is slightly more complex than the module initialization because each sample sequencer is completely programmable.

The configuration for each sample sequencer should be as follows:

1. Ensure that the sample sequencer is disabled by clearing the corresponding ASEn bit in the ADCACTSS register. Programming of the sample sequencers is allowed without having them enabled. Disabling the sequencer
during programming prevents erroneous execution if a trigger event were to occur during the configuration process.

2. In the ADCEMUX register configure trigger event for the sample sequencer.

3. For each sample in the sample sequence, configure the corresponding input source in the ADCSSMUXn register.

4. For each sample in the sample sequence, configure the sample control bits in the corresponding nibble in the ADCSSCTLn register. When programming the last nibble, ensure that the END bit is set. Failure to set the END bit causes unpredictable behavior.

5. If interrupts are to be used, set the corresponding MASK bit in the ADCIM register.

6. Enable the sample sequencer logic by setting the corresponding ASENn bit in the ADCACTSS register.

### 3.2.4 UARTs

LM3S9B96 microcontroller has three Universal Asynchronous Receiver/Transmitters. UART has a separate 16x8 transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading. The programmable FIFO length is 1-byte deep operation providing a conventional double-buffered interface. The FIFO trigger levels are 1/8, 1/4, 1/2, 3/4, and 7/8. It has standard asynchronous communication bits for start, stop, parity, line-break generation and detection. Its fully programmable serial interface characteristics are 5, 6, 7, or 8 data bits; even, odd, stick, or no-parity bit generation/detection; 1 or 2 stop bit generation. Programmable baud-rate generator allows speeds up to 5 Mbps for regular speed (divide by 16) and 10 Mbps for high speed (divide by 8).
The UART signals are alternate functions for some GPIO signals and by default at reset state, with the exception of the U0Rx and U0Tx pins that are default to the UART function. The AFSEL bit in the GPIO Alternate Function Select (GPIOAFSEL) register should be set to choose the UART function. The number in parentheses is the encoding that must be programmed into the PMCn field in the GPIO Port Control (GPIOPCTL) register to assign the UART signal to the specified GPIO port pin.

UART performs the functions of parallel-to-serial and serial-to-parallel conversions. The UART is configured for transmission and/or reception via the TXE and RXE bits of the UART Control (UARTCTL) register. Transmit and receive are both enabled out of reset before any control registers are to be programmed, the UART must be disabled by clearing the UARTEN bit in the UARTCL register. 

Figure 3.8 shows the TXD and RXD pin connections.
If UART is disabled during a TX or RX operation, the current transaction is completed prior to the UART stopping. The UART module has serial IR (SIR) encoder/decoder block that can be connected to an infrared transceiver to implement an IrDA SIR physical layer. The SIR function programmed using the UARTCTL register. Pins U1TX, U1RX are transmission and reception inputs of the Max-232 driver. The RS23_2_TXD and RS232_2_RXD pins are the transmission and reception outputs of the Max232 the communication between the embedded target board and the host computer as shown in Figure 3.9.

3.2.4.1 Transmission and Reception Logic

The transmit logic performs parallel-to-serial conversion on the data read from the transmit FIFO. In Figure 3.10, control logic outputs the serial bit stream beginning with a start bit. Transmit logic is followed by the data bits (LSB first),
parity bit, and the stop bits according to the programmed configuration in the control registers.

![Figure 3.10: Frame of UART character](image)

The receive logic performs serial-to-parallel conversion on the received bit stream after a valid start pulse has been detected. It performs the overrun, parity, frame error checking, and line-break detection. Their status accompanies the data that is written to receive FIFO.

### 3.2.4.2 Baud-rate Generation

The baud-rate divisor is a 22-bit number consisting of a 16-bit integer and a 6-bit fractional part, the number formed by using those two values the baud-rate generator determine the bit period. The fractional baud-rate divider allows the UART to generate all standard baud rates. The 16-bit integer is loaded through the UART Integer Baud-Rate Divisor (UARTIBRD) register and the 6-bit fractional part is loaded with the UART Fractional Baud-Rate Divisor (UARTFBRD) register. The Baud-Rate Divisor (BRD) has following relationship to the system clock. Where the BRDI is integral part of the BRD and BRDF is the fractional part is separated by a decimal place.

\[
BRD = BRDI + BRDF = UARTSysClk / (ClkDiv \times Baud Rate) \ldots (1)
\]

Where UARTSysClk is the system clock connected to the UART, and ClkDiv is either Baud-16 or Baud-8. The 6-bit fractional number, that is to be loaded into the
DIVFRAC bit field in the UARTFBRD register. It can be calculated by taking the fractional part of the baud-rate divisor, multiplying it by 64, and adding 0.5 to account for rounding errors.

\[
\text{UARTFBRD [DIVFRAC]} = \text{integer} (\text{BRDF} \times 64 + 0.5) \ldots \ldots \ldots \ldots (2)
\]

The UART generates an internal baud-rate reference clock at 8x or 16x the baud-rate in UARTCTL. This reference clock is divided by 8 or 16 to generate the transmit clock, and is used for error detection during receive operations. Along with the UART Line Control, High Byte (UARTLCRH) register, the UARTIBRD and UARTFBRD registers from an internal 30-bit register. This 30-bit register is only updated when a write operation to UARTLCRH is performed, so any changes to the baud-rate divisor must be followed by a write to the UARTLCRH register for the changes to take effect. To update the baud-rate registers, there are four possible sequences:

i. UARTIBRD write, UARTFBRD write, and UARTLCRH write

ii. UARTFBRD write, UARTIBRD write, and UARTLCRH write

iii. UARTIBRD write and UARTLCRH write

iv. UARTFBRD write and UARTLCRH write

3.2.4.3 Data Transmission

The data received or transmitted is stored in two 16-byte FIFOs, though receive FIFO has an extra four bits per character for status information. In transmission, the data is written into the transmit FIFO. If the UART is enabled, it causes a data frame to start transmitting with the parameters indicated in the UARTLCRH register. The data continue to be transmitted until there is no data left in the transmit FIFO. The BUSY bit in the UART Flag (UARTFR) register is asserted as
soon as data is written to the transmit FIFO (that is, if the FIFO is non-empty) and remains asserted while data is being transmitted. The BUSY bit is negated only when the transmit FIFO is empty and the last character has been transmitted from the shift register including the stop bits. The UART can indicate that it is busy even though the UART may no longer be enabled.

When the receiver is idle (UnRx signal is continuously 1) and the data input goes low (start bit has been received), the receive counter begins running and data is sampled on the eighth cycle of Baud-16 or fourth cycle of Baud-8 depending on the setting of the HSE bit (bit 5) in UARTCTL register. The start bit is valid and recognized, if the UnRx signal is still low in the eighth cycle of Baud-16 (HSE clear) or the fourth cycle of Baud-8 (HSE set), otherwise it is ignored. After a valid start bit is detected, the successive data bits are sampled on every 16th cycle of Baud-16 or 8th cycle of Baud-8 (that is, one bit period later).

According to the programmed length of the data characters and the value of the HSE bit in UARTCTL register, the parity bit is then checked if parity mode is enabled, the data length and parity are defined in the UARTLCRH register. A valid stop bit is confirmed if the UnRx signal is high, otherwise a framing error has occurred. When a full word is received, the data is stored in the receive FIFO along with any error bits associated with that word.

**Modem Handshake:** It configures and uses the modem flow control and status signals for UART1, when connected as a DTE (data terminal equipment) or as a DCE (data communications equipment). Generally, a modem is a DCE and a computing device that connects to a modem is the DTE.
**Signaling:** UART1 status signals are based on whether the UART is used as a DTE or DCE. The following Table 3.5 shows modem flow control and status signals.

**Table 3.5:** DTE and DCE status and flow control

<table>
<thead>
<tr>
<th>When used as a DTE</th>
<th>When used as a DCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1CTS’ is Clear To Send</td>
<td>U1CTS’ is Request To Send</td>
</tr>
<tr>
<td>U1DSR’ is Data Set Ready</td>
<td>U1DSR’ is Data Terminal Ready</td>
</tr>
<tr>
<td>U1DCD’ is Data Carrier Detect</td>
<td>U1RTS’ is Clear To Send</td>
</tr>
<tr>
<td>U1RI’ is Ring Indicator</td>
<td>U1DTR’ is Data Set Ready</td>
</tr>
<tr>
<td>U1RTS’ is Request To Send</td>
<td>--</td>
</tr>
<tr>
<td>U1DTR’ is Data Terminal Ready</td>
<td>--</td>
</tr>
</tbody>
</table>

The support for DCE functions Data Carrier Detect and Ring Indicator can be emulated by using a general-purpose I/O signal and providing software support.

**Flow Control:** Flow control can be accomplished by either hardware or software.

**Hardware Flow Control (RTS/CTS):** Two devices are accomplished by connecting the U1RTS’ output to the Clear-To-Send (CTS) input on the receiving device, and connecting the Request-To-Send (CTS) output of the receiving device to the U1CTS’ input. The U1CTS’ input controls the transmitter may only transmit data when the U1CTS’ input is asserted. The U1RTS’ output signal indicates the state of the receive FIFO. U1CTS’ remains asserted until the preprogrammed watermark level are reached, indicating that the receive FIFO has no space to store additional characters.

**Software Flow Control (Modem Status Interrupts):** Flow control between two devices is accomplished by using interrupts to indicate the status of the UART.
Interrupts may be generated for the U1DSR’, U1DCD’, U1CTS’, and U1RI’ signals using bits 3:0 of the UARTIM register. The raw and masked interrupt status may be checked by using the UARTRIS and UARTMIS register. These interrupts may be cleared using the UARTICR register.

**FIFO Operation:** The UART has two 16x8 FIFOs; one for transmit and another for receiving. Using UART Data (UARTDR) registers both FIFOs are accessed. The read operations of the UARTDR register return a 12-bit value consisting of 8 data bits and 4 error flags while to write operations place 8-bit data in the transmit FIFO. The FIFOs are enabled by setting the FEN bit in UARTLCRH. The status of the FIFO can be monitored via UART Flag register (UARTFR) and the UART Receive Status register (UARTRSR).

Full and overrun conditions of the hardware monitors are empty. The UARTFR register contains empty and full flags (TXFE, TXFF, RXFE, and RXFF bits), and the UARTRSR register shows overrun status via OE bit. The trigger points at which the FIFOs generate interrupts is controlled via UART Interrupt FIFO Level Select register (UARTIFLS). Both FIFOs can be individually configured to trigger interrupts at different levels.

**Interrupts:** UART can generate the interrupts such as Overrun error, Break error, Parity error, Framing error, Receive timeout, Transmit and Receive. All of the interrupt events are ORed together before being sent to the interrupt controller. So that UART can only generate a single interrupt request to the controller at any given time. The software provides the multiple interrupt events in a single interrupt service routine by reading the UART Masked Interrupt Status (UARTMIS).
UART Initialization: To enable and initialize the UART, the following steps are necessary:

a. The peripheral clock must be enabled by setting the UART0, UART1, or UART2 bits in the RCGC1 register.

b. The clock to the appropriate GPIO module must be enabled via the RCGC2 register in the System Control module.

c. Set the GPIO AFSEL bits of the selected pins. To determine which GPIOs to be configured.

d. Configure the GPIO current level and/or slew rate as specified for the mode selected.

e. Configure the PMCn fields in the GPIOPCTL register to assign the UART signals to the selected pins.

To connect a microcontroller to a serial port on a computer, the level of the signals is adjusted so that communications take place. The signal level on a PC is -10V for logic zero and +10V for logic one. Since the signal level on the microcontroller is +5V for logic one and 0V for logic zero. So communication requires an intermediary stage that converts the levels. One chip specially designed for this task is Max-232 [12]. This chip receives signals from -10 to +10V and converts them into 0 and 5V.

MAX232 is a dual driver/receiver and has a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5V supply. Each receiver converts TIA/EIA-232-F inputs to 5V TTL/CMOS levels. Receivers have a typical threshold of 1.3V, a typical hysteresis of 0.5V, and accept ± 30V inputs. Each line driver converts TTL/CMOS input levels into TIA/EIA-232-F levels.
3.3 ARM Processor Peripherals

3.3.1 Digital to Analog Convertor

The DAC6573 is a low-power, quad channel and 10-Bit buffered voltage output digital to analog converter. Its on-chip precision output amplifier allows rail-to-rail output swing [8]. It utilizes an I²C compatible two-wire high-speed serial interface, with address support of up to sixteen DAC6573s for a total of 64 channels on the bus. I²C uses an open-drain technology, thus requiring the serial data line (SDA) and serial clock line (SCL) to be connected to VDD by resistors. Pulling the line to be grounded is considered logic “0,” and letting the line float is logic “1.” This logic configuration is used as a channel-access method. The transitions of logic states must occur while SCL is low, because transitions while SCL is high indicate START and STOP conditions. The typical supply voltages are 3.3 V and 5 V, although systems with higher or lower voltages are permitted [9]. Figure 3.11 gives the detailed schematic to interface to LM3S9B96 microcontroller or any other I²C interface protocol device. DAC6573 has 16 pin IC, SDA is the data signal and SCL is the clock signal. It operates 3.3V DC power.

Figure 3.11: Circuit diagram of DAC interface
DAC chip requires an external reference voltage to set the output range of the DAC. It incorporates a power-on-reset circuit that ensures the DAC output powers up at zero volts. It contains a power-down feature accessed via an internal control register that reduces the current consumption of the device to 200nA at 5V. The low power consumption makes it ideally suited for battery operated portable equipment. The power consumption is less than 3 mW at $V_{DD}=5V$ reducing to 1 μW in power-down mode.

### 3.3.2 Real Time Clock

A Real-Time Clock (RTC) is an IC clock that keeps track of the current time. RTCs are present in almost any electronic devices like servers and embedded systems, which needs to keep accurate time. RTCs often have an alternate source of power, so they can continue to keep time while the primary source of power is off or unavailable. This alternate source of power is normally a lithium battery system.

The bq32000 device [13] is an industry standard real-time clock. The bq32000 features an automatic backup supply with integrated trickle charger. The backup supply can be implemented using a capacitor or non-rechargeable battery. The bq32000 has a programmable calibration adjustment from –63 ppm to +126 ppm.

The bq32000 registers include an OF (Oscillator Fails) flag indicating the status of the RTC oscillator as well as STOP bit that allows the host processor to disable the oscillator. The time registers are normally updated once per second and all the registers are updated at the same time to prevent a time keeping glitch. The bq32000 includes automatic leap-year compensation.
3.3.3 Serial Flash Memory

The SS25VF016B and SST25VF064C are 25 series Serial Flash family featuring a four-wire SPI-compatible interface that occupies less board space and ultimately lowers system cost. **Figure 3.13** gives the details of pin diagram and a schematic diagram of the flash memory.

SST25VF016B is an SPI serial flash memory with high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. These devices significantly improve performance and reliability while lowering power consumption.
The devices write program or erase with a single power supply of 2.7-3.6V for SST25VF016B. The total energy consumed is a function of the applied voltage, current, and time of application, since for any given voltage range, the Super Flash technology uses less current to program and has a shorter erase time. The SST25VF016B device is available in both 8-lead SOIC (200 mils) and 8-contact WSON (6mm x 5mm) packages.
3.3.4 Relay Driver

The eight NPN Darlington transistor arrays in this ULN2800 family are ideally suited for interfacing between low logic level digital circuitry and external high current circuits. They feature open-collector outputs and freewheeling clamp diodes for transient suppression. The ULN2803 is designed to be compatible with standard TTL families with eight inputs and eight outputs. Figure 3.14 gives the details of the pin assignment of the driver as a microcontroller peripheral.

![Circuit diagram of Relay driver](image)

**Figure 3.14:** Circuit diagram of Relay driver

3.3.5 SIM900 GSM/GPRS

SIMCom provides an ultra compact and reliable wireless module-SIM900. This is a complete Quad-band GSM/GPRS module in an SMT type, designed with a very powerful single-chip processor integrating AMR926EJ-S core which allows benefit from small dimensions and cost-effective solutions.
Figure 3.15: Circuit diagram of SIM card interface

Figure 3.16: Circuit diagram of GSM/GPRS
Featuring an industry-standard interface, the SIM900 delivers GSM/GPRS 850/900/1800/1900MHz performance for voice, SMS, Data, and Fax in a small form factor and with low power consumption. With a tiny configuration of 24mm x 24mm x 3 mm, SIM900 can fit almost all the space requirements in your M2M applications, especially for slim and compact demands of the design. Figures 3.15 and 3.16 provide the SIM card and GSM schematic circuit diagrams to interface with microcontroller.

3.3.6 ISO35 RS-485 Differential Line Transceiver

The ISO15 is an isolated half-duplex differential line transceiver while the ISO35 is an isolated full-duplex differential line driver and receiver for TIA/EIA 485/422 applications.

Figure 3.17: Circuit diagram of Differential Line driver

These devices are ideal for long transmission lines since the ground loop is broken to allow for a much larger common mode voltage range. The symmetrical isolation barrier of the device is tested to provide 2500 Vrms of isolation for 60s
between the bus-line transceiver and the logic-level interface. Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or nearby sensitive circuitry if they are of sufficient magnitude and duration. **Figure 3.17** presents the pins detail from microcontroller to RS-485 differential line transceiver. These isolated devices can significantly increase protection and reduce the risk of damage to expensive control circuits. The ISO15 and ISO35 are qualified temperature for use from -40°C to 85°C.

### 3.3.7 Dedicated Power Supply

Digital circuits and processors operate on a regulated +3.3V or +5 volt power supply. The LM1117 voltage regulator [14] Integrated Circuit (IC) is an industry standard that sets the output voltage from 1.25V to 13.8V with only two external resistors. It is available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. It offers current limiting and thermal shutdown. The circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%. Sometimes capacitors are usually added to the circuit to filter and smooth out noise and to get a better 5 volts output. **Figure 3.18** shows a PCB digital power supply attached to the micro controller board to run microcontroller and its peripherals interfaced to it.
3.3.8 ARM Processor and Transmitter Interface Connector

A 50-pin FRC connector J2 is provided for interface between transmitter sensors/controls and ARM Cortex-M3 target board. The interface connector J2 pin details are presented in the Figure 3.4. The inputs are the ADC channel inputs from transmitter sensors and Relay driver outputs to the transmitter.

![Circuit diagram of input/output Extension](image)

Figure 3.19: Circuit diagram of input/output Extension
3.4 Transmitter Hardware Interface

The MST Radar system operates at 53 MHz and generates 2.5 mega watts RF power using 32 high power vacuum-triode based transmitters Tx that has been installed and running successfully since 1991. The detailed description of radar and transmitter is covered in the introductory chapter.

The transmitters were installed with control and interlock units based on the LSI TTL logic devices with control and interlock unit spreading over 15 PCBs in each transmitter as shown in Figure 3.20. The interlock subsystem receives input from the sensors placed in the amplifier cavities and monitors a total of 12 safety interlock parameters.

![Figure 3.20: Photograph of the TTL ICs based control and interlock units](image)

This unit has independent logic circuits to process inputs for indication of any abnormal voltage, temperature and current deviations, and switches-off the transmitter subsystems incase of the faults with the help of control unit. This ensures the protection of the expensive devices from any failure in the system. The control circuit ensures the proper ON/OFF sequence for the transmitters cathode, heater then anode supplies switching ON’ with a time gap of 3 minutes each, i.e. A total of 6 minutes is
required for warm up of the transmitter triode amplifiers. All the four amplifier stages in the transmitter use expensive devices. A comprehensive safety interlock is built into the transmitter to protect these devices. The interlock unit senses anode voltage, heater current and airflow in each RF amplifier to ensure them within the safe limits. It automatically switches OFF respective power supplies to prevent critical damage to the transmitter. This research activity provided advancement of technology of control and interlock units based on the LSI TTL logic devices spread over 15 PCBs in each transmitter, to high speed ARM Cortex processor, centralized LAN based interlock and control system.

### 3.4.1 Transmitter Amplifiers

The pre-driver (PDR), driver (DR) and high power amplifiers (HPA) are high power triode amplifiers with 11dB gain at each stage to generate about 1kW, 10 kW, and 120 kW peak pulsed output power at the respective amplifier output. 3CX1500A7, 3CPX1500A7 and 3CX5000A7 triodes of Varian/CPI make use in grounded grid class C amplifiers to generate high peak powers.

The following Figures 3.21, 3.22, 3.23 present the RF cavity and an RF power flow scheme thorough RF tank circuits L1-C1-C2 and L2-C4-C5. The figures show filament supply, cathode supply, anode (HT-High Tension) voltage connectivity to triode. As soon as transmitter amplifier is switched on, cathode voltage is applied to triode. After ensuring cathode voltage application, the filament voltage is applied to triode using safety interlocks. The filament timer ensures 50% filament power application for first 3 minutes and then full filament power is applied to triode to avoid temperature surge. After a further 3 minutes triode filament warming with full power, another timer activates to connect HT to triode anode. Filament current is monitored using current transformer and full wave rectifier circuit, to bring out the
rated current application to triode. It also provides information about the filament supply application to triode (if not; zero current). The airflow sensor monitors the forced air cooling of triode for proper heat dissipation in the RF cavity. The anode voltage is sensed by bleeder (potential divider) circuit to generate a TTL level signal for digital circuits’ monitoring purpose. In the present activity, ADCs are used to digitize the actual voltages, to monitor minute variations to ensure better safety.

![Figure 3.21: PDR RF Amplifier Cavity Power Supplies and Sensor Network](image)

The RFC (Inductor- RF choke) and using two filaments (bifilar) chokes pass DC but stop RF entering power supplies. E1 is a spark gap to limit input to a rated limit. Anode current and grid current meters represent respective values; anode
current is representative of RF output power, grid current is an amplifier internal safety monitor. Grid current should be at a minimum.

**Figure 3.22:** DR RF Amplifier Cavity Power Supplies and Sensor Network
Figure 3.23: HPA RF Amplifier Cavity Power Supplies and Sensor Network
3.5 Tx Interlock Control Operations

3.5.1 Air Flow (PDR, DR and HPA)

Any transmitter amplifier cavity fan fails, it is sensed by interlock circuit and it switches OFF the RF input power and the anode power supply of the respective amplifier.

![Circuit diagram of Airflow monitor](image)

**Figure 3.24:** Circuit diagram of Airflow monitor

A single phase 230V AC fan cools PDR amplifier. The optical coupler circuit senses the applied voltage to fan terminals and provides sense voltage for interlock. A blower IMA-15 (230V, 100cfm) has been used in the pre-driver amplifier plug-in for cooling the triode. When the fan is “ON” resistance R connected in series with the blower develops an AC voltage shown in Figure 3.24. This AC voltage is rectified and filtered into a DC voltage which drives an opto-coupler. The opto-coupler output is ‘0’ when the fan is ‘ON’ and is ‘1’ when the fan is ‘OFF’. This information is passed to interlock plug-in.
Figure 3.25: Blower (fan) monitor circuit for DR Amplifier.

Three phase AC blower fans are used for DR and HPA. A blower is used in the driver amplifier plug-in for cooling the triode. The airflow in these cavities is sensed by a wind flap/vane near the fan within the RF cavity which is attached to a micro-switch as shown in Figure 3.25. The microswitch with a kapton flap attached to the lever senses the airflow from the blower. The microswitch is in the NC mode when the fan is OFF and the voltage sensed by the interlock circuits is +5V (fault signal). When the blower is started, because of the airflow pressure on the kapton flap, the switch changes its connection to NO mode which is grounded. The zero (0) voltage is sensed as the operating state, when the fan attains full speed. That is the switch changes its state because of air pressure and gives low output; interlock circuit continuously monitors this output. These parameters for different amplifier stages come out from their respective plug-in back panel connectors. The system interlock logic senses output of comparator card if any fan failure is sensed. It automatically switches OFF, RF input power and the corresponding anode power supply.
3.5.2 Cathode Voltage (PDR, DR and HPA)

A sample voltage of approximately 4.2V is generated from each cathode supply. This sampled voltage comes with the back panel connector of each amplifier plug-in. These signals are compared with pre-set reference voltage which corresponds to the minimum cathode voltage required for the respective amplifier stage. If any of these cathode monitor signal fall below, the pre-set reference voltage logic circuit switches ‘OFF’ RF input power and the anode supply of the respective amplifier stage.

3.5.3 Filament Current (PDR, DR and HPA)

![Circuit diagram of current transformer in series with the filament transformer](image)

**Figure 3.26:** Circuit diagram of current transformer in series with the filament transformer

A DC voltage 3.5V proportional to rated filament current is generated by using a current transformer in series with the filament transformer is shown in **Figure 3.26**. This signal is then sent to status and fault indicator plug-in for further processing. Here signal is compared with a pre-set reference voltage which corresponds to the maximum operating filament current. If sense voltage is less than the pre-set reference voltage, logic circuit switches off anode supply of the amplifier stages. If the sensor voltage goes below the preset reference voltage, due to failure of...
triode, logic circuit switches ‘OFF’ RF input power as well as anode supply of that amplifier stage.

### 3.5.4 Anode Voltage (PDR, DR and HPA)

![Circuit diagram of Anode voltage power supply](image)

**Figure 3.27:** Circuit diagram of Anode voltage power supply

**Figure 3.27** is one of the Anode voltage power supply circuit and list components are given in Table 3.6. Pre-Driver amplifier plug-in requires an anode supply of 2.5kV DC, Driver amplifier anode supply is 5.6kV, and HPA anode supply is 6.2kV. A sample voltage of the order of 4.2V DC has been generated by using a bleeder network and is driven out by feed through capacitor mounted on the RF portion of the plug-in. HPA anode supply of 6.2kV is monitored using similar potential divider networks to get the sense voltage of about 3V.
Table 3.6: Components of Anode Supply Circuitry

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| T1   | Three phase high voltage transformer  
      Primary: 0-400-440  
      Secondary: 0-4150-5320 |
| T2   | Transformer for Lamp  
      Primary: 0-230V  
      Secondary: 12V |
| L1   | Filter Choke 2H, 200 mA |
| D1-D6| Meltron HVR-10 |
| C    | 10M 2YQ (2uF 10 KV) CSI Cap. USA |
| RL   | 56 ohms, 60W |
| R    | 180 K - 3 W - 12 No. in series |
| R1   | 3.9 K - 3W |
| R2   | 3.3 K - 3W |
| R3   | 220 - 3W |
| RF   | 3.9K - ½ W POT |
| M    | RS BPM-85 Panel Meter - Full Scale 100 μA |

Figure 3.28: Circuit diagram of Resistor divider (bleeder)
Figure 3.28 represents a number of series resistors that have been put between the anode supply and the cathode supply for anode voltage monitoring. The bleeder circuit is a simple potential divider circuit with large number of high power/watt and high value resistors connected in series. Anode supply monitoring voltage is taken out from one of the resistor according to potential divider formula \( V = I x (R_2/R_1+R_2) \) for getting monitor voltage from bleeder circuit, without loading the high voltages and taking safety precautions in HT section.

A sample of 4.2 volts is generated and the same is given to the interlock. These signals come out from each amplifier plug-in in back panel connector. These signals are compared with a reference voltage which corresponds to the minimum anode voltage required for that amplifier stage, if the sample voltage is less than the reference voltage, RF input power cannot be switched ON, because if RF power is applied in the absence of anode supply, large grid current will flow in the amplifier which can cause damage to the triode tube. So this protection circuit ensures that RF input power will not be applied in the absence of anode supply.

3.5.5 Excess Anode Voltage (PDR, DR and HPA)

A sample of 4.2 volts is generated using resistive divider. This sample voltage is taken out from cavity amplifier plug-in through back connector. Each signal gets compared to a preset reference voltage which corresponds to maximum operating anode voltage for that particular tube amplifier stage. If the parameter exceeds its preset limit, a high signal is generated. In case of excess anode voltage, interlock switches OFF RF input power and the same anode power supply.
3.5.6 Excess Anode Current (PDR, DR and HPA)

Anode current sensing card has been put behind the cavity amplifier plug-in. A sense voltage corresponding to anode current has been taken out. These signals enter interlock and these parameters are compared with the reference voltage which corresponds to maximum operating DC or average current for that amplifier stage. If the parameter exceeds its preset limit logic circuit senses it and switches OFF RF input power and anode power supply for the same amplifier stage.

3.5.7 Temperature of Tube (PDR, DR and HPA)

![Circuit diagram of Temperature monitoring](image)

**Figure 3.29:** Circuit diagram of Temperature monitoring

A transducer is used to sense the temperature of the hot air coming out of the tube anode pins is shown in Figure 3.29. The transducer develops a DC voltage proportional to the temperature of the hot air which comes out from the amplifier plug-in back panel connector. If any of the signals exceeds the preset reference voltage, the logic circuit switches OFF RF input power to the transmitter as well as the anode power supply of the corresponding tube.
3.5.8 SSA Power Supply Overload

The 24V DC power supply for the solid-state amplifier has a specific current limit. If more current is drawn from the supply, due to failures like excess heating of MOSFET amplifier or oscillations due to unwanted RF feedback; the amplifier draws more power supply current and DC supply voltage falls. When current drawn is more than the supply rated current from the power supply, the SSA overload occurs. The power supply voltage reduces automatically. A potential divider and comparator circuit is used to monitor the SSA overload, so that the variation in the supply voltage is sensed, and if it falls below a preset reference voltage, logic circuit switches OFF RF input power and SSA power supply.

3.5.9 Excess Antenna VSWR

Voltage Standing Wave Ratio (VSWR) provides antenna feeder network health parameter. The antenna array feeder network failures as water entry into RF cavities and loose connectivity sparks or arcing changes feeder network impedance and RF power reflections and standing waves in feeder network are observed. This further aggravates the failures in feeder network and transmitter high power output stages. To monitor the RF power reflections from the antenna feeder network, a dual directional RF power coupler is available at transmitter output. The coupled reflected RF output power from the dual directional coupler enters SSA plug-in where it is detected and fed to the sample and hold circuit where it converts RF pulse into DC voltage corresponding to its amplitude. The circuit gives DC voltage corresponding to the reflected RF power. This DC voltage is compared with a preset reference voltage which corresponds to maximum allowable reflected RF power setting (VSWR 2:1). If
the parameter exceeds the reference voltage, the logic circuit switches OFF RF power to the transmitter.

3.5.10 External Error

The transmitter safety is fully ensured by another interlocking system which monitors duplexer microwave pin diodes health. Each duplexer is operated using 9-pin diodes and any diode failure, reduces isolation of duplexer and the transmitter gets reflections and excessive leakage power damages sensitive receiver systems. The diodes biasing and voltage sensing system sends a logic TTL signal in case of failure. This voltage is sensed and interlock circuit switches OFF RF input power to the transmitter.

3.6 Transmit Power Display/Record Management

![Block diagram of Tx Power Display/Management]

**Figure 3.30:** Block diagram of Tx Power Display/Management
3.6.1 High Power Solid State Amplifier

The high power Solid State Amplifier (SSA) consists of MOSFET amplifiers. It has a nominal driver requirement of 0 dBm. This SSA is capable of delivering power up to 80 watts. The power supply to SSA is regulated +28V DC and is available from the Low Voltage Power Supply (LVPS) unit. The SSA module has the associated RF circuits for transmitter power display, and reflected power display using RF detectors, video amplifiers, sample and hold circuits as shown in Figure 3.30. The Automatic Level Control (ALC) circuit is also hardwired in this module. If Tx output is not within ALC loop, it is displayed using an unleveled LED.

The RF flow in the solid state amplifier is through PIN diode switch, pin diode attenuator (ALC attenuator) and gain control attenuator, and then applied to Solid State Amplifier. The pin diode switch is a voltage controlled absorptive RF control which is used to control Tx RF input drive in case of failures in transmitter modules for safety. The ALC attenuator has attenuation range of 0.5 dB to 18dB, to keep the transmitter output at the rated power level. The gain control attenuator is used to set the transmitter output using transmitter front panel, manually.

Samples of Tx forward transmitted power and reflected power at the output of the transmitter are monitored using 60 dB dual directional co-axial coupler located after the transmitter. The sampled forward and reflected RF signals are fed into a two channel detector and video amplifier assembly. The pulsed output (from video amplifier) corresponding to forward and reflected powers are given for reading transmitter power level of transmitter front panel analog panel meter, automatic level control feedback circuit and interlock respectively. SYNC Pulse (available from distribution rack located in local processor room) is also fed to these two cards for
enabling the controls, the attenuation level of the PIN attenuator whereas the output of
interlock card controls the ON/OFF state of the PIN switch. A two channel detector
and video amplifier circuit, ALC and interlock cards ensure Tx at rated output power
level. Due to aging, this circuitry is not functioning and getting a power rating of the
transmitter is becoming difficult. Hence, the Tx power level recording in computer
database and software controlled ALC are experimented in the present activity.

3.6.2 Transmitter power supply

Distribution panels are used to distribute the AC mains supply to different plug-
ins as well as to the EHT transformers through some control circuits. The three phase
mains power (400V, 3-phase) for the transmitter enters the rack through 16 amp fuses.
The single phase preventer circuit would de-energize the contactor in case of failure
of any of the three phases. Two micro switches S1 and S2 are connected in series with
these relays which act as the door interlock. Three line filters are connected to the 3-
phase lines to eliminate electrical interference. The switch ON sequence demands that
the 3-phase supply for fans be switched ON prior to switching ON the transmitter
mains. A separate 3-phase line is used for all blowers and fans in the Tx rack. All fans
remain 'ON' after about 10 minutes of switching OFF of transmitters using the FAN
timer relay circuit for total cooling of the transmitter.

Three phase mains power for Pre-driver, Driver and HPA anode supplies are
controlled through three contactors, through which AC supplies to the primary of
anode voltage (HT) transformers are applied. Unless both the EHT timer and the relay
are ON and their respective relay contacts are made, no contactor will be energized
and hence no anode supply will be ON. The relay control is derived through the
control unit and passed thru interlock for safe operations. The EHT timer ensures that
a cathode warm-up time of 3 minutes for triodes is allowed before the application of the anode supply. In the event of any malfunction in the transmitter, the same relays are used to switch OFF the anode supplies automatically as dictated by the 'Status & Fault Indicator' (Interlock) plug-in in conjunction with the 'Control Unit'.

### 3.6.3 Custom Built Power Supply (CBPS)

![Figure 3.31: Photograph of Transmitter Custom Built Power Supply](image)

The digital circuits in control and interlock unit, SSA ALC card, Interlock card and SSA amplifier module require low voltage power supplies. A custom built power supply (CBPS) in transmitter provides these four DC output voltages using linear power supply modules (1) +5V, 2Amps, (2) +15V, 2Amps, (3) -15V, 1Amps and (4) +28V, 3Amps as shown in Figure 3.31.

### 3.6.4 Transmitters output RF power measurement and archival

A method is developed to measure the transmitter pulsed RF signal amplitude to derive total radar Tx power output ($P_t$). In this activity, we developed a method of Automatic Level Control (ALC) for MST radar transmitter and logging the power level at remote radar controller computer using ARM processor based card. The triode based pulsed power transmitter output is maintained at constant level using the developed automatic level control. The transmitter forward power is obtained using a
60 dB directional coupler. This low power RF pulse is converted into a DC pulse using the diode detector module. Video amplifier amplifies the DC pulse amplitude to the required level for digitization. An ARM Cortex-M3 microcontroller system based card digitizes the DC pulse; the necessary equation for corresponding DC level output for controlling RF power is incorporated into software to generate a DC voltage from the DAC for ALC attenuator. Transmit power level is transferred to the remote radar controller computer over an ethernet LAN for computing total transmitted power ($P_t$). ADC, ethernet controller and DAC are interfaced to ARM by I2C protocol. The DAC output is given to RF attenuator to provide attenuation in the range of 0.5 dB to 18 dB for a control voltage variation from 0V to 12V. The transmitter ALC track range is within in 3 dB and stable output range of 1 dB is partially fulfilled.

Transmitter output power at 60 dB coupler = $V_{(pk-pk)} = 3V$

Power = $V_{rms}^{2/R}$ ................................................................. (1)

Power = $(V_{(pk-pk)}^{2/8xR}) = [V_{(pk-pk)}^{2/800}] \times 10^6 = 22.5 \text{ K watts}.........(2)$

Power = $10 \times \log (\text{power}) / 10^{-3} = 73.5 \text{ dBm}......................... (3)$
3.7 ARM Cortex-M3 Processor based Control and Interlock Unit

The hardware of the ARM Cortex-M3 based centralized control and interlock consists of the following major sub sections.

3.7.1 Experimental Setup

Figure 3.32: Photograph of complete view of experimental setup and working model

The web based remote monitor and controller system integrated with the MST radar transmitter is shown in Figure 3.32. The signal FRC cable is connected to the embedded target board which is taken from the transmitter. The power +14V DC from Low Power Supply (LPS) resides in transmitters and is applied to ARM Cortex-M3 microcontroller unit. The LAN cross cable is plugged to the personal computer from the ARM Cortex-M3 microcontroller unit. It goes to the internet browser through the corresponding IP address and finally the web page is obtained.
The printed circuit board ARM Cortex-M3 (LM3S9B96) and is specially designed for industrial applications purpose is shown in Figure 3.33. This section will explain about components that are used in the system. It includes the radar transmitter, microcontroller LM3S9B96, ADC, DAC, RTC, power supply (5V/3.3V), RJ45 ethernet communication of microcontroller and relay circuitry to control the transmitter.

Table 3.2 presents the pin assignments of LM3S9B96 microcontroller in MST radar health monitoring and controller system. Pins not stated in the table are not used and left hanging. Figure 3.34 shows the complete overview of the web based remote monitoring and controller system. At the beginning, the microcontroller will receive command signals from a personal computer through ethernet port. The detected transmitter’s triode amplifier signals are read by microcontroller through ADC channels. The microcontroller is operated as it is user programmed as per the application.
The ARM processor board is interfaced to transmitters using 12 ADC channels and 8 I/O lines. The ethernet connector on the ARM board is connected to a computer to browse the transmitters through cat-5 LAN cable. The power supply and ground are taken from the transmitter supply box and there is no need to connect external supply for the ARM board. The DB-32 pin connector consists of sensor outputs, input controls, grounds and power supplies. The pins are connected through the help of box header on ARM board to control and monitor the T/R modules. The two 10-bit ADCs 12 channels ADC0, ADC1 to ADC12 are interfaced to the triode amplifiers that are cathode voltages PDR, DR and HPA, heater voltages PDR, DR and HPA, heater current monitor PDR, DR and HPA, SSA ALC and fan operation.

The ARM microcontroller board has a control inputs PJ5 and PJ7 and are connected to the Tx ON/OFF and RF ON/OFF of the transmitter. The TX and RF are connected to relay card which is interfaced with the transmitter sensor device. The ARM always reads the sensor data (analog signals) and converts into digital form and updated to buffer. After converting digital form, ethernet process is initialized and framed the packet. This ethernet packet sends to the web server running on the personal computer client. A packet is simply a chunk of data enclosed in one or more wrapper that help to identify the chunk of data and route it to the correct destination. Destination in this sense means a particular application or process running on a particular machine. These wrappers consist of headers, or sometimes headers and trailers. Headers are simply bits of data added to the beginning of a packet. Trailers are added to the end of a packet. The ARM board receives the commands in the form of ethernet packet for the user through a standard web browser. After receiving user commands from client system, the server perform the appropriate actions like turning OFF/ON the specified devices in transmitters.
### Table 3.7: Hardware interfacing of Transmitter sensors to MCU

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Description</th>
<th>Transmitter Sensors</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC0</td>
<td>1</td>
<td>Input Pin</td>
<td>Video-Amplifier output (ALC purpose)</td>
</tr>
<tr>
<td>ADC1</td>
<td>2</td>
<td>Input Pin</td>
<td>PDR Current</td>
</tr>
<tr>
<td>ADC2</td>
<td>5</td>
<td>Input Pin</td>
<td>PDR Anode Supply</td>
</tr>
<tr>
<td>ADC3</td>
<td>6</td>
<td>Input Pin</td>
<td>Dr Fan</td>
</tr>
<tr>
<td>ADC4</td>
<td>100</td>
<td>Input Pin</td>
<td>Dr Current</td>
</tr>
<tr>
<td>ADC5</td>
<td>99</td>
<td>Input Pin</td>
<td>Dr Anode Supply</td>
</tr>
<tr>
<td>ADC6</td>
<td>98</td>
<td>Input Pin</td>
<td>HPA Fan</td>
</tr>
<tr>
<td>ADC7</td>
<td>97</td>
<td>Input Pin</td>
<td>HPA Current</td>
</tr>
<tr>
<td>ADC8</td>
<td>96</td>
<td>Input Pin</td>
<td>HPA Anode Supply</td>
</tr>
<tr>
<td>ADC9</td>
<td>95</td>
<td>Input Pin</td>
<td>PDR Fan</td>
</tr>
<tr>
<td>ADC10</td>
<td>92</td>
<td>Input Pin</td>
<td>DAC a output to ALC Attenuator</td>
</tr>
<tr>
<td>ADC11</td>
<td>91</td>
<td>Input Pin</td>
<td>SSA Overload</td>
</tr>
<tr>
<td>ADC12</td>
<td>13</td>
<td>Input Pin</td>
<td>VSWR</td>
</tr>
</tbody>
</table>
Table 3.8: Power Supply connection for LM3S9B96, Tx control system and Ethernet port

<table>
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<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Description</th>
<th>Radar Transmitter</th>
</tr>
</thead>
<tbody>
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<td>VDD</td>
<td>8</td>
<td>Positive Supply +3.3V</td>
<td>Power supply to chip</td>
</tr>
<tr>
<td>VDD</td>
<td>20</td>
<td>Positive Supply +3.3V</td>
<td>Power supply to chip</td>
</tr>
<tr>
<td>VDD</td>
<td>44</td>
<td>Positive Supply +3.3V</td>
<td>Power supply to chip</td>
</tr>
<tr>
<td>GND</td>
<td>94</td>
<td>Ground Reference</td>
<td>Ground reference to the chip</td>
</tr>
<tr>
<td>GND</td>
<td>82</td>
<td>Ground Reference</td>
<td>Ground reference to the chip</td>
</tr>
<tr>
<td>GND</td>
<td>9</td>
<td>Ground Reference</td>
<td>Ground reference to the chip</td>
</tr>
<tr>
<td>ADC13</td>
<td>12</td>
<td>Input/Output Pin</td>
<td>--</td>
</tr>
<tr>
<td>ADC14</td>
<td>11</td>
<td>Input/Output Pin</td>
<td>--</td>
</tr>
<tr>
<td>ADC15</td>
<td>10</td>
<td>Input/Output Pin</td>
<td>--</td>
</tr>
<tr>
<td>RXIN</td>
<td>37</td>
<td>Ethernet +ve I/P</td>
<td>PC RX</td>
</tr>
<tr>
<td>RXIP</td>
<td>40</td>
<td>Ethernet -ve I/P</td>
<td>PC RX</td>
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<tr>
<td>TXON</td>
<td>46</td>
<td>Ethernet +ve O/P</td>
<td>PC TXON</td>
</tr>
<tr>
<td>TXOP</td>
<td>43</td>
<td>Ethernet -ve O/P</td>
<td>PC TXOP</td>
</tr>
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<td>PJ5</td>
<td>53</td>
<td>Input/Output Pin</td>
<td>TX ON/OFF Relay control</td>
</tr>
<tr>
<td>PJ7</td>
<td>55</td>
<td>Input/Output Pin</td>
<td>RF ON/OFF Relay Control</td>
</tr>
</tbody>
</table>
Block diagram of complete overview of the system

Figure 3.34: Block diagram of complete overview of the system
Figure 3.35 (a): Schematic diagram of ARM Cortex-M3 (LM3S9B96) processor board.
Figure 3.35 (b): Schematic diagram of ARM Cortex-M3 (LM3S9B96) processor board.
Figure 3.35 (c): Schematic diagram of ARM Cortex-M3 (LM3S9B96) processor board.
REFERENCES


[12] Successive Approximation Analog to Digital Converter, By Team Number 7 Nila Barot

