CHAPTER-1
INTRODUCTION

1.1 Introduction

The need for portable devices operating at low power and at high speeds is growing day by day. During the recent years there is a huge demand for portable devices and they all demand for low power dissipation. Hence low power design has emerged as a very striking and fast growing field. High performance digital systems such as DSP, microprocessors, and other applications demand for low power design. The low power operation is essential mainly to increase the battery life and to reduce the cost of excessive cooling, and to avoid failures because of hot spots etc.

In view of this it is essential to minimize the power dissipation in digital integrated circuits. The various techniques that are employed to reduce the power dissipation are recycling the energy that might be stored in nodal capacitances, reduction in voltages and currents, reduction in transitions (0 to 1 or 1 to 0), and so on. The techniques based on operation at very low currents usually below the normal conduction region, especially in FET based circuits is known as sub threshold operation. Sub threshold circuits work generally with a supply voltage less than the threshold voltage of transistor and leakage current is used as operating current. As power is related quadratically to the supply voltage, reducing the voltage to ultra low levels causes a reduction in power consumption. These circuits are limited to low frequency applications, because of low current operation. Conventional
digital CMOS circuits have two modes of operation called ON mode (saturation) and OFF mode (sub threshold mode). But sub threshold circuits are either in OFF mode or an almost-ON mode (still in sub threshold region). This has fascinated several investigators, as it has flexibility to choose their own logic levels and power dissipation. But the main drawback of this technique is the circuits suffer from large delays and hence the realization of high frequency circuits becomes complicated. This is due to small driving current.

Sub threshold circuits offer a good choice for applications like RFID tags, medical equipment such as hearing aids and pace makers, wearable computing or implants, personal digital assistants, laptops etc where power reduction is the main concern and speed is of secondary importance. Then the concept of dynamic threshold MOSFET (DTMOS) with variable substrate voltage have been invented to improve the driving current of sub threshold CMOS circuits. This DTMOS technique does not seem to be enough to bring down the power dissipation to a lower value. Analysis of various techniques and idea behind the evolution of these techniques has resulted in the proposal of Variable threshold MOSFET (VTMOS) circuits which forms the basis for this thesis.

This thesis is an effort to modify the operation of normal sub threshold DTMOS circuits, by reducing the power dissipation without affecting the performance. The modified operation that is suggested is based on biasing the substrate of FET dynamically in tune with the gate voltage and is termed as variable threshold MOS (VTMOS) operation.
It has been shown that VTMOS operation can result in power saving of up to 54% (under the sub threshold condition of operation as chosen in this thesis) compared to sub threshold CMOS and DTMOS operation and they can be cascaded as that of CMOS circuits. The thesis depicts the same effort in the following chapters.

### 1.2 Formulation of the problem

Several approaches have been suggested, in which fixed forward body bias is applied, to increase the speed of the sub threshold circuits. The main drawback of these approaches is that the threshold voltage is decreased both in ON and OFF states resulting in increase in leakage power even in OFF state. To overcome this problem, some variable threshold circuits are proposed. They employed an additional stabilization scheme to provide appropriate body bias. The body bias can be varied by reducing the threshold voltage in the active mode and increasing the threshold voltage in standby mode. Another approach is multi threshold voltage CMOS. This technology has both low threshold voltage and high threshold voltage MOSFETS. The low threshold MOSFETS increases speed, while high threshold voltage MOSFETS suppress the standby leakage current, during the sleep mode. However these reduction techniques in standby mode have complex architectures and occupy large chip area. Hence a simple method called DTMOS technique is suggested, where the body is connected to gate and body bias varies with gate voltage. In this case no additional circuitry is needed. when the gate voltage is high (ON condition), the forward body bias is applied, causing reduction in threshold voltage and providing
large driving current which is better than that in sub threshold CMOS circuits. Hence this can be used in high speed applications and when the gate voltage is low, i.e. when it is in OFF state, the threshold voltage increases which results in low leakage current and this leakage current is equivalent to CMOS leakage currents.

In order to reduce the leakage current of DTMOS further in OFF mode, a new technique called Variable Threshold MOSFET technique (VTMOS) technique is proposed in this thesis. Through this method a fixed bias is applied between gate and substrate in such a way that the leakage current can be further reduced and at the same time the current drive is maintained at a reasonable level. This approach is investigated for realizing digital sub threshold circuits and showed that it is feasible to realize all basic logic gates and complex digital systems.

All the investigations are carried out using Hspice simulation tool and the new technique (VTMOS technique) mainly focused on sub threshold region of operation and has a significant improvement in power reduction (up to 54%), compared to sub threshold MOSFETS and DTMOSFETS. The other performance parameters like propagation delay, power delay product, cascadability are comparable with sub threshold CMOS and DTMOS circuits. These investigations form the contents of this thesis. The suggested technique (VTMOS) is relatively simple and achieve considerable reduction in power dissipation and leakage current, while maintaining other performance characteristics at acceptable level.
1.3 Objectives

The main objective is the performance evaluation of VTMOS technique for low power VLSI digital circuits. The following issues associated with the main objective are addressed.

- To study the suitability of NMOS and PMOS transistors under VTMOS condition ($I_{ds}$-$V_{ds}$ and $I_{ds}$-$V_{gs}$ characteristics for different substrate bias) for circuit applications.
- To study the characteristics of VTMOS Inverter through simulation and evaluate its performance.
- To realize basic digital logic circuits and sequential circuits using VTMOS approach.
- To understand the feasibility of realizing complex digital circuits using basic VTMOS family.
- To examine the scope of applying VTMOS approach for digital VLSI systems.
### 1.4 Methodology used

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1.5 Contribution of the Thesis

- Conceiving VTMOS operation.
- Realizing basic universal logic gates and basic sequential circuits based on VTMOS family.
- Realizing cascadable digital blocks.
- Demonstration of VTMOS based digital systems.
- Proposing VTMOS digital circuit family for low power and low leakage digital systems.

1.6 Organization of Thesis

Chapter 1 is an introductory chapter which brings out the importance of low power design of VLSI circuits and the role that VTMOS circuits can take part in. Chapter 2 is devoted to the description and fundamentals needed to appreciate the operation of FETS and FET based circuits. Chapter 3 emphasizes the literature survey. The Chapter 4, Chapter 5, Chapter 6, Chapter 7 and Chapter 8 are devoted to demonstrate the feasibility of VTMOS circuits (both VTMOS basic combinational, sequential circuits and other digital systems). Chapter 9 concludes with a note on the advantages and limitation of VTMOS circuits for electronic gadgets.