CHAPTER-3

REVIEW OF LITERATURE

This section deals with different power reduction techniques like Supply voltage reduction, Effective capacitance reduction, Switching activity reduction, Reduction of leakage and static current, Adiabatic circuit approach ,Technology scaling and Power reduction using sub threshold region and different body biasing techniques.

3.1 Low power digital design techniques

3.1.1 Supply voltage reduction

Anantha P. Chandrakasan in his article [7] focused on the supply voltage reduction for obtaining low power. The switching power consumed is a quadratic function of the operating voltage. Hence reducing the operating voltage, results in considerable reduction of switching power. However reducing the operating voltage, increases the delay of the different logic circuits, since the delay is proportional to the capacitor being charged and discharged and inversely proportional to $V_{dd}/(v_{dd}-v_{th})^2$, being $V_{th}$ the threshold voltage. Hence he concluded that power reduction through supply voltage reduction results in increase in delay and in turn reduces the throughput.

3.1.2 Effective capacitance reduction

Effective Capacitance reduction is one of the means for power reduction and this can be obtained by reducing the physical capacitance and the switching activity.

3.1.3 Physical capacitance reduction

Physical capacitance reduction is a technique for low power consumption. Bellaouar.A[13] said that the physical capacitance present at the output of a CMOS gate is the sum of the three components. There are 1) Total input capacitance of N driven gates 2) Parasitic output capacitance of the driver gate and 3) Wiring (routing and interconnect) capacitance.


3.1.4 Switching activity reduction

Switching activity reduction is one technique for power reduction. Callaway.T.K [24] in his work discussed on the speed and dynamic power consumption of CMOS implementations of six different adders.wide simulations are carried out by him, to evaluate their switching
characteristics and the outcome of those simulations are used to rank the adders on speed, size and number of logic transitions. The same type of investigations are carried out by him for various parallel multiplier circuits and is reported by him in [25]. For minimizing switching activities of logic networks, Technology decomposition and Mapping techniques have been introduced by Tsui.C.Y[26], Tiwari.V[27], Macii.E [28] and Bisdounis.L [29]. The concept of Technology decomposition and Mapping is to first decompose a given Boolean network such that the total switching activity of the network is minimized. Further power reductions are achieved by hiding high activity nodes inside more complex CMOS gates. This is because complex gates tend to exhibit an overall lower capacitance since more signals are confined to internal nodes rather than to the more heavily loaded output nodes. In this way signals with high switching activities are mapped to low capacitance internal nodes.

Pedram.M [30] focused on power consumption of glitches. He said that in CMOS circuits, an average of 15-20% of total power is consumed in glitching. Schimpfel C.V [31] proposed a retiming approach for placement of registers to balance different path delays for glitch reduction.

A sequential optimization technique which pre computes the output logic values of a circuit, one clock cycle before they are required have been presented by Alidina .M[32]. The pre computed logic values are then used in the following clock cycle to reduce the switching activity at the internal nodes of a circuit. However the pre computation logic adds to the circuit area and can also result in an increased clock.
Musoll.E and Jortadella.J [33] presented Scheduling and Resource binding algorithms for low power data path design. The algorithms minimize the number of transitions on the signals feeding functional units (adders, multipliers, etc) and register which effectively minimize the switched capacitance. Kim.D and Choi.K[34] proposed loop folding technique for minimizing the number of transitions in the input operands of a functional unit.

### 3.1.5 Reduction of leakage and static current

Gary yeap[35] discussed about reducing leakage and static current in digital circuits for overall power reduction. Leakage power dissipation of a CMOS digital circuit is several times smaller than dynamic power. The leakage power problem mainly appears in very low frequency circuits or one with “sleep modes” where dynamic activities are suppressed. Static current can be reduced by transistor sizing, layout techniques and careful circuit design.

### 3.1.6 Adiabatic circuit approach

Adiabatic circuit approach is an approach, where the energy that is normally wasted in discharging the nodal capacitances is collected and recycled. Younis.S [36] and Koller.J [37] proposed Adiabatic or Charge recovery circuits for low energy requirements. These circuits resonate the load capacitance with an inductor, which recovers some of the energy needed to change the capacitor’s voltage. The energy loss in switching the load can be reduced to $\tau/TCV^2$ where $\tau$ is the intrinsic delay of the gate, and $T$ is the delay set by the LC circuit, while this case in trading energy for delay is attractive, the energy delay product for these circuits is much
worse than normal CMOS gates. This is studied by Indermaur.T [38]. Thus adiabatic circuits became attractive only when you need to operate at delay beyond the range feasible by voltage scaling and transistor sizing standard CMOS.

### 3.1.7 Technology scaling

One way to greatly improve the energy delay product and thus save energy is to improve the technology. In ideal scaling proposed by Dennard.R [39], all voltages and linear dimensions are reduced by a scale factor γ(<1). Since the E-fields in the devices and wires remain constant, the device current and device and wire capacitance all scale as γ. Since the voltage also scales by γ, the energy of an operation scales as γ³. The delay of each gate also improves by γ. Since the delay is roughly \( t_d = \frac{c v}{i} \). The energy delay product decreases by γ⁴.

The difficulty with ideal scaling is the requirement for threshold voltage to scale along with the supply voltage. As mentioned earlier, static power caused by leakage current through the off transistors will limit the threshold voltage to be scaled.

### 3.2 Power reduction by sub threshold operation

Well known methods of low power design such as Voltage scaling, switching activity reduction, Architectural techniques of Pipelining and Parallelism may not be sufficient in many applications such as portable computing gadgets, Bio medical applications, where ultra low power consumption with medium frequency of operation is the primary requirement. Lot of research is carried out to investigate the ultra low
power (low speed) region of operation. One of the methods to attain ultra-low power is operating the transistors in sub-threshold region.

Origin of sub-threshold circuit design started with the measurement of current-voltage characteristics of p-channel MOS transistor by Vittoz E [40]. He identified the exponential dependency of drain current on the gate voltage at low current region. The region where the current is exponentially related to gate voltage is named as weak inversion region or sub-threshold region. This sub-threshold current is the leakage current.

Barron M.B [41] considered that the sub-threshold current was exponentially dependent on surface potential. Up to 1990’s sub-threshold digital circuits were totally ignored. Ultra low power design became popular from 1990 with the increase of portable electronic devices.

Bipul C Paul [42] focused on sub-threshold digital CMOS carry save array multiplier, which can operate excellently even if the supply voltage (0.47V) is far below the threshold voltage (0.67V) of NMOS transistor. The power delay product of the multiplier is about 25 times better than its strong inversion operation.

In the article “Digital CMOS logic operation in the sub-threshold region” Soeleman H [43] analyzed both CMOS and pseudo NMOS logic circuits operating in sub-threshold region, and showed that there is two orders of magnitude reduction in power, when a 8 x 8 Carry Save Array multiplier is operated in sub-threshold compared to strong inversion region. He concluded that sub-threshold circuits are used where ultra-low power is the primary requirement and performance is secondary.
Ultra low powered DLMS Adaptive filter for hearing aid applications, was proposed by Chris Hyung-II Kim[44]. He used parallel architecture with pseudo-NMOS logic style. Pseudo NMOS logic operating in the sub-threshold region provides better power delay product, when compared to CMOS. Simulation results showed that 91% power efficiency can be achieved with this logic style compared to non parallel CMOS implementation.

Vahid Moaleni[45], in his paper investigated 1 bit full adder cells in sub 100nm technology. The analysis is done using different full adder cells and the study on power, delay and power delay product of the cells is made.

Bipul C. Paul [46] proposed an optimized transistor structure for digital sub-threshold operation. The optimized sub-threshold devices showed more than 50% improvement in power delay product.

Farshad Moradi[47], in his article, 1 bit sub threshold full adders in 65 nm CMOS technology, proposed a 1 bit sub-threshold full adder based on modified XOR gates. The supply voltage is considered to be less than 0.3v and frequency response and power dissipation is studied.

Jaydeep P.Kulkarni[48] proposed a novel schematic trigger (ST) based differential 10- transistor SRAM bit cell suitable for sub threshold operation. The proposed memory bit cell operates at a lower (175 mv) supply voltage with 18 % reduction in read/ write power compared to conventional 6T cell.

Keshavrzi.A [49] discussed the main sources of leakage current i.e threshold voltage, channel physical dimension, channel and surface
doping profiles, drain and source junction depths, gate oxide thickness and supply voltage. He not only made a study of leakage current components, he made a thorough analysis as how to control the leakage current to improve the operation of the circuit.

Yang.S and Wolf.W [50] demonstrated an accurate and efficient stacking effect macro-model for leakage power in sub -100 nm circuits. Analysis on the effects of transistor stacking on gate leakage between the channel and gate and between drain and source and the gate is made in this article.

Melek.L.A.P, Schneider.M.C and C. Galup-Montoro,[51]have made the performance analysis of Conventional CMOS Inverter, NAND -2 and NOR static logic gates operating in sub-threshold region. The dependence of the drain currents on the process parameters can give rise to drive currents of NMOS and PMOS transistors that differ by an order of magnitude or even more. To compensate for this difference in currents, they proposed three bias circuits in single-well processes that adjust the body voltage. A test chip was fabricated in both AMIS 1.5 \( \mu \)m and TSMC 0.35 \( \mu \)m to further validate the proposal.

Burr.J.B and Peterson.A.M [52] have narrated that systems which are energy efficient can be designed by sub threshold CMOS circuits. Wang.A and Chandrakasan.A.P [53] analyzed the energy dissipation and performance of 0.18 \( \mu \)m CMOS circuits with supply voltages ranging from 0.1V to 0.6V and threshold voltage varying from 0 to 0.6V. They showed that sub threshold circuits can be used in low performance applications and applied the work to build adders and multiplier circuits. Parameter
sensitivity analysis of threshold voltage and temperature variation is also done in the article.

Paul.B.C and Roychowdhary.A [54] concluded that sub-threshold CMOS circuits, can provide excellent power reduction over strong inversion CMOS circuits. They designed devices which are suitable for sub threshold operation. Results indicate that the optimized device improves the speed and power delay product (PDP) of an inverter chain by 44% and 51%, respectively, over the normal super-threshold device operated in the sub threshold region.

Kim .C.H [55] presented a sub threshold delayed least mean square (DLMS) adaptive filter for hearing aid applications. He employed parallel architecture with pseudo NMOS logic style. Sub threshold pseudo NMOS logic provides improved power delay product compared to sub threshold CMOS logic. DLMS adaptive filter results in 91% power improvement compared to a non parallel CMOS implementation and can operate at 22kHz using a 400mV supply voltage.

Wang.A and Chandrakasan.A[56] demonstrated a 180mV FFT sub threshold Processor. A 256kb sub-threshold SRAM in 65nm CMOS is proposed by Calhoun.B.H and Chandrakasan.A.P [57]. They said that standard 6T approach limited to ~0.6-0.7V and 16 cells per bit line and 10T bit cell approach contain good overall energy and power savings.

Benton Highsmith Calhoun [58] reported that sub threshold leakage currents increases considerably with process scaling in CMOS
Low power consumption has become an important design concern as device sizes decrease and many more devices fit on a single chip. Since switching power is proportional to $C_L V_{dd}^2$, where $C_L$ refers to load capacitance and $V_{dd}$ refers to supply voltage. For maintaining performance, the threshold voltage needs to be reduced along with supply voltage scaling. This threshold voltage reduction results in problematic increase of sub threshold leakage currents.

Ming Liu[59] designed a low power wireless BCI system. The system is composed of an electrode, a stimulator, antennas and an Integrated circuit including a preamplifier, an analog to digital connector, a current mode digital to analog converter, a transceiver and a micro control unit. The system is a closed loop which can detect and record Electron cephalogram signals and send the signals to computer wirelessly and generate stimulating signals according to an analysis results from the computer. In this case sub threshold circuit technology is used to realize ultra low power micro control unit.

Abdul Karim[60], in his article presented a new low power multiplexer-based 1-bit full adder with 12 transistors. Simulation results show that the proposed design consumes 26% less power than conventional 28 transistor CMOS adder. In addition to charging, recycling capability and reduced transition activity, this circuit has no direct connections to power supply nodes and the entire signal gates are directly stimulated by the fresh input signals, leading to noticeable reduction in short -current power consumption. This new MBA-12T
adder thereby, is a good primitive cell to build larger low power VLSI systems.

### 3.2.1 Body biasing techniques

The Body biasing technique is an approach used for obtaining low power and high speed. In this technique, the threshold voltage of the device is varied in accordance with body bias voltage. By varying the threshold voltage, high speed and low power can be achieved. Various Body biasing techniques like Swapped Body Biasing technique, Dynamic Threshold MOS technique, Multiple Threshold CMOS technique, Dual Threshold techniques etc have been discussed in this section.

#### 3.2.1.1 Swapped Body Biasing technique

Narendra.S [61] proposed a Swapped Body Biasing technique where PMOS substrate is connected to ground and NMOS substrate is connected to supply. It is a fixed body biasing where body of each transistor is connected to some fixed potential. Because of this reason there is no dynamic threshold voltage control. The delay is going to reduce and power consumption is going to increase, in both ON and OFF states of MOSFET'S. Main advantages of this approach are no additional circuitry is required and produces high speed when compared to both Traditional Body Biasing and DTMOS configuration. The disadvantage of this approach is that extra power consumption, when compared to both Traditional and DTMOS configuration.

#### 3.2.1.2 Dynamic threshold MOS Technique

Fariborz Assaderaghi[62] in his article proposed a dynamic threshold MOSFET(DTMOS). In DTMOS, the gate is connected to substrate and
when transistor is ON, the threshold voltage is reduced, causing high current drive than regular CMOS. Similarly when transistor is OFF, the threshold voltage is raised causing reduction in leakage current and power. Assaderaghi[63] discussed about dynamic threshold MOSFET which is suitable for ultra-low voltage (0.6 V and below) VLSI circuits. At $V_{gs} = 0$, the MOSFET can have a high threshold voltage and low leakage power. And at $V_{gs} = V_{dd}$, it can have low threshold voltage and high speed. This body biasing technique is useful because there is no need for overhead circuitry. This DTMOS technique is a good option for high speed ultra-low power applications.

Soeleman.H and Roy.K[64] in their article, proposed two different sub threshold logic families - Variable threshold voltage sub threshold CMOS (VT-sub-CMOS logic) and sub threshold dynamic threshold voltage MOS logic (Sub-DTMOS logic). VT-sub-CMOS logic uses an additional stabilization scheme for identifying change in transistor current due to temperature and process variations and provides appropriate substrate bias. But coming to sub-DTMOS logic, no additional stabilization circuitry is required and both logic families have comparable power consumption as regular sub threshold CMOS logic, with superior robustness and tolerance to process and temperature variations than that of regular sub threshold CMOS logic.

Ernst.T[65] compared the propagation delay time of ring oscillator realized by SOI (silicon on Insulator) NMOS devices in DTMOS configuration, with its body grounded and with its body floating and showed that devices in DTMOS configurations are of high speed. He also
compared the speed performance of DTMOS devices with its body
ground, and body floating for a supply voltage and he concluded that
DTMOS devices are best option for ultra low power sub-threshold
circuits.

Because of shrinking of transistor size and higher packing density of
chip, there is a considerable reduction in power dissipation. Kuroda.T[66] suggested power reduction as a solution, to improve the
lifetime of silicon based technologies. Kobayshi.T[67] concentrated on
power reduction with medium speed. He proposed a self-substrate bias
technique for reducing threshold voltage variations, to adjust the leakage
current of MOSFET. A test chip with self-substrate bias is fabricated.

Assaderghi.F[68] in his article made some proposals for improving
the design of DTMOS technique. Wet Jin, Philip C.H. Chan[69] proposed
a power dissipation model including switching, short–circuit and static
Power dissipation for SOI DTMOS Inverter.

Soleimani.S, Sammak.S[70] proposed a sub threshold improved
DTMOS Technique and evaluated the performance parameters. He
concluded that improved DTMOS technique provided good power
reduction, compared to other DTMOS techniques.

Kureshi A.K[71] in his paper presented a novel energy efficient
method of designing switches and routing interconnects inside FPGA
using dynamic threshold MOS (DTMOS), instead of traditional NMOS
pass transistor based switches and interconnects.

Simulation results at supply voltage of 0.9v and operating frequency
of 300MHZ, shows 23.33% improvement in power delay product of PSMSA
pass switch, and an average 32.83% improvement in power delay product of vertex-II interconnects.

Tanaka.T[72] presented an experimental study of the threshold voltage shift versus the drain voltage of SOI NMOS devices in DTMOS configuration and the inverse sub-threshold slope. He concluded that DTMOS devices have superior sub-threshold slope and smaller threshold voltage shift, and less short-channel effect, compared to the conventional one. The current driving capability and transconductance of DTMOS devices are increased compared to other conventional devices. But because of large gate capacitance due to body tied to gate configuration, the advantage of transconductance has not much effect.

Chung.I.Y[73] proposed a DTMOS Inverter circuit using auxiliary transistors, for extending the power supply voltage beyond 0.7 V. Lee.J.W[74] presented a detailed study of substrate control techniques such as (a) The conventional SOI NMOS devices with substrate connected to ground and (b) The conventional SOI DTMOS device with substrate connected to gate. (c) The SOI DTMOS device with an NMOS auxiliary device sharing gate and drain to control its substrate. (d) The DTMOS device with an NMOS auxiliary device for its drain and gate connected to the gate of main device to control its gate. The DTMOS technique has fascinated so many investigators due to its low power consumption and high performance.

Abhisek dixit and Ramgopal Rao.V[75] in their work proposed a new DTMOS implementation using electrically induced junction MOSFET. The EJ-MOSFET overcomes the speed reduction, due to increased
concentration in the gate tied to body implementation of DTMOS. The simulation results shows that EJ_MOSFET have moderate improvement in dc characteristics and superior transient characteristics compared to DTMOS circuit.

Martin.S.M[76] in his article pointed out that as supply voltage is scaled, the dynamic power consumption can be reduced. But this in turn reduces the current drive capability and speed. Hence the threshold voltage and gate oxide thickness also to be reduced accordingly. But this causes an exponential increase in leakage current. Hence he concluded that 20% of total power constitutes leakage power in modern scaled CMOS technologies.

Keshavarji[77], in his article proposed reverse body biasing to reduce leakage power during standby mode by increasing the threshold voltage.

Scott Hanson[78], in his study proposed the design of a sub threshold processor for use in ultra-low-energy sensor systems. He described an 8 bit processor fabricated in a 0.13µm technology that consumes only 3.5 PJ/ instruction at $V_{dd} = 350$mv. He used body biasing technique to minimize process and temperature induced variations. He also investigated global and local techniques for performance improvement at low voltages.

Jabulani Nyathi [79] in his article, analyzed different logic circuit families operating in the sub threshold region. He compared different body biasing schemes such as Swapped body biasing, Tunable body biasing and DTMOS with traditional CMOS in terms of performance metrics like power and speed.
Wei Jin and Philip Chan, C.H[80] compared 4 types of SOI MOSFETS 
(1) Fully depleted (2) Non-Fully depleted (3) Dynamic threshold (4) 
Double gate in terms of power dissipation, delay and power – delay 
products and concluded that double gate MOSFET is superior when 
compared to other types of SOI MOSFET's for low-power applications.

Srivastava.A [81] in his article, showed that Forward Body Bias (FBB) 
technique can be used in digital applications. However the FBB method 
has a drawback. When transistor turned off, the leakage current 
increases due to electrically reduced threshold voltage. The leakage 
current increases rapidly with the reduction of threshold voltage. With 
increasing forward body bias, the leakage current increases significantly. 
The leakage current can be reduced using a dynamic body bias technique 
called DTMOS technique.

Improved DTMOS inverter design is proposed by Zhang.C [82] for 
design of ultra low power CMOS operational amplifier. The drawback of 
conventional DTMOS inverter is limited to its operation below 0.6v. 
Higher supply voltage will cause the forward body bias greater than 0.6v, 
and then turn on the p-n junction between source and substrate. This 
drawback can be rectified in improved DTMOS technique by using two 
level shift transistors. The voltages applied to substrates are limited by 
these transistors. Brent C Bero[83] in his work proposed a Tunable Body 
biasing technique which enables ultra low power or high speed operation, 
depending on the supply voltage of the circuit.
3.2.1.3 MTCMOS Technique

Mutoh.S et.al [84] proposed Multi threshold CMOS devices (MTCMOS) for leakage power reduction. MTCMOS technique employs high threshold voltage power switches for leakage current reduction during OFF mode. In this technique, when high threshold voltage transistors are ON, the low threshold voltage logic gates are connected to power and virtual ground, and switching is done through fast devices. When the circuit is in OFF mode, the high threshold voltage transistors are switched off, causing a very low sub threshold leakage current from supply voltage to ground. MTCMOS technique, effectively reduce standby leakage currents and is more suitable in burst mode type applications. Compared to PMOS devices, NMOS sleep transistors are more effective because of lower on resistances and they can be made smaller for the same current drive. The main drawback of this technique is the dependence of performance on sleep device sizing. Increasing the sleep transistor size, would cause an increase in circuit capacitance and power dissipation, while reducing the size would result in a supply current limitation and speed degradation. A methodology for properly sizing the sleep device to minimize the delay based on mutual exclusive discharge patterns was proposed by Kao J.T[85].

Douseki.T[86] developed a MTCMOS circuit using SIMOX Technology. In this case a fully depleted low-threshold CMOS logic gates and a partially depleted high-threshold power-switch transistors are combined to provide low-power operation in the sleep mode and high speed operation in the active mode at a low supply voltage below 0.5 V. A 16
bit ALU at 0.5v supply voltage and 40 Mhz frequency is designed and fabricated using 0.25 micrometer MTCMOS/SIMOX technology.

Kawaguchi.H [87] said that high threshold voltage and low leakage current is possible during standby mode, by reverse biasing the sleep transistors to more than supply voltage. The low threshold sleep device provides more current drive during the active mode and is desirable in order to achieve more speed. By increasing the voltage swing of the gate of the sleep transistor, the gate to source voltage (Vgs) becomes greater than zero and boosts the current drive.

Dong whee kim [88], in his article describes a low-power carry look ahead adder with MTCMOS technology. Comparing with conventional CMOS circuit, the circuit achieved reduced power consumption by 14.7% and power delay product by 16.11%.

Shin Ichiro Muto [89], in his article proposed a 1-v power supply, high speed low power digital circuit technology with 0.5µm multi threshold voltage CMOS. This technology have both low threshold voltage and high threshold voltage MOSFETS in a single list. The low threshold voltage MOSFET'S improves speed performance at a low supply voltage of 1v or less while the high threshold voltage MOSFET'S suppress the standby leakage current during the sleep period.

Kawaguchi.H[90], in his article pointed out that high threshold voltage PMOS sleep devices can be used, so that body terminals can be tied to virtual supply instead of actual power supply which may simplify the logic structures, because libraries PMOS cells may not need to be modified.
Stan.M[91], in his work mentioned that it is important for sleep transistors to have a high enough conductance during the active mode because the series resistance act to degrade performance. One simple way to improve the conductance of the sleep device in the active mode is to over drive the gate voltage. (ie. above supply voltage for NMOS device) and similarly the leakage reduction can be improved by under driving the gate (ie. below ground for NMOS device) during standby mode. Cutting off leakage current by under driving the gate is actually more useful for low threshold voltage sleep devices although reliability issue may become a concern.


Many researchers have proposed MTCMOS sequential circuits that can preserve state during standby mode. Mutoh.S[93] proposed parallel high threshold voltage CMOS Inverters, to provide a static recirculation path during standby mode. This is one of the first and straight forward method of preserving the state.

Shigematsu.S [94] described another MTCMOS sequential circuit, called “balloon” circuits that hold state during the idle mode. This approach uses autonomous balloon circuit that is used to write in stored data during off state and can be read out during active mode. These balloon circuits take up less area, because they simply hold data and don’t need to be fast. The other advantage is that all MTCMOS gates can share common virtual supply and virtual ground lines.
Because of control and area costs of previous sequential circuits much research has been done to search for different solution. Akamatsu.H[95] used an attractive periodic refresh mechanism to hold state, but suffers from extra overhead and potential noise issues. The other methods of state retention in MTCMOS blocks that are previously proposed by Kumagai.K[96] and Makino.H [97] used the approach in which MTCMOS structure is modified with diode devices such that during the sleep mode, internal nodes do not float. As a result logic gates continue to operate on a reduced voltage scaling and leakage currents are still reduced.

In order to increase the speed of operation of normal Silicon on insulator (SOI) MTCMOS circuits, logic gates are realized with low threshold fully depleted (FD) device. The main drawback in this method is leakage currents increases during active mode of operation. Hence FujI1.K[98] proposed a triple –threshold SOI CMOS circuit scheme. In this case a power-switch transistor made of a high threshold PDSOI device is used as in the case of MTCMOS technique. But the logic gates are realized using both low and medium threshold FDSOI CMOS devices. Low-threshold FD devices are used for implementing the logic gates along the critical path. The threshold voltages of medium and low- threshold FD devices are chosen in such a way that during active mode, leakage current and power consumption are reduced without affecting the operating speed.

Von Arnim[99], in his paper estimated the effectiveness of body biasing techniques for performance improvement and leakage reduction
in a 90nm CMOS low-power technology with triple-well option. He presented static measurements of single devices and dynamic measurements of ring oscillators. The experimental results show that in 90nm CMOS circuits, the efficiency of body biasing strongly depends on the device type and operating temperature of the device.

Sameh Andrawes[100], in his article focused on the design of sub-threshold multi-threshold low power shift register, using 90nm CMOS technology. The design and simulation of the circuit is done using Cadence tools. This technique attain high performance during active mode and low power consumption during standby mode.

Liu.X and Mourad.S [101] studied the effect of substrate bias on performance of sub-threshold circuits. He evaluated two types of body bias (1) Forward Body Bias and (2) Reverse Body Bias. Reverse Body Bias, reduces the off-state leakage current and hence standby power. Forward Body Bias improves current drive and causes significant raise in power dissipation. Hence Forward Body Bias is applied in circuits where performance is the main criteria. DTMOS and Swapped Body Bias techniques used Forward Body Bias to increase the speed of the circuit.

To improve performance at low supply voltage, Dongwook.S[102] used partially depleted SOI(PDSOI). A PDSOI MOSFET contains floating body circuit topologies which are susceptible to parasitic bipolar effect. In some circuits, the parasitic bipolar effect results in additional power consumption and the noise margin degradation. Kao.J and Chandrakasan.A[103] incorporated both high threshold and low threshold MOSFETS in a single circuit. Because of variable threshold,
high performance operation in active mode and low power in idle mode are possible. The circuits can be operated in active mode or in sleep mode. In sleep mode, high threshold voltage MOSFETS limit leakage current and in active mode, low threshold MOSFETS improve current drive.

Moisiadis.Y [104] applied a technique called substrate back-biasing, to increase the threshold of the devices, during the off state. The technique provides a good reduction in leakage current and is applied for a range of possible supply voltages.

### 3.2.1.4 Switched source impedance Technique

Horiguchi .M[105] proposed a method for reducing leakage current, by decreasing gate to source voltage in standby mode by raising the source voltage through switched source impedance CMOS. In this approach, passive resistor is switched in between a gate’s source nodes and ground during standby mode. During active mode, the resistor is shorted out so that there is no additional delay penalty. In practice, switched source impedance circuits are rare because the resistor must be large.

### 3.2.1.5 Transistor stacking

Narendra etal[106] examined the effect of transistor stacking on subthreshold leakage current reduction. The stack effect can reduce leakage current by two orders of magnitude for low threshold devices and three orders of magnitude for high threshold devices.

James Kao .T [107] in his article presented several dual threshold voltage techniques for reducing standby power dissipation, while still
maintaining high performance in static and dynamic combinational logic blocks.

Liqiong wei [108] in his work used Dual Threshold Technique to reduce leakage power by assigning high threshold voltage to some transistors in non-critical paths and using low threshold transistors in critical path.

3.2.1.6 Variable threshold CMOS technique

Kuroda et al.[109] proposed a variable threshold CMOS technique which employs all low threshold devices. However the threshold voltage is controlled using the substrate bias of the devices in a triple well CMOS process. During the active mode, the threshold voltage is decreased and during the off mode the threshold voltage is raised. The problem with the approach is that the threshold voltage varies as the square root of body source voltage. Therefore the body-source has to considerably increase to change the threshold voltage to a reasonably higher value.

Inukai.T[110] reported that variable threshold CMOS is very effective in suppressing leakage current for series connected transistors due to the increased body effect. Keshavarzi.A [111] discussed that variable threshold CMOS scheme depends on a high body effect to control the threshold voltage with technology scaling. The body effect is primarily reduced due to the short channel effects. Techniques such as substrate doping can be applied to enhance the short channel effects. However well doping causes the doping levels in the vicinity of source body and drain body junctions to increase significantly. As the doping limit approaches the tunneling limit, the junction current increases exponentially and
become the dominant leakage component. Body effect is reduced and
limits the effectiveness of variable threshold CMOS scheme.

Yang et al.[112] in his work used SOI technology for the
implementation of variable threshold CMOS. He used a silicon-on-
insulator with active substrate to dynamically control the threshold
voltages.

Kobayashi.T[113] and Kuroda.T[114], in their articles specified that
the main benefit of body biasing is that the threshold voltage can be
dynamically controlled during runtime, instead of just switching between
the no body bias or maximum reverse body bias. It is more useful to be
able to selectively chosen a body bias value that can be used to actually
fine tune threshold voltages to meet performance and leakage
specification. Bowman[115] in his article showed that as technology
scales, the short channel effects worsens and this causes an increase in
variation in threshold voltage.

Narendra.S[116] proposed a new design using forward body biasing to
achieve better current drive with less short channel effects. High
threshold voltage transistor with reduced leakage current is used in
standby mode, and low threshold voltage transistor is employed to
achieve high performance in active mode. Both high channel doping and
forward body bias reduce short channel effect relaxing the scalability
limit of channel length due to threshold voltage roll off and drain induced
barrier lowering. This results in higher on current compared to low
threshold voltage design for same off current case, improving
performance. Reverse body bias can also be applied in standby mode
together with forward body bias to further reduce leakage current.

3.2.1.7 Dynamic threshold voltage scaling

Kim.C.H [117] came out with Dynamic Threshold Voltage Scaling
(DVTS) scheme which employs substrate biasing to adjust threshold
voltage based on the performance demand. This technique uses same
concept of variable threshold CMOS (VTCMOS), but the threshold voltage
is varied based on system performance requirement. When high
performance is necessary, the lowest threshold voltage is obtained
through zero body bias and when performance demand is low, threshold
voltage is raised through Reverse Body Bias. In cases when there is no
workload at all, the threshold voltage can be increased to its upper limit
to significantly reduce the standby leakage power. This scheme delivers
just enough throughput for current workload by tracking the optimal
supply voltage. It considerably reduces leakage power by intermittently
lowering down the circuit.

3.2.1.8 Dual threshold CMOS technique

WEI.L[118] proposed dual threshold technique to reduce the leakage
power in low-voltage, low power and high performance applications. In
this technique he applied a high threshold voltage to some transistors in
non critical paths, and used low threshold transistors in critical paths.
High threshold voltage transistors suppress the sub threshold current,
while low threshold voltage transistors are used to achieve high
performance. The dual threshold CMOS technique has the same critical
delay as the single low threshold CMOS circuits, while leakage power is
saving in non critical paths. No additional control circuitry is required and both high performance and low leakage power can be achieved simultaneously. Many researchers have proposed many other design techniques based on Dual Threshold CMOS. Upsizing a high threshold voltage transistor is a method to improve performance. But it can cause area penalty according to Pant.P [119].

3.3 Conclusions

Various approaches have been discussed in the present chapter to reduce the power dissipation. Well known methods of low power design such as voltage scaling, switching activity reduction, architecture techniques of pipelining which were discussed above may not be sufficient in portable applications, where ultra low power with medium frequency of operation is the main requirement. One of the techniques to achieve ultra low power is by operating the devices in sub threshold region. Lot of research has been taken place in the area of sub threshold operation. But the main drawback of sub threshold circuits is low speed. In order to increase the speed of the sub threshold circuits, some body biasing techniques were discussed.

One of the body biasing techniques to increase the speed of sub threshold circuits is fixed body biasing technique. The main problem with this technique is that the threshold voltage is decreased both in OFF mode and ON mode causing increase in leakage current even in OFF state. Hence some variable threshold techniques are proposed by some investigators. In this case the body biasing can be varied by reducing the threshold voltage in the active mode and increasing the threshold voltage
in standby mode. They need additional stabilization techniques to provide appropriate body bias. Another approach is multi threshold voltage CMOS. This technology has both low threshold voltage and high threshold voltage MOSFETs. The main drawback of this type of technique is that they produce complex architectures and occupy large chip area. Hence a simple technique called DTMOS approach is suggested by some researchers, where the substrate is connected to gate and body bias varies with gate voltage. When the gate voltage is high (ON condition), the forward body bias is applied causing reduction in threshold voltage and providing large driving current which is better than that in sub threshold CMOS circuits. Hence this can be used in high speed applications and when it is in OFF mode, the threshold voltage increases which results in low leakage current.

In order to reduce the leakage current of DTMOS further in OFF mode, a novel technique called Variable threshold MOSFET (VTMOS) technique is proposed in this thesis. This approach is investigated in the next few chapters, for realizing the basic logic gates and complex digital systems. It has been clearly shown that there is significant reduction in power dissipation up to 54 percent. These investigations form the contents of this thesis.