ABSTRACT

In modern communication systems, it needs noise free signal processing with reduced cost. Particularly in portable mobile systems, such things become essential. Even though Digital signal processing based architectures fulfill this, it suffers from speed limitation. Specific filtering architecture is needed with reduced scaling technology. Wiener filter is one of the most attractive filters for noise removal in speech enhancement operations because of its straightforward design. One key problem associated with Wiener filter is iteration issues. In order to remove iteration issues, highly complicated units are needed. Hence there is a need for area and power efficient FPGA (Field Programmable Gate Array) based VLSI (Very Large Scale Integration) architecture for Wiener filter without degrading in performance.

In this work, an efficient Wiener filter architecture for noise degradation system is proposed. The proposed reconfigurable architecture is based on the modified CORDIC (COordinate Rotational DIgital Computer) based FFT (Fast Fourier Transform) /IFFT (Inverse Fast Fourier Transform) processor with an efficient addressing scheme is adopted to reduce area utilization. Also a temporal cache memory is adapted to acquire hardware and power efficiency with optimized speed in QR decomposed matrix inversion of Wiener filter architecture. The division operation is replaced by a productive inverse and multiplication process in proposed design to reduce complexity. Pipelined operation is used here to effectively enhance the operation of the Wiener filter architecture for noise degradation system. In this work, modified CORDIC architecture is named as memory less rotational CORDIC.

CORDIC (CO-ordinate Rotational DIgital Computer) is an iterative algorithm for fast implementation of trigonometric functions, multiplications
with reduced hardware along with good speed. In this work, Radix-4 CORDIC architecture is modified as completely eliminating the ‘Z’ path by precompiling the direction of micro-rotations along with memory less logic to store rotation angles in rotation mode. Proposed CORDIC architecture is elaborated in terms of hardware complexity, iteration delay and memory reduction. Results are compared with other available radix-2 and radix-4 CORDIC architectures. The whole Radix-4 CORDIC architecture is coded in Verilog HDL for 16 bit precision, synthesized and implemented in Xilinx tool with available FPGA devices for thorough comparison with existing techniques. Almost in various FPGA synthesis/implementation, results show that improvement in hardware resources utilization, speed and power with little hardware overhead.

In this work, as the key idea of area and power saving technique with optimized speed in FFT operation, butterfly unit is replaced with modified Radix-4 CORDIC for twiddle factor operation. Efficient addressing scheme is effectively used to reduce dynamic power consumption. The whole FFT architecture is coded in Verilog HDL for 16 bit precision of different length FFT’s, synthesized and implemented in Xilinx tool with available FPGA devices for enough comparison with available conventional Radix-2 and Radix-4 CORDIC based FFT architectures. Results show that latency, power and hardware improvement with little hardware overhead.

An effective wiener filter for noise suppression combined with modified CORDIC based FFT/IFFT processor were executed with greater speed. Iteration issues of conventional wiener filter is evacuated in this work. Matrix size is predefined as 32x32 for matrix inversion operation. The whole reconfigurable wiener filter structure is integrated and executed on Virtex 5 FPGA. Results show that considerable reduction in hardware resources utilization by adjusting with proposed technique without any degradation in signal performance in terms of SNR and PSNR. The proposed wiener filter architecture exhibits greater performance with reduced complexity.