CHAPTER 2

MODULATION TECHNIQUES

2.1 INTRODUCTION

The sinusoidal shaped waveforms with more than two-level contains less voltage harmonic in the load. However, the performance improvement of the voltage harmonic depends on the control technique. In this chapter, the theoretical analysis of pulse width modulation techniques such as synchronous sequential circuits based PWM and Alternatively in Opposition (APO) disposition PWM used for the research work are discussed.

2.2 SYNCHRONOUS SEQUENTIAL CIRCUIT BASED PWM

Almost all power electronic converters are operated in the switching mode. The switches in the multilevel inverters are always turned either ON or OFF. The flow of power in the multilevel inverter is controlled by changing the switches between these two states, and the required switching pulses are designed by using a synchronous sequential circuit. The synchronous sequential circuit has been developed for seven-level multilevel inverter. The level of voltage is decided by the switching pulses of the synchronous sequential circuit. The synchronous sequential circuits based multilevel inverters offer several advantages like simple control of circuitry-level, ease of formulation, etc.
2.2.1 Designing of Synchronous Sequential Circuit

The design procedure of synchronous sequential circuit is followed in step by step manner [Morris MM]. The synchronous sequential circuits based PWM is focusing on the seven-level output voltage, the level of voltage converted to equivalent binary numbers which are as shown in Figure 2.1. Either half of the voltage waveform (positive or negative waveform) is considered for designing of synchronous sequential because a sinusoidal waveform is symmetrical waveform. The equivalent decimal numbers of phase voltages are 0, 12, 14, 15, 6, and 4. P₁, P₂, P₃ are the switching pulses of the inverter and ASP is the auxiliary switching pulse.

![Figure 2.1 Seven-level voltage to binary conversion](image)

The state diagram has been drawn from the equivalent decimal numbers as shown in Figure 2.2. The state diagram provides another useful information when the state of the entities in the system will change in response to events. The next state of the state variables is assigned as the order of equivalent binary of phase voltage. This state diagram is acting as a ring counter.
From the state diagram, the state table is developed and binary values are assigned to each state in the state table. The JK flip-flops are used for designing the synchronous sequential circuits. The JK flip flop excitation table is shown in Table 2.1 and the state table of the synchronous sequential circuit is shown in Table 2.2. Present state and next state of state table have been derived from state diagram. The state table contains the flip-flop inputs of $J_A$, $K_A$, $J_B$, $K_B$, $J_C$, $K_C$ and $J_D$, $K_D$ respectively, the value of binary numbers are denoted based on the present state and the next state of JK flip flop excitation table.

### Table 2.1 Excitation table of JK flip flop

<table>
<thead>
<tr>
<th>$Q_n$</th>
<th>$Q_{n+1}$</th>
<th>$J$</th>
<th>$K$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>×</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>×</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>×</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>×</td>
<td>0</td>
</tr>
</tbody>
</table>
Table 2.2 State table

<table>
<thead>
<tr>
<th>Decimal Number</th>
<th>Present State</th>
<th>Next State</th>
<th>Flip Flop</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$Q_A$</td>
<td>$Q_B$</td>
<td>$Q_C$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>14</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>15</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

The Boolean expression for the synchronous sequential circuit is determined from the state table which is shown in Table 2.2. The K-map method has been used to find the Boolean expression of the synchronous sequential circuit. The K-maps are constructed from Table 2.2, notice that the terms which are having output 1, the corresponding cells are marked in K-map as 1. Similarly, other cells are marked as zero and don’t care conditions as (×). The sum of product form of Boolean expression using K-map is shown in Table 2.3 to Table 2.10.
Table 2.3 K-map to find $J_A$

<table>
<thead>
<tr>
<th></th>
<th>$C'D'$</th>
<th>$C'D$</th>
<th>$CD$</th>
<th>$CD'$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A'B'$</td>
<td>1</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
</tr>
<tr>
<td>$A'B$</td>
<td>0</td>
<td>$\times$</td>
<td>$\times$</td>
<td>0</td>
</tr>
<tr>
<td>$AB$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
</tr>
<tr>
<td>$AB'$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
</tr>
</tbody>
</table>

$J_A = A'B'C'D'$

Table 2.4 K-map to find $K_A$

<table>
<thead>
<tr>
<th></th>
<th>$C'D'$</th>
<th>$C'D$</th>
<th>$CD$</th>
<th>$CD'$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A'B'$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
</tr>
<tr>
<td>$A'B$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
</tr>
<tr>
<td>$AB$</td>
<td>0</td>
<td>$\times$</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$AB'$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
</tr>
</tbody>
</table>

$K_A = ABCD$

Table 2.5 K-map to find $J_B$

<table>
<thead>
<tr>
<th></th>
<th>$C'D'$</th>
<th>$C'D$</th>
<th>$CD$</th>
<th>$CD'$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A'B'$</td>
<td>1</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
</tr>
<tr>
<td>$A'B$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
</tr>
<tr>
<td>$AB$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
</tr>
<tr>
<td>$AB'$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
<td>$\times$</td>
</tr>
</tbody>
</table>

$J_B = A'B'C'D'$
### Table 2.6 K-map to find $K_B$

<table>
<thead>
<tr>
<th></th>
<th>C’D’</th>
<th>C’D</th>
<th>CD</th>
<th>CD’</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A’B’$</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>×</td>
</tr>
<tr>
<td>$A’B$</td>
<td>1</td>
<td>×</td>
<td>×</td>
<td>0</td>
</tr>
<tr>
<td>$AB$</td>
<td>0</td>
<td>×</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$AB’$</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>×</td>
</tr>
</tbody>
</table>

$K_B = A’BC’D’$

### Table 2.7 K-map to find $J_C$

<table>
<thead>
<tr>
<th></th>
<th>C’D’</th>
<th>C’D</th>
<th>CD</th>
<th>CD’</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A’B’$</td>
<td>0</td>
<td>×</td>
<td>×</td>
<td>×</td>
</tr>
<tr>
<td>$A’B$</td>
<td>0</td>
<td>×</td>
<td>×</td>
<td>×</td>
</tr>
<tr>
<td>$AB$</td>
<td>1</td>
<td>×</td>
<td>×</td>
<td>×</td>
</tr>
<tr>
<td>$AB’$</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>×</td>
</tr>
</tbody>
</table>

$J_C = ABC’D’$

### Table 2.8 K-map to find $K_C$

<table>
<thead>
<tr>
<th></th>
<th>C’D’</th>
<th>C’D</th>
<th>CD</th>
<th>CD’</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A’B’$</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>×</td>
</tr>
<tr>
<td>$A’B$</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>1</td>
</tr>
<tr>
<td>$AB$</td>
<td>×</td>
<td>×</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$AB’$</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>×</td>
</tr>
</tbody>
</table>

$K_C = A’BCD’$
Table 2.9 K-map to find \( J_D \)

<table>
<thead>
<tr>
<th></th>
<th>( C'D' )</th>
<th>( C'D )</th>
<th>( CD )</th>
<th>( CD' )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A'B' )</td>
<td>0</td>
<td>( \times )</td>
<td>( \times )</td>
<td>( \times )</td>
</tr>
<tr>
<td>( A'B )</td>
<td>0</td>
<td>( \times )</td>
<td>( \times )</td>
<td>( 0 )</td>
</tr>
<tr>
<td>( AB )</td>
<td>0</td>
<td>( \times )</td>
<td>( \times )</td>
<td>( 1 )</td>
</tr>
<tr>
<td>( AB' )</td>
<td>( \times )</td>
<td>( \times )</td>
<td>( \times )</td>
<td>( \times )</td>
</tr>
</tbody>
</table>

\[ J_D = ABCD' \]

Table 2.10 K-map to find \( K_D \)

<table>
<thead>
<tr>
<th></th>
<th>( C'D' )</th>
<th>( C'D )</th>
<th>( CD )</th>
<th>( CD' )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A'B' )</td>
<td>( \times )</td>
<td>( \times )</td>
<td>( \times )</td>
<td>( \times )</td>
</tr>
<tr>
<td>( A'B )</td>
<td>( \times )</td>
<td>( \times )</td>
<td>( \times )</td>
<td>( \times )</td>
</tr>
<tr>
<td>( AB )</td>
<td>( \times )</td>
<td>( \times )</td>
<td>( 1 )</td>
<td>( \times )</td>
</tr>
<tr>
<td>( AB' )</td>
<td>( \times )</td>
<td>( \times )</td>
<td>( \times )</td>
<td>( \times )</td>
</tr>
</tbody>
</table>

\[ K_D = ABCD \]

From the developed K-Map (Table 2.3 to Table 2.10), Boolean expressions are determined as follows

\[ J_A = A'B'C'D' \]  \hspace{1cm} (2.1)  
\[ K_A = ABCD \]  \hspace{1cm} (2.2)  
\[ J_B = A'B'C'D' \]  \hspace{1cm} (2.3)  
\[ K_B = A'BC'D' \]  \hspace{1cm} (2.4)  
\[ J_C = ABC'D' \]  \hspace{1cm} (2.5)  
\[ K_C = A'BCD' \]  \hspace{1cm} (2.6)  
\[ J_D = ABCD' \]  \hspace{1cm} (2.7)  
\[ K_D = ABCD \]  \hspace{1cm} (2.8)
2.2.2 Execution of Synchronous Sequential Circuit

The logical circuit based on synchronous sequential circuit has been designed by the Boolean expression of Equations 2.1 to 2.8 and the resultant logic circuit is shown in Figure 2.3. The synchronous sequential circuit contains JK flip-flop (A, B, C, D), four input and single output AND gate. The flip-flop outputs are compliment function (high or low). Four-input AND gate are connected based on the derivation of K-map and the output of AND gate is connected to flip-flop input as per Figure 2.3. The clock pulse generator produces the sequence of square pulses, which decide the fundamental frequency of seven-level multilevel inverter. The frequency of clock pulse generator is 650Hz.

![Figure 2.3 Synchronous sequential circuit](image)

The synchronous sequential circuit produces the sequence of switching pulses, this sequence of pulses are used for both half cycles. The continuation of switching pulse is broken up in every half cycle by using breakup logic circuits and it is shown in Figure 2.4. The breakup logic circuit consists of a flip-flop and required clock pulse are taken from the output $Q_B$ of the flip-flop B.
The breakup logic circuit is designed from the possible switching state of the multilevel inverter. The following expressions are used for breaking the sequence of switching pulses.

\[
S_1 = D'E' \\
S_2 = C'E' \\
S_3 = B'E' \\
S_4 = D'E \\
S_5 = CE' \\
S_6 = BE'
\]  

(2.9) \hspace{2cm} (2.10) \hspace{2cm} (2.11) \hspace{2cm} (2.12) \hspace{2cm} (2.13) \hspace{2cm} (2.14)

Figure 2.4 Break up logic circuits
The synchronous sequential circuit provides the stepped sinusoidal waveform in the multilevel inverter and also improves the behavior of the inverter topology. The multilevel inverter fundamental frequency can be changed by changing the clock pulse of generator’s frequency.

This synchronous sequential circuit algorithm has been implemented to different topology and n-level of the multilevel inverter. It has been tested for five-level inverter topology and the same design procedure of synchronous sequential circuit algorithm provide logic and breakup logic circuit which are shown in Figures 2.5 and 2.6 respectively.

![Figure 2.5 Synchronous sequential logic circuit](image)

![Figure 2.6 Break up logic circuit](image)
2.3 APO DISPOSITION PWM

One of the most popular switching techniques for the multilevel inverter is Sinusoidal Pulse Width Modulation (SPWM) method. It has advantages like simplicity, good results in all the operating conditions etc. SPWM has categorized into open loop sinusoidal reference and closed loop sinusoidal reference by p-q theory. In this work, APO disposition PWM has been used to control the MLI.

2.3.1 APO Disposition PWM using Open Loop Sinusoidal Reference

The Alternatively in Opposition (APO) disposition PWM is one of the efficient methods in sinusoidal pulse width modulation technique. It contains four triangular signals ($A_c$) and keeping an open loop modulating sinusoidal signal ($A_r$). All the triangular waveforms are the same amplitude ($A_c$) and frequency ($\omega_c$). However, every triangular waveform is in opposite disposition as shown in Figure 2.7.

In APO disposition PWM, two triangular waveforms are placed in above the zero reference and other two triangular waveforms are placed below the zero reference. At every instant, each triangular waveform is compared with the modulating sinusoidal signal. At each comparison stage gives 1 or -1 based on the modulation sinusoidal signal and carrier waveform, if the modulation signal is greater than the carrier waveform which has produced the pulse, otherwise zero. APO disposition parameters give the gate control pulses to the switches for having different voltage levels in the output waveform.
The analytical expression of output voltage for an APO disposition PWM controlled single phase multilevel inverter has been derived by using Fourier series modulation model method. The expression of output voltage at under modulation (M <1) is given as follows:

\[
v(t) = M \left( \frac{N-1}{2} \right) E \sin(\omega_m t + \phi) + \frac{(N-1)E}{\pi} \sum_{n=3, odd}^{\infty} \left\{ M \left[ \frac{\sin(\frac{\pi}{2}) - \sin(\frac{\pi}{2} + \frac{n}{n+1})}{n-1} \right] \right. \\
\left. + \frac{2}{n} \cos \left( \frac{n \pi}{2} \right) \right\} J_n \left[ m M \left( \frac{N-1}{2} \right) \right] \frac{\pi}{2} \\
\cdot \sin(n \omega_m t + n \phi) + \frac{4E}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} \sum_{n=1}^{\infty} \left[ J_h \left[ m M \left( \frac{N-1}{2} \right) \right] \frac{1}{n+h} \cdot \sin \left( \frac{(n+h) \pi}{2} \right) \right] \\
\cdot \sin(m \omega_c t + n \omega_m t + n \phi) \right.
\]

\[ (2.15) \]
Simplifying the Equation (2.15), final expression of output voltage as

\[ v(t) = M \frac{(N - 1)E}{2} \sin(\omega_n t + \phi) \]

\[ + \frac{4E}{\pi^2} \sum_{m=1}^{\infty} \frac{1}{m} \sum_{n=-\infty}^{\infty} J_n \left( mM \left( \frac{N - 1}{2} \right) \pi \right) \frac{\pi}{2} \]

\[ - \sum_{h=\text{odd}} \sin \left( \frac{(n + h)\pi}{2} \right) \sin(m\omega t + n\omega_n t + n\phi) \]

\[ . \sin(m\omega t + n\omega_n t + n\phi) \]

(2.16)

The expression of output voltage for overmodulation \( (M > 1) \) is given as

\[ v(t) = \frac{(N - 1)E}{2\pi} \left\{ M \left[ 2 \arcsin \left( \frac{1}{M} \right) - \sin \left( \arcsin \left( \frac{1}{M} \right) \right) \right] \right\} \sin(\omega_n t + \phi) \]

\[ + 4 \cos \left[ \arcsin \left( \frac{1}{M} \right) \right] \left\{ \left[ \sin(n - 1) \arcsin \left( \frac{1}{M} \right) \right] \right\} \sin(n\omega_n t + n\phi) \]

\[ + \frac{(N - 1)E}{2\pi} \sum_{n=3,\text{odd}}^{\infty} \left( 1 - (-1)^n \right) \left\{ \left[ \frac{\sin(n - 1) \arcsin \left( \frac{1}{M} \right)}{n - 1} \right] \right\} \sin(n\omega_n t + n\phi) \]

\[ \left\{ J_n \left[ mM \left( N - 1 \right) \frac{\pi}{2} \right] \left[ 1 - (-1)^n \right] \right\} \]

\[ + \frac{2E}{\pi^2} \sum_{m=1}^{\infty} \frac{1}{m} \sum_{n=-\infty}^{\infty} \left\{ \frac{1}{n + h} \sum_{k=1}^{(n-1)} \cos \left[ m(k - 1)\pi \right] \left[ x_{k+1} - x_k \right] \right\} \]

\[ - \sum_{h=\text{odd}} \left\{ J_n \left[ mM \left( N - 1 \right) \frac{\pi}{2} \right] \left[ 1 - (-1)^{n+1} \right] \right\} \]

\[ \left\{ \sum_{k=1}^{(n-1)} \cos \left[ m(k - 1)\pi \right] \left[ \sin \left[ (n + h)x_{k+1} \right] \right] \right\} \]

\[ \left\{ \sin \left[ (n + h)x_k \right] \right\} \]

\[ . \sin(m\omega t + n\omega_n t + n\phi) \]

(2.17)
The expression of output voltage equation given in equation (2.17) is used for determining the multilevel inverter topology output terminal voltage with respect to various modulation indexes.

### 2.3.2 APO Disposition PWM using Closed Loop Sinusoidal Reference

A p-q theory has been implemented for closed loop sinusoidal reference control strategy. The control strategy of the p-q theory is based on Clarke’s theory of \( \alpha \beta 0 \) transformation. According to this theory, a single phase system can be defined as a pseudo two-phase system by giving \( \pi/2 \) lead or \( \pi/2 \) lag, which is each phase voltage and current of the original three-phase systems. This resultant two-phase system can be represented in \( \alpha - \beta \) coordinates, thus, the active and reactive currents are calculated from these \( \alpha - \beta \) components and are applied as a reference signal for APO Disposition PWM. The p-q control is based on the \( \alpha \beta 0 \) transformation, which consists of a real matrix to transform three-phase voltages and currents into the \( \alpha \beta 0 \) stationary reference frame. The Clarke’s Transform of phase voltages to \( \alpha \) and \( \beta \) coordinates is in the form given below

\[
\begin{bmatrix}
V_{\alpha} \\
V_{\beta}
\end{bmatrix}
= \sqrt{\frac{2}{3}}
\begin{bmatrix}
1 & -1 & -1 \\
\frac{2}{\sqrt{3}} & \frac{2}{2} & -\frac{\sqrt{3}}{2}
\end{bmatrix}
\begin{bmatrix}
V_{a} \\
V_{b} \\
V_{c}
\end{bmatrix}
\]  

(2.18)

It is assumed that line voltages \( (V_a, V_b, V_c) \) are referenced to an artificial zero, i.e., \( V_a + V_b + V_c = 0 \). At such a condition, the Clarke’s Transform of phase voltages can be simplified Equation (2.19).

\[
\begin{bmatrix}
V_{\alpha} \\
V_{\beta}
\end{bmatrix}
= \begin{bmatrix}
\frac{\sqrt{3}}{2} & 0 \\
\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}}
\end{bmatrix}
\begin{bmatrix}
V_{a} \\
V_{b}
\end{bmatrix}
\]  

(2.19)
Similarly, in three-wire systems \( I_a + I_b + I_c = 0 \), thus, the Clarke’s Transform of the line currents has the form of the Equation (2.20).

\[
\begin{bmatrix}
  I_a \\
  I_\beta
\end{bmatrix} = \begin{bmatrix}
  \frac{\sqrt{3}}{2} & 0 \\
  \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \sqrt{2}
\end{bmatrix} \begin{bmatrix}
  I_a \\
  I_\beta
\end{bmatrix}
\]  

(2.20)

With \( \alpha \) and \( \beta \) co-ordinates voltages and currents are made to calculate, the instantaneous active (real) and reactive power are defined, according to p-q theory.

\[
\begin{bmatrix}
  p \\
  q
\end{bmatrix} = \begin{bmatrix}
  V_\alpha & V_\beta \\
  V_\beta & -V_\alpha
\end{bmatrix} \begin{bmatrix}
  I_a \\
  I_\beta
\end{bmatrix}
\]  

(2.21)

Where, real power is,

\[
p = V_\alpha I_\alpha + V_\beta I_\beta
\]  

(2.22)

and reactive power is,

\[
q = V_\alpha I_\beta + V_\beta I_\alpha
\]  

(2.23)

and \( p = p_{dc} + p_{ac} \)

\( q = q_{dc} + q_{ac} \)

In DC, \( p_{dc} \) and \( q_{dc} \) are represented as fundamental active and reactive powers and in AC system, they are represented as harmonic power. The average current, active and reactive powers are calculated by summing instantaneous fundamental active and reactive power demands of all the three phases.

\[
p = p_{dc}(a) + p_{dc}(b) + p_{dc}(c)
\]  

(2.24)

\[
q = q_{dc}(a) + q_{dc}(b) + q_{dc}(c)
\]  

(2.25)
The $p$ and $q$ are instantaneous powers. The instantaneous active current, $I_p$, is defined in the $\alpha$ and $\beta$ coordinates as:

$$I_{\alpha p} = \frac{V_\alpha}{V_{\alpha^2} + V_{\beta^2}} \cdot p$$  \hspace{1cm} (2.26)

and

$$I_{\beta p} = \frac{V_\beta}{V_{\alpha^2} + V_{\beta^2}} \cdot p$$  \hspace{1cm} (2.27)

The instantaneous reactive current, $I_q$, in the $\alpha$ and $\beta$ co-ordinates is defined as:

$$I_{\alpha q} = \frac{-V_\beta}{V_{\alpha^2} + V_{\beta^2}} \cdot q$$  \hspace{1cm} (2.28)

and

$$I_{\beta q} = \frac{V_\alpha}{V_{\alpha^2} + V_{\beta^2}} \cdot q$$  \hspace{1cm} (2.29)

Respective compensating $\alpha$, $\beta$ currents are:

$$I_{c\alpha} = I_{\alpha p} + I_{\alpha q}$$  \hspace{1cm} (2.30)

$$I_{c\beta} = I_{\beta p} + I_{\beta q}$$  \hspace{1cm} (2.31)

Line currents can be obtained from $\alpha$ and $\beta$ coordinates currents by inverse Clarke’s Transform:

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_{c\alpha} \\ I_{c\beta} \end{bmatrix}$$  \hspace{1cm} (2.32)

The current from equation (2.32) is compared with the current at the point of common coupling. The resulting current is taken as the reference signal.
for the modulation scheme of seven-level FCMLI. Figure 2.8 reveal the block diagram of a p-q control for reference current signal.

**Figure 2.8 p-q control**

The seven-level multilevel inverter requires a modulating signal and six carrier waves for each phase, which is shown Figure 2.9. In modulation scheme, the reference signals $I_a$, $I_b$ and $I_c$ are displaced from each other by 120°, All the carriers waves are same frequency ($f_c$) and amplitude ($A_c$), while the modulating signals contain the frequency of $f_m$ and amplitude of $A_m$.

**Figure 2.9 Modulation scheme of seven-level multilevel inverter**

At every instant, each triangular waveform and closed loop modulating sinusoidal signals are compared. Each comparison stage gives 1 or -1 based on the modulation sinusoidal signal and carrier waveform. The
modulating signal varies from 0% to 100%, based on the error signal. The amplitude of six carrier waveforms chambers with respect to positive and negative as in Figure 2.9. Whenever the modulating signal is greater than carrier waves it produces the pulses to the switches, in order to obtain the desired voltage level of the multilevel inverter.

2.4 SUMMARY

The synchronous sequential circuit based PWM method and Alternatively in Opposition (APO) disposition PWM method which are used for the different multilevel topologies were discussed. The synchronous sequential circuit offers advantages like simplicity of control circuitry-level, easy fault identification, low-cost, less space, and low power consumption. However, synchronous sequential circuit based PWM method create complexity in more than seven-level multilevel inverter based on computation time, circuit-level and space. The Alternatively in Opposition (APO) disposition PWM method provides better performance compared with synchronous sequential circuit based PWM strategy.