LIST OF SYMBOLS AND ABBREVIATIONS

ACK - Acknowledge
AXI - Advance eXtensible Interface
AMBA - Advanced Micro Controller Bus Architecture
ARM - Advanced Reduced Instruction Machine
ASIC - Application specific Integrated circuit
CMP - Chip Multi Processor
CISC - Complex Instruction Set Computer
CNI - Core Network Interface
DATA AV - Data Available
DEMUX - De -Multiplexer
DSM - Deep Sub Micron
DSP - Digital Signal Processing
DXBar - Dual Crossbar
EMI - Electro Magnetic Interference
FSM - Finite State Machine
FIFO - First In First Out
GUI - Graphic User Interface
HPS - Hardcore Processing System
ID - Identification
MPSoC - Multi Processor System On Chip
NACK - Negative Acknowledge
NI - Network Interface
NIC - Network Interface Controller
NoC - Network On Chip
NRE - Non Recurrent Engineering
PLL - Phase Lock Loop
This chapter presents the synthesis and performance evaluation of our proposed NoC-based multiprocessor systems. The router and the systems are created based on the implementation details described in the preceding chapters. Multiple configurations of the standalone router have been implemented in programmable logic and also synthesized in Cyclone V SoC FPGA to characterize the resource utilization and performance.

Multiprocessor systems were configured based on three different network topologies, having been implemented in programmable logic for system-level characterization. A high-level discussion of the potential area savings for embedded NoC support is also provided. Operational results are represented to demonstrate functionality and correctness of the router design and the NoC systems.

Experimental starts with loading an application program in PE, evaluating the architecture for different configurations and algorithms, and finally observing the results. The configured NoC components are operated at different frequencies. The Figure 6.1 shows the NoC Flow used in the design. In this design, the Nios II and HPS clock frequency is 250 MHz. Avalon bus interface clock frequency can be equal to core clock or half the frequency. The NoC network clock is 1 GHz. Slave PEs include a UART, memory, SRAM controller, floating point arithmetic cores, and VGA controller working at 100 MHz. On-chip embedded memory runs at 400 MHz frequency.

PE - Processing Elements
PAL - Programmable Array Logic
QoS - Quality Of Service
RISC - Reduced Instruction Set Computer
SNI - Slave Network Interface
SAF - Store And Forward
SF - Store And Forward
SA - Switch Allocator
ST - Switch Traversal
SoC - System On Chip
UART - Universal Asynchronous Receiver Transmitter
VC - Virtual Channel
VCT - Virtual Cut Through
WOT - Weighted Ordered Toggle
WH - Worm Hole