APPENDIX

PROTOTYPE MODEL SPECIFICATION

COMPONENT SPECIFICATION

- Altera Cyclone® V SE 5CSEMA5F31C6N device
- Altera serial configuration device – EPCQ256
- USB-Blaster II onboard for programming; JTAG Mode
- 64MB SDRAM (16-bit data bus)
- 4 push-buttons
- 10 slide switches
- 10 red user LEDs
Six 7-segment displays
Four 50MHz clock sources from the clock generator
24-bit CD-quality audio CODEC with line-in, line-out, and microphone-in jacks
VGA DAC (8-bit high-speed triple DACs) with VGA-out connector
TV decoder (NTSC/PAL/SECAM) and TV-in connector
PS/2 mouse/keyboard connector
IR receiver and IR emitter
Two 40-pin expansion header with diode protection
A/D converter, 4-pin SPI interface with FPGA

HPS (HARD PROCESSOR SYSTEM)

800MHz Dual-core ARM Cortex-A9 MPCore processor
1GB DDR3 SDRAM (32-bit data bus)
1 Gigabit Ethernet PHY with RJ45 connector
2-port USB Host, normal Type-A USB connector
Micro SD card socket
Accelerometer (I2C interface + interrupt)
UART to USB, USB Mini-B connector
Warm reset button and cold reset button
One user button and one user LED
LTC 2x7 expansion header
SOURCE CODE

// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_mult_cell ( 
   // inputs:
   A_mul_src1,
   A_mul_src2,
   clk,
   reset_n,

   // outputs:
   A_mul_cell_result
)

;

output [31:0] A_mul_cell_result;
input  [31:0] A_mul_src1;
input  [31:0] A_mul_src2;
input clk;
input reset_n;

wire  [31:0] A_mul_cell_result;
wire  [31:0] A_mul_cell_result_part_1;
wire  [15:0] A_mul_cell_result_part_2;
wire      mul_clr;
assign mul_clr = ~reset_n;
altmult_add the_altmult_add_part_1
  ( .aclr0 (mul_clr),
    .clock0 (clk),

    .aclr0 (mul_clr),
    .clock0 (clk),
.dataa (A_mul_src1[15:0]),
.dataab (A_mul_src2[15:0]),
.ena0 (1'b1),
.result (A_mul_cell_result_part_1)
);

defparam the_altmult_add_part_1.addnsub_multiplier_pipeline_aclr1 = "ACLR0",
         the_altmult_add_part_1.addnsub_multiplier_pipeline_register1 = "CLOCK0",
         the_altmult_add_part_1.addnsub_multiplier_register1 = "UNREGISTERED",
         the_altmult_add_part_1.dedicated_multiplier_circuitry = "YES",
         the_altmult_add_part_1.input_register_a0 = "UNREGISTERED",
         the_altmult_add_part_1.input_register_b0 = "UNREGISTERED",
         the_altmult_add_part_1.input_source_a0 = "DATAA",
         the_altmult_add_part_1.input_source_b0 = "DATAB",
         the_altmult_add_part_1.intended_device_family = "Cyclone II",
         the_altmult_add_part_1.lpm_type = "altmult_add",
         the_altmult_add_part_1.multiplier1_direction = "ADD",
         the_altmult_add_part_1.multiplier_aclr0 = "ACLR0",
         the_altmult_add_part_1.multiplier_register0 = "CLOCK0",
         the_altmult_add_part_1.number_of_multipliers = 1,
         the_altmult_add_part_1.output_register = "UNREGISTERED",
         the_altmult_add_part_1.port_addnsub1 = "PORT_UNUSED",
         the_altmult_add_part_1.port_signa = "PORT_UNUSED",
         the_altmult_add_part_1.port_signb = "PORT_UNUSED",
         the_altmult_add_part_1.representation_a = "UNSIGNED",
         the_altmult_add_part_1.representation_b = "UNSIGNED",
         the_altmult_add_part_1.signed_pipeline_aclr_a = "ACLR0",
         the_altmult_add_part_1.signed_pipeline_aclr_b = "ACLR0",
         the_altmult_add_part_1.signed_pipeline_register_a = "CLOCK0",
         the_altmult_add_part_1.signed_pipeline_register_b = "CLOCK0",
         the_altmult_add_part_1.signed_register_a = "UNREGISTERED",
the_altmult_add_part_1.signed_register_b = "UNREGISTERED",
the_altmult_add_part_1.width_a = 16,
the_altmult_add_part_1.width_b = 16,
the_altmult_add_part_1.width_result = 32;

altmult_add the_altmult_add_part_2
(
.aclr0 (mul_clr),
.clock0 (clk),
.dataa (A_mul_src1[31 : 16]),
.datab (A_mul_src2[15 : 0]),
.ena0 (1'b1),
.result (A_mul_cell_result_part_2)
);

defparam the_altmult_add_part_2.addnsub_multiplier_pipeline_aclr1 = "ACLR0",
the_altmult_add_part_2.addnsub_multiplier_pipeline_register1 = "CLOCK0",
the_altmult_add_part_2.addnsub_multiplier_pipeline_register1 = "UNREGISTERED",
the_altmult_add_part_2.dedicated_multiplier_circuitry = "YES",
the_altmult_add_part_2.input_register_a0 = "UNREGISTERED",
the_altmult_add_part_2.input_register_b0 = "UNREGISTERED",
the_altmult_add_part_2.intended_device_family = "Cyclone II",
the_altmult_add_part_2.lpm_type = "altmult_add",
the_altmult_add_part_2.multiplier1_direction = "ADD",
the_altmult_add_part_2.multiplier_aclr0 = "ACLR0",
the_altmult_add_part_2.multiplier_register0 = "CLOCK0",
the_altmult_add_part_2.number_of_multipliers = 1,
the_altmult_add_part_2.output_register = "UNREGISTERED",
the_altmult_add_part_2.port_addnsub1 = "PORT_UNUSED";
the_almult_add_part_2.port_signa = "PORT_UNUSED",
the_almult_add_part_2.port_signb = "PORT_UNUSED",
the_almult_add_part_2.representation_a = "UNSIGNED",
the_almult_add_part_2.representation_b = "UNSIGNED",
the_almult_add_part_2.signed_pipeline_aclr_a = "ACLR0",
the_almult_add_part_2.signed_pipeline_aclr_b = "ACLR0",
the_almult_add_part_2.signed_pipeline_register_a = "CLOCK0",
the_almult_add_part_2.signed_pipeline_register_b = "CLOCK0",
the_almult_add_part_2.signed_register_a = "UNREGISTERED",
the_almult_add_part_2.signed_register_b = "UNREGISTERED",
the_almult_add_part_2.width_a = 16,
the_almult_add_part_2.width_b = 16,
the_almult_add_part_2.width_result = 16;

assign A_mul_cell_result = {A_mul_cell_result_part_1[31 : 16] +
    A_mul_cell_result_part_1[15 : 0]};
endmodule
Comment #1

Which tools & versions are used for simulation and implementation are not shown. It should be demonstrated

Response #1

Software : ALTERA QUARTUS II version 15.0
Implementation device : Cyclone V SoC FPGA

Comment #2

Comparative study with standard latest publications such IEEE, Springer etc., are not shown. It should be in thesis by which people should know the novelty of your work

Response #2

<table>
<thead>
<tr>
<th>Implementation Target</th>
<th>Processor</th>
<th>Resource Utilization</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>xc5vlx110ff1760</td>
<td>3- µBlaze &amp; 1- Leon</td>
<td>39,700</td>
<td>Luciano et al. (2014) IEEE explore</td>
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<td>XC5VLX110T</td>
<td>2- µBlaze</td>
<td>17978</td>
<td>Wang et al. (2015) (Elsiver Vlsi Integration)</td>
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<tr>
<td>Statrix EP1S40</td>
<td>3- NIOS II</td>
<td>20000</td>
<td>Lehtorantaet al. (2011) (Springer LCNS)</td>
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<td>Virtex II Pro 50</td>
<td>5- µBlaze</td>
<td>22500</td>
<td>Karanamet al. (2013) IEEE explore</td>
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<tr>
<td>Cyclone V SoC</td>
<td>2- NIOS II &amp; ARM Cortex</td>
<td>14500</td>
<td>Present work</td>
</tr>
</tbody>
</table>
I express my profound gratitude to my respected guide Dr. A. AROKIASAMY, Professor, Department of Computer Science and Engineering, E.G.S Pillay Engineering college, Nagapattinam for his invaluable guidance, encouragement, support and patient guidance. He was a constant source of knowledge and inspiration during my work. I thank him for the confidence he had in my abilities and her whole hearted involvement in my work.

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