CHAPTER 1

INTRODUCTION

This chapter opens with the introduction to Single Event Upset and CNTFETs. It identifies the need for solutions to the Single Event Upset (SEU) problems and the need to analyse the issue in the presence of faults and development of sensor to detect the occurrence of SEU. This chapter also speaks about the importance of CNTFET circuits and the necessity to look at the impact of SEU in CNTFET circuits. It talks about the motivation behind the selection of choosing this topic for inquiry. It briefly surveys the plan goals and social organization of the dissertation.

1.1 SINGLE EVENT UPSET

For the past few years, the study about the impact of radiation effects in nanoscale circuits has gained importance. The design and implementation of the circuits at different level have been badly affected by this radiation effect. Certain research proves that as the device size is shrinking down the impact of Single Event Effect seems to increase in the circuits.

The research about radiation takes us to analyse different parameters. This includes the study of total dose, neutron-based damages and single event radiation based effects. This work concentrates more on the SEU impact on the circuits.
Semiconductor devices are prone to radiation environments. The environment can be either space environment or ground level cases. When these devices are exposed to ionisation environment they are being affected by the charged particles. These particles as they pass through the device material, they lose energy by ionising the material. This results in the introduction of electron-hole pairs along the path. The electron-hole pairs affect the struck device and also the neighbouring devices. The electrons, protons, ions when interacting with the semiconductor devices causes parameter degradation and functional failures.

At the ground level, these errors occur due to the interaction of thorium and uranium impurities located within the chip itself. Various events happened by these ionisation particles are collectively known as Single Event Phenomena (SEP). The majority of the radiation sources are neutrons, protons and alpha particles. The effect due to protons is more compared to heavy ions. Neutrons do not interact with silicon but indirectly produces the electron-hole pair. It generates secondary charged particles.

The alpha particles which are similar to heavy ion particles carries positive charges, constitutes most of the cosmic rays and cause reliability issues in the devices. Heavy ions have the atomic number larger than one. Some of the alpha particles are Ne, Ar, Ni, etc. They have longer penetration property. Study of SEUs by IBM concludes that the upset threat decreases when the altitudes are approaching sea level. Every device may experience the SEU once in twelve months. Some of the additional causes for upsets are power glitches, Alpha particles, software bugs and product quality.

Upsets have been found to increase as the memory size increases. Hence, as the memory densities had increased nowadays the impact of SEU in these devices has to be studied and should be taken care of properly.
The unique properties of carbon nano materials have made their way high-performance devices. The high mobility and ambipolar behaviour found to be useful in other analog devices which include power amplifiers and radio receivers (KocabasC, 2008). Therefore, it is necessary to study the radiation response, hardening and detecting schemes in parallel with device development to have good reliability in harsh environments.

1.2 (CARBON NANO TUBE FET) CNTFET

The necessity to move towards the CNTFET devices is being explained in the forthcoming lines. The semiconductor industry is scaling down the device size and increasing the size of integration. The basic CMOS device size has reduced from several microns down to nano scales. The short channel effects, DIBL increases rapidly with decreasing device size.

The new devices which are found to be promising over the normal CMOS circuits include SOI devices, FinFET, CNTFETS. Research works project CNT devices as a promising material. The main advantage of replacing the silicon MOSFET with CNTFET is the reduction in leakage currents. Much progress has been made in research work which projects CNTFETs to be promising over the silicon devices.

The previous results indicate that the radiation damaging the crystal lattice by creating the defects. This defect orientation depends on the energy, mass and the angle of the incident ions.

In this research, we have projected our work towards the study of CNTFET SRAM voltage and current variations in the presence of SEU, discussed the resistive open and bridging faults, discussed the techniques to
detect the occurrence of SEU and reviewed hardening techniques to correct the errors.

1.3 MOTIVATION

Since the late 1990s, the study of SEU has become increasingly attractive to designers of space-based systems. The effect of SEU on the highly integrated device is much higher. Hence the analysis of these effects on the emerging components is required.

CNTFET possesses the advantage of having good electrical, optical and chemical properties. The Short channel effects in CMOS down beyond 32nm is more when we do the scaling, these kind of devices is losing importance and paving way for new kind of devices which includes CNTFETS, FinFETs. The increase in leakage currents is very much reduced in CNTFET devices.

Hence the study of the impact of SEU in CNTFET based devices seems to be unavoidable. The development of detection circuitry and hardening circuitry are also challenging one for CNTFET based devices.

1.4 DESIGN GOALS

- To study the effect of Single event upsets in current and voltage behaviour, leakage current variations in CNTFET SRAM and comparison with CMOS SRAM.
- To study the impact of various faults present by inserting resistors in particular nodes and how they impact the output values in the presence of SEU for CNTFET SRAM.
• To develop novel BICS Circuit to detect SEU in CNTFET.
• To develop the hardening scheme for the reduction of SEU in CNTFET SRAM.

1.5 CONTRIBUTION TO THE RESEARCH:

The objective of this research is to explore and examine the impact of single event upset in CNTFET SRAM, the introduction of the different type of faults in CNTFET SRAM in the presence of SEU, to develop effective circuitry to detect and correct the errors. The research work was initialised with the study of comparing CMOS based circuits and CNTFET based circuits. All the simulations are carried out in Synopsis HSPICE. Berkeley Predictive model files are used for modelling CMOS SRAM and the Stanford CNTFET library files are used for CNTFET circuits. HSPICE is faster and has more capabilities like easy to detect error, high accuracy and includes good algorithms for convergence issues.

The leakage currents are first analysed for CNTFET Inverter circuit, compared with CMOS Inverter and the results are compared with the literature work. The impact of leakage currents in CNTFET circuit is extended for SRAM. SRAM leakage currents are analysed at HOLD mode. Current characteristics in READ and WRITE operations of CMOS SRAM and CNTFET SRAM are studied and compared. Single Event Upsets are modelled with an exponential current pulse and is applied to NMOS and PMOS OFF transistors and the impact of SEU on voltage and current characteristics are done. The performance analysis of CNTFET in terms of variation in diameter, chirality, temperature, the threshold voltage is done.

Fault analysis is done in CNTFET SRAM with the introduction of resistors. Fault occurrence is analysed first without the presence of SEU and
comparative study is done with CMOS SRAM. Fault analysis is then extended with the introduction of SEU. The occurrence of the fault in CNTFET SRAM is observed for a smaller value when compared to CMOS SRAM. The flipping of cells varies with performance parameters also which is not observed in the previous case. Variations in faults with variation in diameter values are also analysed.

The previous detection techniques failed to detect for very small flow of current. In Hardening schemes previous techniques were applied only for CMOS SRAM. Several error detection and correction circuitries is experimented. Comparison of several correction and hardening techniques with respect to CMOS SRAM is done and extended for CNTFET SRAM. Fault tolerant design techniques are also used along with the correction circuits to reduce the impact of single event upset in SRAM. In this research work, it is extended for CNTFET SRAM and experimented for various diameter and chirality factors.

A novel Bulk/Substrate based detection scheme is developed. The advantage is that it is connected to the substrate and not to the power terminals. It is fast compared to Error Control Circuitries and is detecting the SEU and not the internal signals. It is having the flexibility to work in different sizes. The number of transistors used is also less compared to previous error detection mechanisms. The same circuit can be extended for detection of SEU in PMOS devices.

Present research involving CNTFET SRAM deals with leakage analysis and dealt with the dual chirality characteristics. Fault introduction and analysis of faults were limited with CMOS SRAM. The detection algorithms and circuits possess limitations in terms of detecting the current at nanoscales and restricted with CMOS SRAM. The performance metrics evaluated and
experimental analysis done helps us to choose between the choice of using CMOS or CNTFET SRAMS.

1.6 STRUCTURE OF DISSERTATION

The thesis is organised into seven chapters and each chapter focusing on the review of existing work, implementation of proposed approach, experimental evaluation of the results along with a comparative investigation. This thesis work is based on the author's research work which is submitted as manuscripts or still in review during the PhD study. Each chapter starts with an introduction, which gives a connection between previous chapters and the present chapter. The incisive conclusion concludes each chapter. The organisation of the thesis is summarised as follows.

In chapter 1 an introduction of the CNTFET devices, its comparison with CMOS devices, introduction to SEU, motivation and Design goals have been discussed.

Chapter 2 describes previous related works happened with Single Event Upsets, carbon nano tubes, faults in memories, the advantages and disadvantages of various detection circuits, and several hardening circuit development.

Chapter 3 describes the concept of Single Event Upset (SEU), modelling of SEU, its impact on CMOS SRAM and CNTFET SRAM. The voltage and current characteristics in the presence of SEU have been analysed.

In chapter 4 discusses the introduction of faults in CNTFET SRAM. The effect of faults in the presence of SEU and their experimental
results is discussed. In this chapter resistive open and Resistive bridging faults are introduced in CMOS SRAM and CNTFET SRAM and variation in the resistance values and fault models due to the presence of SEU is described.

Chapter 5 deals with the detection of SEU in SRAM. Various Built In Current Sensor circuits have been reviewed and an effective BICS for CNTFET SRAM is developed. Its advantages over other circuits have been discussed.

Chapter 6 covers the review of hardening schemes with CMOS SRAM. When certain techniques are applied for CNTFET SRAM, there are some variations occurred in the output when compared to CMOS SRAM. The necessity for the new hardening scheme for CNTFET SRAM is also elaborated in this chapter.

Chapter 7 gives the summary and conclusion of the thesis work. It has also summarised the future Scope of CNTFET based detection and hardening schemes, the necessity for the extension of the research to sub circuits.