CHAPTER 5

CONTROL TECHNIQUES FOR THREE STAGE SOFT SWITCHING BOOST CONVERTERS

5.1 GENERAL

This chapter deals with various control schemes related to Three stage soft switching boost converter system. The load and line regulations of the boost converter depend largely on the control schemes. Various techniques have been developed to meet the requirement of output voltage and at the same time it is also necessary to get more resolution to increase precision. By varying on time of the switching device present in a converter, the output voltage can be maintained at a constant value during load variations and supply voltage variations. Pulse-width modulation (PWM) is the most common control scheme for boost converter. However, the resonant switching converters require a variable-frequency controller to achieve the desired energy conversion than the PWM scheme.

5.2 PULSE-WIDTH MODULATION

The technique of modulating the duration of the ON or OFF time of pulses that are applied to the semiconductor switch is called Pulse width modulation (PWM). The expression for duty ratio D is given in Equation 5.1.

\[
D = \frac{t_{on}}{t_{on} + t_{off}}
\]  

(5.1)
Modulating either $t_{on}$ or $t_{off}$ or both can vary duty ratio. There are two schemes of PWM.

- Fixed frequency PWM
- Variable frequency PWM.

With fixed frequency PWM, both $t_{on}$ and $t_{off}$ are varied to maintain frequency constant. In variable frequency PWM, either $t_{on}$ or $t_{off}$ is kept constant and frequency is varied. The major problem associated with the variable frequency PWM is Electro magnetic interference due to the varying switching frequency. There are two PWM modes of operation depending on the control signals required.

- Voltage-Mode PWM scheme
- Current mode PWM scheme

5.3 VOLTAGE MODE PWM SCHEME

Switched-mode power supply systems inevitably require feedback control to regulate the output voltage to a desired value. The output voltage should be kept constant, regardless of changes in the input voltage or load current. This is accomplished by building a feedback circuit that varies the converter control input in such a way that the difference between output voltage and desired reference value should be minimized. Figure 5.1 shows voltage-mode control of DC-DC Converter. The error amplifier compares the sampled output voltage with a fixed reference voltage and generates an error voltage.

$$
V_e = V_{ref} - \frac{2}{Z_1} \left( V_a \frac{R_a}{R_1 + R_2} - V_{ref} \right)
$$  (5.2)
To generate the required duty ratio, the control input from the error amplifier output, is compared with fixed saw tooth waveforms. Whenever the error voltage is higher than the sawtooth signal, the output is high. This PWM signal is then fed to a gate drive circuitry that drives the switching MOSFET of the boost converter. The output voltage of the boost converter running in steady state continuous conduction mode is given as

\[ V_o = \frac{V_{in}}{1-D} \]  \hspace{1cm} (5.3)

From Equation (5.1), it seems that the feedback compensation network only has to increase the duty ratio as output voltage decreases and vice versa. However, the output voltage does not change in phase with the duty ratio. Assume that some AC variation is introduced in the converter duty ratio as

\[ d(t) = D + \tilde{d}(t) = D + \tilde{d}\sin\omega t \]  \hspace{1cm} (5.4)

Then, the output voltage is

\[ v_o(t) = V_o + \tilde{v}_o \sin(\omega t + \Phi) \]  \hspace{1cm} (5.5)

Where the amplitude of AC variation \( |\tilde{v}_o| \) is much smaller than the steady-state output voltage \( V_o \) and \( \Phi \) is the phase difference between duty ratio and output voltage variation. The control-to-output transfer functions of voltage-mode-controlled boost converters are given in Equation (5.6). The boost converter exhibits two poles and a right half plane zero. The right half plane zero moves with load condition and duty ratio which makes it very difficult to have a high crossover frequency for a boost converter operating in continuous conduction mode. The presence of right half plane zero causes the output to change in the opposite direction when the duty ratio changes fast, which limits the speed of the control loop.
Figure 5.1 Voltage mode control of DC-DC converter

\[
\frac{v_0}{v_{EA}} = \frac{v_o}{v_p(1-D)} \frac{(1-s)/\omega_{HZ}}{1 + \frac{s}{Q\omega_o} \left(\frac{s}{\omega_o}\right)^2}
\]  

(5.6)

where,

\[
\omega_{HZ} = \frac{(1-D)^2 R_L}{L}
\]  

(5.7)

\[
\omega_o = \frac{(1-D)}{\sqrt{L C_o}}
\]  

(5.8)

\[
Q = (1 - D) R_L \sqrt{\frac{C_o}{L}}
\]  

(5.9)

The design specifications and the circuit parameters, for simulation are chosen as: input voltage =12V, desired output voltage =24V, inductance =1mH, capacitance =100\(\mu\)F, and load resistance =100\(\Omega\). The switching frequency is set to 20 kHz. The simulation circuit is shown in Figure 5.2.
Figure 5.2 Simulink model for TSSSBC with Voltage mode control

In voltage mode control, the three stage soft switching boost converter output is sampled using a potential divider arrangement to get 5V for the rated output voltage. It is in turn subtracted with a reference of 5V using a constant block to produce the error signal. The error signal is compared with a sawtooth wave produced using a repeating sequence block. The frequency of the sawtooth wave decides the frequency of operation of MOSFET. The output of the comparator which is realized using relational operator, provides the PWM signal based on its sawtooth input. The simulated output is shown in Figure 5.5. The sawtooth oscillator output is shown in figure 5.5a. The error signal produced by comparing reference signal with the feedback signal is shown in figure 5.5b. The relational operator output produced by comparing the error signal with the oscillator input is shown in Figure 5.5c. The pulses produced for gate signal to MOSFET are shown in Figure 5.5d. The three pulses to the MOSFET are phase shifted by 120°. The output voltage is shown in Figure 5.5(e). It increases and actually reached 47.4V at 0.1 second. The simulated output shown here is only for the time period 0.02 to 0.0205s to explain the transient condition. Feed back
signal proportional to the output is shown in Figure 5.5 (f). It is compared with the reference signal to produce the error signal.

(a)

(b)

(c)

Figure 5.3 (Continued)
Figure 5.3  Simulation Results of Voltage mode control (a) Input Voltage (b) Error signal (c) Comparator Output (d) Feedback Voltage (e) Output Voltage (f) Inductor Current

Line regulation is a measure of the ability of the power supply to maintain its output voltage with variations in the input line voltage. Line regulation is expressed as percent of change in the output voltage relative to the change in the input line voltage. The output voltage is regulated for 17% as source disturbance by closing a feedback loop between the output voltage
and duty ratio signal. The response of the system for step change in input Voltage is shown in Figure 5.4. It is inferred that the voltage mode output is having a smooth transient for change in input Voltage.

![Figure 5.4](image)

**Figure 5.4** Output voltage, current and power of voltage control for line regulation (a) Without Voltage controller (b) With Voltage controller

Load regulation is the capability to maintain a constant voltage level on the output channel of a power supply despite changes in the supply's load (such as a change in resistance value connected across the supply output. Figure 5.5 shows the response of the system without voltage controller and with Voltage controller. The output voltage is maintained almost constant and fast voltage transient recovery takes place using voltage control scheme.

With respect to current waveform there is a huge spike present in voltage mode control. This is the disadvantage of voltage mode control as it may lead to damage of switch present in the system.
5.4 CURRENT MODE PWM SCHEME

Voltage-mode control contains a single loop and adjusts the duty ratio directly in response to output voltage changes. Hence, it is also called duty-ratio control. During transient condition, the inductor current of TSSSBC may exceed causing excessive switch current. Voltage mode control is not suitable for interleaved converters as it possess problem while current sharing as shown in Figure 5.6. The circled portion shows that the current is high during transient condition and hence may cause damage to the switches.
In current mode control, several converters can be connected in parallel without a load sharing problem because all the converters receive the same Pulse width modulated control signal from the feedback circuit and hence carry the same magnitude of current. Current-mode control is a multiple-loop control method that contains two loops: an inner current loop and an outer voltage loop. Current loop controls the inductor peak current, while the voltage loop controls the output voltage. The technique is called current-mode control because the inductor current is directly controlled, whereas the output voltage is controlled only indirectly by the current loop. The inductor peak current is close to the inductor average current. The inductor average current is related to the load current. In TSSSBC, the average input current is equal to the average inductor current. The inner current loop initially adjusts the duty ratio in response to the changes in inductor current, and the outer voltage loop produces a reference voltage for the current loop in response to the changes in the converter output voltage. The duty ratio is determined by the time instants at which the inductor or switch current reaches a threshold level determined by a control signal. This threshold level becomes the input to the inner loop. The key feature of current mode control is that the inner loop changes the inductor into a voltage-dependent current source at frequencies lower than the crossover frequency of the current loop. The action of the current loop is similar to that of a sample-and-hold circuit, which is a nonlinear, time-varying system.

The different types of current-mode control techniques are shown in Figure 5.7. In constant frequency control, the switching frequency is constant and synchronized to a clock signal. In variable frequency control technique self-oscillating converters are present.
Figure 5.7 Types of Current mode control

In this work fixed frequency peak current mode control with ramp compensation and Hysteresis control is discussed.

Circuit of the fixed frequency peak current mode control is shown in Figure 5.8.

Figure 5.8 Peak current mode control
It contains two loops viz. an inner current loop and an outer voltage loop. The inner current control loop contains an op-amp voltage comparator, a set–reset latch, a clock (CLK), and a current sensor which is noninductive sense resistor $R_s$, which senses the inductor current $i_L$ or the switch current $i_S$. In general, $R_s$ represents the transfer function from the inductor or switch current to the current sensor output voltage. It may be a transfer function of a current transformer, which has corner frequencies in the low-frequency and high-frequency ranges. The latch $S$ input sets (or presets) the $Q$ output to 1, and the latch $R$ input resets (or clears) the $Q$ output to 0. The op-amp comparator, the set–reset latch, and the clock CLK form an inductor current modulator. The analog control voltage $v_C$ is applied to the comparator inverting input, and the voltage $R_s i_L$ (proportional to the inductor current $i_L$) or the voltage $R_s i_S$ (proportional to the switch current $i_S$) is applied to the comparator non inverting input. Figure 5.9 depicts the key waveforms of PWM converter with current-mode control.

![Figure 5.9 Key waveforms of Current mode control](image-url)

The clock generates voltage pulses at a constant clock frequency equal to the switching frequency $f_s = 1/T_s$. When the clock output voltage goes high, the latch $Q$ output goes high. Therefore, the gate-to-source voltage
$v_{GS}$ also goes high, turning the switch on. This event initiates the transistor on-time and starts the cycle $T_s$ of the switching frequency $f_s$. Since the turn-on times are periodically clocked, a constant-frequency operation is obtained. While the switch is on, the inductor current $i_L$ and the switch current $i_S$ increase linearly. The inductor current $i_L$, or the switch current $i_S$, is sensed by a current probe. The currents $i_L$ and $i_S$ are equal during the transistor on-time. The sensed inductor current $i_L$ (or the switch current $i_S$) flows through the resistor $R_s$ and develops a voltage $R_s i_L$. When the voltage $R_s i_L = v+$ is lower than the control voltage $v_C = v-$, the comparator output voltage $v=0$ goes low. When the voltage $R_s i_L$ reaches the control voltage $v_C$, the comparator output voltage $v_R$ goes high, resetting the latch $Q$ output to 0. Therefore, the gate-to-source voltage $v_{GS}$ goes low, turning the switch off for the remaining time of the switching period. As a result, the inductor current $i_L$ decreases. Since $R_s i_L < v_C$, the comparator output voltage $v_R$ goes low. In summary, the clock sets the latch and turns the transistor on at the beginning of the cycle $T_s$. The comparator resets the latch and turns the transistor off when the inductor current $i_L$ reaches the control current $i_C$. Consequently, the peak inductor current $I_{Lpk}$ and the peak switch current $I_{Spk}$ follow the control current $i_C = v_C/R_s$. Thus, amplitude modulation of the inductor current $i_L$ takes place, where the control current $i_C$ or the control voltage $v_C$ is the modulating signal. The average inductor current is

$$I_L = I_{Lpk} - \frac{\Delta i_L}{2} \quad (5.10)$$

Since the peak inductor current is directly controlled, this method is called peak current mode control.

The outer voltage loop senses the output voltage and develops a control voltage $v_C$, which serves as a reference voltage for the inner current loop; thus, the outer voltage loop adjusts the control voltage $v_C$. The inductor
jcurrent is fed back through a sensing resistor $R_s$ and the resulting voltage $R_s i_L$ is compared with the control voltage $v_C$. The output voltage is fed back through a resistive voltage divider $R_A - RB$, is compared with the reference voltage $V_R$, and sets the control voltage $v_C$. The input to the current loop is the control voltage $v_C$, which is compared to the sensed inductor current $i_L$ (or voltage $R_s i_L$) and sets the duty ratio. In turn, the duty ratio produces a corresponding inductor current and output voltage. As a first-order approximation, the current loop causes the inductor to act like a voltage-controlled (or current-controlled) current source $v_C/R_s$.

Current-mode control offers several advantages over voltage-mode control. The load current can be held below a predetermined maximum level in current control. It provides a fast response and over current load protection. In addition, the transient peak values of the inductor, switch, and diode currents are limited. A disadvantage of peak-current-mode control is its inherent instability of the inner current loop when $D > 0.5$, resulting in sub-harmonic oscillations. For a duty ratio greater than 0.5, slope compensation is required.

The instability of the current loop can be eliminated by subtracting an artificial periodic ramp waveform from the control signal waveform, or by adding an artificial ramp waveform to the inductor or switch current waveform.

Figure 5.10 shows the inductor voltage and current waveforms under Continuous conduction mode. The rising and falling slopes of the inductor current waveform are

$$M_1 = \tan \alpha = \frac{\Delta i_L}{\Delta T_s}$$  \hspace{1cm} (5.11)
\[ M_2 = \tan \beta = \frac{\Delta i_L}{(1-D)T_s} \]  

(5.12)

The ratio of the absolute value of inductor current slope is given by

\[ \frac{M_2}{M_1} = \frac{D}{1-D} \]  

(5.13)

The inner current loop is stable if \( \frac{M_2}{M_1} < 1 \). Therefore the condition \( M_2 < M_1 \) should be satisfied for stable operation. This occurs for \( D < 0.5 \). At \( D = 0.5 \), the converter is marginally stable. The inner current loop is unstable if \( D > 0.5 \).

The block diagram for deriving the input voltage-to-duty ratio transfer function (\( A_{id} \)) for the closed-current loop is shown in Figure 5.11.
The current through the inductor is

\[ i_t = i'_t - i''_t = T_{pi}d - A_i i_0 \]  \hspace{1cm} (5.14)

and the duty ratio is given by

\[ d = -T_{ms}R_s i_1 = -R_s T_{pi} T_{ms} d + R_s A_i T_{ms} i_0 \]  \hspace{1cm} (5.15)

Resulting in

\[ d(1 + R_s T_{pi} T_{ms}) = R_s A_i T_{ms} i_0 \]  \hspace{1cm} (5.16)

the input voltage-to-duty ratio transfer function for the current-closed loop,

\[ A_{vd}(s) = \frac{d(s)}{i_o(s)} = \frac{R_s T_{ms} A_i}{1 + T_i} = \frac{12f_0^2 A_{lx}(s+\omega_{en})}{T_{pi}(s+\omega_{zi1})(s^2 + \omega_{sh}s + 12f_0^2)} \]  \hspace{1cm} (5.17)

For \( s=0 \)

\[ A_{vd0} = \frac{A_{lx} \omega_{en}}{T_{pi} \omega_{zi1}} = \frac{(1-D)R_L}{2V_o} \]  \hspace{1cm} (5.18)

Figure 5.12 shows the response of the duty ratio to a step change of the load current from 0.5 to 0.6 A. The steady-state value of the duty ratio is

\[ d_T(\infty) = D(0^-) + A_{vd0} \Delta I_o = 0.5 + 0.5 \times 0.1 = 0.55 \]  \hspace{1cm} (5.19)
The transfer function of the forward path in outer loop is given by

\[ A_o = \frac{V_o}{V_E} = T_{co} T_{clo} T_{po} \]  \hspace{1cm} (5.20)

The loop gain of the outer loop is

\[ T_o = \frac{V_F}{V_E} = \beta A_o = \beta T_{co} T_{clo} T_{po} \]  \hspace{1cm} (5.21)

The closed loop gain of the outer loop is

\[ T_{clo} = \frac{V_o}{V_R} = \frac{A_o}{1 + \beta A_o} \]  \hspace{1cm} (5.22)

The closed loop output impedance is given by Equation 5.2. This value will be nearer to zero.

\[ Z_{oclo} = \frac{Z_o (1 + T_{io} + R_s T_{m} H_{sh} A_{io} T_{po})}{1 + T_{po} + T_{io}} \]  \hspace{1cm} (5.23)

The simulation circuit of Current mode PWM control scheme for TSSSBC is shown in Figure 5.13. The duty ratio of the converter is based on the reference control signal. The MOSFET turns off when the inductor current
reaches the reference level. Hence the failure of MOSFET due to excessive current is prevented by setting the reference control signal. This circuit also includes a compensating ramp to overcome the instability for $D>0.5$. The simulation circuit consists of two loops. The outer loop is used to sense the output voltage and provides the reference control signal to inner current loop. The inner current control loop signal senses the current flowing through the MOSFET and thereby keeps the output voltage constant. The SR latch used in the simulation is to provide the gate signal. The input to the S terminal is a pulse train whose frequency is equal to the converter operating frequency. Its pulse width is kept minimum as it is required only as a triggering pulse to activate SR latch. For the three MOSFETs present in the TSSSBC the pulses obtained from the latch is phase shifted by 120°.

![Figure 5.13 Simulation circuit of Current mode PWM control scheme](image)

The simulated results are shown in Figure 5.14. The inductor current based on which the current control loop is operated is shown in Figure 5.14(a). The comparator output based on inductor current and...
compensated ramp added with voltage reference signal is shown in Figure 5.14(b). The comparator output is high when the inductor current reaches the reference value. The comparator output is used to reset the latch. The triggering pulse provided for S terminal of the SR latch is shown in Figure 5.14(c). Figure 5.14(d) shows the output of the SR latch which provides the gate signal for the MOSFET. The compensating ramp whose slope is based on the negative slope of the inductor current is shown in Figure 5.14(e). The output current and the output voltage obtained for an input of 12V is shown in Figure 5.14(f) and (g) respectively. When compared to the Voltage mode control, fast transient response is obtained for current mode control. This can be inferred from the output voltage waveform. The output voltage not reached the final value at 0.02 second and it is still raising and reached only during 0.1 second. But the output voltage reached its maximum of 24V with ripple of 1V and the steady state output can be viewed from Figure 5.14(f).

![Figure 5.14 (a)](image1)

![Figure 5.14 (b)](image2)
Figure 5.14 (Continued)
Figure 5.14 Simulation output of Current Controlled TSSSBC (a) Inductor Current (b) Comparator Output Voltage (c) Triggering pulse (d) Flip flop output Voltage (e) compensating ramp (f) Output Voltage (g) Output current

The line and load regulation of the converter under change in source and load condition are determined by varying the source voltage and load resistance respectively and the corresponding output is shown in Figure 5.15 and 5.16 respectively.

Figure 5.15 Output voltage, current and power of current control with Line Regulation (a) Without current control (b) With Current Control

Figure 5.15 clearly represents the absence of overshoot during line regulation when a step change in input voltage is applied to the system.
5.16 shows the response of the system for change in load. There is no sudden overshoot present in the current waveform. Hence the peak current mode control is more advantageous than Voltsge mode control.

![Figure 5.16](image)

**Figure 5.16** Output voltage, current and power of current control with Load Regulation (a) Without Current Control (b) With Current control

### 5.5 HYSTERESIS CURRENT CONTROL

In hysteresis current mode control method, the main switch is switched on when the inductor current goes below a certain value, and it is switched off when the inductor current goes above a specified maximum value. Thus, the amplitude of the current is bounded between these two limits. It does not require an external oscillator or saw-tooth generator for operation and it has the ability to provide a fast response to a transient event. Figure 5.17 shows a block diagram of a current-mode hysteretic controlled DC-DC converter.

The power converter circuit with feedback control consists of a TSSSBC with switches, storage elements, an inner controller, an outer
controller adjusting the inner loop’s reference in response to deviations from the desired output. The control system shown in fig consists of two control loops. One is the current control loop and the other is the voltage control loop. The error between the actual output voltage and reference voltage gives the error voltage. A Proportional or PI control block can use the voltage error signal to provide a reference current for hysteresis control.

The control law for hysteresis control is

\[ u = \begin{cases} 1, & S > 0 \\ 0, & S < 0 \end{cases} \]  

(5.24)

Where ‘u’ is a discontinuous input that is either 0 or 1, \( S \) is the difference between the two comparator inputs

\[ S = K_p(v_{ref} - v_o) - ki_L \]  

(5.25)

where \( K_p \) is the controller gain as proportional controller is considered and \( k \) is the current sensing gain.

The simulation studies have been performed on a DC-DC boost converter based on the hysteretic current control method under dynamic conditions of line variations. The boost converter parameters chosen for the simulation studies are input voltage of 12V, for a desired output of 24V,
inductance \( L = 3 \text{mH} \), capacitance \( C = 110 \mu\text{F} \), load resistance \( R = 100 \Omega \), voltage reduction factor \( k_i = 0.11 \), proportional gain \( k_p = 0.011 \). The switching frequency \( f_s \) is set to 20 kHz. The output voltage is sampled in each cycle and it is compared with the reference input signal. A simple proportional controller is considered here. The simulations are done using MATLAB/SIMULINK.

Figure 5.18 Simulation circuit of Hysteresis current mode control

The simulated output is shown in Figure 5.19. A step change in load is made at 0.4 second. This is reflected in the inductor current waveform as shown in Figure 5.19(a). The frequency of the inductor current is increased after 0.4 second as the relay is turned on and off within the upper and lower band limit. The pulses applied to MOSFET is shown in Figure 5.19(b). The increase in frequency after 0.4 s is observed from the waveform. This change in frequency may complicate the filter design and produces EMI interference.
5.6 COMPARISON OF CURRENT WAVEFORMS

As the line and load fluctuates, the voltage control strategy regulates the voltage at the prescribed reference value. However, the oscillations occur at the current. To minimize the oscillations, current control strategy has been introduced along with the voltage control strategy. Hysteresis control strategy provides uniform band of current for step change in input. Hysteresis method is easy to implement and possess good transient response. But this control strategy possess disadvantage of variable frequency for change in load. It is easy to connect power converters with current-mode control in parallel in order to increase current capability and/or redundancy without load current-sharing problems. This is because the output current of each unit is determined by the control signal. When current mode control is used, the reference signal for the inner loop and the inductor current depends on the converter output voltage. As a result, one variable controls the other.
Consequently, there is only one true state variable (i.e., the capacitor voltage), resulting in a system that behaves approximately as a first-order system.

Figure 5.20 Comparison of current control waveforms

The comparison table for the three controllers are given in Table 5.1. As the hysteresis band is fixed to be 0.02, it is maintained as per the design. There is a reduction of 1 W as compared to other methods in hysteresis controller, As the frequency is varied the average output power is varied.

Table 5.1 Performance comparison of control strategies

<table>
<thead>
<tr>
<th></th>
<th>Voltage mode</th>
<th>Current Mode</th>
<th>Hysteresis</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage</td>
<td>48V</td>
<td>48V</td>
<td>46V</td>
</tr>
<tr>
<td>Output current</td>
<td>0.5A</td>
<td>0.5A</td>
<td>0.5A</td>
</tr>
<tr>
<td>Output Power</td>
<td>24W</td>
<td>24W</td>
<td>23W</td>
</tr>
<tr>
<td>Voltage ripple</td>
<td>0.8</td>
<td>0.6</td>
<td>0.02</td>
</tr>
<tr>
<td>Current ripple</td>
<td>0.6</td>
<td>0.2</td>
<td>0.02</td>
</tr>
</tbody>
</table>
5.7 CONCLUSION

In this chapter the voltage mode, current mode and hysteresis current mode control techniques are applied to TSSSBC and the performance of the converter is studied. The MATLAB/SIMULINK model is developed for all the three techniques and the simulated output is analyzed. It is inferred the voltage mode technique is not suitable for interleaving operation as it cause high current transient during current sharing. The peak current mode PWM Control is found suitable for TSSSBC than the other two control strategy discussed in this chapter.