LIST OF SYMBOLS AND ABBREVIATIONS

1D	-	One Dimensional
2D	-	Two Dimensional
3D	-	Three Dimensional
ALUs	-	Arithmetic and Logic Units
AOI	-	AND-OR-INVERT Logic
ASICs	-	Application Specific Integrated Circuits
CAD	-	Computer Aided Design
CF	-	Cost Function
CLBs	-	Configurable Logic Blocks
CPLDs	-	Complex Programmable Logic Devices
CSA	-	Carry Select Adder
CSA	-	Carry Select Adder
CSO	-	Cuckoo Search Optimization
DDFG	-	Directed Data Flow Graph
DDM	-	Data Dependency Matrix
DSP	-	Digital Signal Processing
EAC	-	Empty Area Compaction
EDA	-	Electronic Design Automation
EDF	-	Earliest Deadline First
FPGAs	-	Field Programmable Gate Arrays
GA	-	Genetic Algorithm
GPP	-	Genetic Purpose Processor
GSA	-	Gravitational Search Algorithm
HDLs	-	Hardware Description Languages
I/O	-	Input/ Output
IC	-	Integrated Circuit
JTAG	-	Joint Tag Access Group

KAMER	-	Keeping All Maximal Empty Rectangle
LUT	-	Look Up Table
MAC	-	Multiply and Accumulate
MER	-	Maximal Empty Rectangle
MGA-ASICs	-	Masked Gate Array-Application Specific Integrated Circuits
MSDL	-	Merge Serve Distribute Load
NOL	-	Non-Overlapping
NP	-	Non-Polynomial
NRTHT	-	Non Real Time Hardware Tasks
OL	-	Overlapping
PaR	-	Placement and Routing
PDR	-	Partial-Dynamic Reconfiguration
PLDs	-	Programmable Logic Devices
PROMs	-	Programmable Read Only Memories
PRTR	-	Partial Run Time Reconfiguration
PSO	-	Particle Swarm Optimization
RAM	-	Random Access Memory
RC	-	Reconfigurable Computing
RCA	-	Ripple Carry Adder
RDDFG	-	Random Directed Data Flow Graph
RecOS	-	Reconfigurable computing Operating System
RMU	-	Resource Management Unit
RTHT	-	Real Time Hardware Tasks
RTL	-	Register Transfer Logic
RTR	-	Run Time Reconfiguration
SQRT	-	Square Root
SRAM	-	Static Random Access Memory
SUR	-	Space Utilization Ratio

TTM	-	Time to Market
VHDL	-	Very high speed Hardware Description Language
VLSI	-	Very Large Scale Integration
XST	-	Xilinx Synthesis Tool