CHAPTER 6

CONCLUSION

In case of advanced computing platforms, high performance applications such as image processing, embedded systems, cryptography, matrix multiplications and network security demand the processors with a higher processing capability in terms of speed, area and power than ever before. With the evolution of field programmable devices, demands get fulfilled because of their excellent features such as reconfigurability and high parallelism. Due to an increase in the advancement of VLSI technology, FPGAs with a high density and software support are now available that attract VLSI designers to enter the field of reconfigurable computing. With the help of CAD tools, designers can implement the digital system with FPGAs, but with the cost issues in the placement process of the design flow.

In order to attain the complete profit in utilizing the FPGAs computing capability, certain issues should be solved irrespective of the incoming applications being either real or non-real time in their operations. To solve the issues, certain investigations have been carried out to determine the suitable and effective algorithms that can be used in FPGA based system design process. Both real and non real time hardware tasks placement algorithms have been discussed to ensure that the FPGA based design fulfils the necessity of current emerging applications. Speed and area are the two

placement metrics to be considered while developing these placement algorithms.

In the case of real time applications execution, the placement algorithms must define the speed at which the application gets executed and the compactness in placement of the incoming tasks related to the application In this research work, existing methods considered in the discussion include the overlapping and non-overlapping maximal empty rectangles (MER) best fit based placement, overlapping MER first fit based placement and the Least Interference fit placement algorithms. Further, bottom left first fit row-column reduction method,windowing sum CLook method, Top left first fit based on column-row reduction method and bottom left first fit tree search method based placement algorithms have also been developed for performance analysis. To achieve high speed in real time hardware tasks execution, a new concept of Windowing-OR-Logic method in first fit strategy based placement algorithm has been proposed in this research work, and the simulation has been carried out for both small scaled and large scaled FPGA devices. The proposed method outperforms better than the others, especially for large scaled devices.

The performance improvement of proposed method in terms of algorithm execution time are found to be 1.9 and 1.6 times better than the overlapping and non-overlapping maximal empty rectangles (MER) best fit method,1.4 times better than the overlapping MER first fit method , 6.2 times better than the Least interference fit method,12.8 times than bottom left first fit row column reduction method,8.99 times better than the windowing sum CLookmethod,1.3 times better than the top left first fit based on column-row reduction method and 2.32 times better than the bottom left first fit tree search method placement algorithms.

In order to achieve the best performance in non-real time applications execution, certain optimization methods have to be applied to the incoming application tasks before the placement phase. Both the algorithmic and logic level optimization methods have been discussed in this research work. In algorithmic approach, several optimization algorithms such as particle swarm optimization, attractive-repulsive particle swarm optimization, gravitational search algorithm and cuckoo search optimization algorithms have been considered to obtain the better placement with a minimal wirelength and area.. Non real time hardware tasks can be modelled using directed data flow graphs and have been randomly generated for experimentation. The simulation has been carried out for wire length and the area minimization subject to single and multi-objective constraints.

From the simulation results, it can be observed that the cuckoo search optimization algorithm produces better placement when compared to the others. Sample discussions on performance improvement of the cuckoo search algorithm are 36.8% better than Particle Swarm Optimization for the input DDFG7, 30.3% better than Attractive-Repulsive PSO for the input DDFG2 and 17.25 % better than Gravitational Search Algorithm for the input DDFG1 in wire length minimization.

For area minimization, performance improvement of the cuckoo search algorithm is 23.7% better than Particle Swarm Optimization for the input DDFG4, 24% better than Attractive-Repulsive PSO for the input DDFG3 and 19% better than Gravitational Search Algorithm for the input DDFG3.For wirelength and area minimization, an improvement in performance is 36.1%, 37.1% and 26% for the input DDFG3 when compared to PSO, ARPSO and GSA algorithms.

Logic level optimization at design entry level has been discussed in this research work, in which computing elements are designed using a new method called Muxed AOI Logic to achieve better placement. As an adder acts as the basic computing element, various types of existing carry select adder have been discussed and the results are compared with proposed logic based carry select adder. The simulation results prove that the proposed adder produces better placement with minimal area and wire length. Further, the proposed adder has been applied in multiply-accumulate unit design and the results validated.

The performance improvement of proposed adder in the number of LUTs used are found to be 17.8%, 24.4 5 and 17.8% when compared to regular 16bit square root carry select adder, modified 16bit square root carry select adder and AOI logic based carry select adder. The total real time to PaR completion time of proposed adder is 2 seconds, where the existing adders take 3 seconds for the same. Multiply and Accumulate unit has been designed and simulated using proposed adder with the Wallace tree multiplier and mod-2 logical shift multipliers. The number of LUTs used in former MAC unit is 75 whereas in the latter, the number of LUTs is 267. The total real time to PaR completion of proposed adder based MAC unit with Wallace tree multiplier was found to be 10 seconds and with mod-2 logical shift multiplier,13 seconds.

Thus, both the real and non-real time hardware tasks placement algorithms have been discussed and their performance analyzed in this research work. New methods and approaches have been proposed to improve the FPGA based design styles of digital systems related to applications. In future, this work can be extended to develop more real time optimization algorithms for better placement and integrating both scenarios of placement algorithms on System-On-Chip(SoC).