CHAPTER 2

LITERATURE SURVEY

2.1 INTRODUCTION

Basics of reconfigurable computing and its methods were discussed by (De Hon & Wawrzynek 1999, Todman et al. 2005). Reconfigurable computing architectures, models and algorithms have been explained in a paper presented by (Bondalapatti & Prassana 2000). The research issues in operating systems for reconfigurable computing have been investigated by (Wigley & Kearney 2002). The importance in role of reconfigurable hardware to execute the emerging applications such as embedded systems has been discussed in paper (Garcia et al. 2006).

Iqbal et al. (2010), presented the requirement of automation in placement and routing process of CAD flow to handle the high complexity design in reconfigurable computing platform. Hymer et al. (2007), have discussed the importance of scheduling and placement to attain better resource customization by exploiting partial reconfigurable devices which offers reduction in area, power and time.

2.1.1 Survey on Real time Hardware tasks Placement algorithms

Bazargan et al. (2000), have explained the various online and offline placement methods for dynamic and static reconfigurable FPGAs and different placement approaches for configuration management. Walder & Platzner (2002) developed footprint transform based placement for coarse grained non rectangular tasks.Analysis was carried out for various fitting strategies and the results showed that the best fit strategy performs better than the first fit strategy.They also discovered that the execution time gets improved by 4% using best fit strategy. Walder & Platzner (2003), discussed Earliest Deadline First (EDF) based scheduling methods for placement of tasks on block partitioned reconfigurable devices. A new concept of free space management using hash matrix based data structure was presented by (Walder et al. 2003) in order to find a feasible location at a constant time. In addition, simulation results showed that the placement quality improved upto 70%. Ahmadinia & Teich (2003), presented a new method called loop transformation in order to improve the speed of online placement of tasks.

Two heuristics namely horizon and stuffing have been presented by (Steiger ,Walder & Platzner, 2003) to tackle the nexus between scheduling and placement. Input sets were randomly generated to analyze the placement performance and a confidence level of 95% with an error range of +-3 % was obtained. Steiger,Walder, Platzner et al. (2003),proposed a guarantee-based scheduling method to improve the online scheduling and placement of real time tasks on partially reconfigurable devices. The performance analysis revealed that for a reasonable load and laxity class set of tasks, improved task rejection ratio was improved.

Steiger et al. (2004), discussed the operating systems for emdedded systems platforms. Tomono et al. (2004) discussed staircase algorithm with I/O communication constraints based placement process, which in addition to the degree of fragmentation, the speed of I/O communication has also been computed. Handa and Vemuri et al. (2004) introduced a novel representation of FPGA area and the placement performance analysis was carried out with help of staircase type data structure. The simulation results showed improved running time as it scans only 15% of FPGA cells.improvement in run time as it scans only 15% of FPGA cells.

Ahmadinia, Bobda, Bednara et al. (2004) introduced a new approach for online placement of hardware tasks (also called modules) on reconfigurable devices by managing the occupied space rather than free space information. Also considerable reduction in communication and routing costs was also been achieved. Ahmadidnia, Bobda & Teich et al. (2004) introduced new method of free space management based on Maximal Empty Rectangles (MER). The percentage of task rejection ratio between Keeping All Maximal Empty Rectangles (KAMER) method and cluster based method was compared and an 20% improvement was achieved.A new fragmentation metric model was presented by (Handa & Vemuri 2004) to obtain high quality placement and the online placement with best fit and first fit strategies were discussed.

Banarjee et al. (2005), in which cost improvement in terms of speed up and quality of 55% was achieved. Tabero, Jesus et al. (2006) explained the 3D adjacency value based placement to improve the vertex-list approach.A 2D window based stuffing method was proposed by made by (Zhou, X-G et al. 2006) in order to tackle the issue of 2D stuffing method.

Two preemptive scheduling methods namely Earliest deadline first(EDF) and server based scheduling called Merge Server Distribute Load (MSDL) were proposed by (Danne & Platzner 2005). The simulation results explained that the MSDL approach achieves an acceptance rate of 50% in tasks placement. Koester et al. (2005) proposed an algorithm for tasks placement on heterogeneous reconfigurable architectures. (Ahmadinia,Bobda,Fekete et al. 2004) proposed a method in which free space management has been carried out with constraints of minimal communication cost to place the incoming real-time hardware tasks in order to improve the task rejection ratio in online placement of tasks.

Elfarag et al. (2007) proposed fragmentation aware placement of tasks to minimize the miss ratio metric.(Cui,Gu et al. 2007) used scan line algorithm with incremental update approach to find the maximal empty rectangles on two dimensional PRTR FPGAs. Hardware multitasking management in runtime reconfiguration management ,using vertex-list approach was proposed by (Tabero,J et al. 2003 & Tabero, Jesus et al. 2004) in which the contour of unoccupied free fragment in reconfigurable computing device has been discussed. The compact reservation method has been proposed to reduce the runtime cost and the proposed method outperforms the 2D stuffing and 2D windows based stuffing by(Zhou, X et al. 2007).Three different works have been explained by (Cui,Deng, et al. 2007) for efficient online task placement algorithm such as fragmentation minimization on PRTR FPGAs, considering the probability distribution of sizes of future tasks arrival, 3D fragmentation metric and look-ahead heuristic. The simulation results showed a lesser task rejection ratio and a higher FPGA utilization in tasks placement.

Lu et al. (2007) proposed a novel model with resource wastage from placed and rejected tasks for placement quality measurement, which provides a clear representation of placement on FPGAs. A new concept in placement of hardware tasks using space filling curves have been explained by Both partition and merging concept were applied by (Roman et al. 2008) to allocate the tasks for their execution with real time constraints. The information about the dynamic reconfiguration architectures and its algorithms were discussed by (Vaidyanathan & Trahan 2003).

Septein et al. (2008), discussed new technique called relative quadrature of the free area perimeter to estimate the fragmented area, which is easy to compute the fragmentation factor Tabero, Jesus et al. (2008) discussed about the allocation heuristics and defragmentation measures for placaement. Marconi et al. (2008a) gave a new method called ‘Intelligent merging’ to improve the speed and placement quality of online placement algorithm. The author have explained how the proposed method outperforms Bazargan’s algorithm by 1.72 times faster and the quality was also found to improve by 0.89%.

(Lu,Marconi,Gaydadjiev & Bertels 2008) proposed a new method of scanning process to find the complete set of empty rectangles with the help of dynamic information of all running task edges. The proposed scanning method found the complete set of empty rectangles and proved that the speed of placement improved by 1.5 to 5 times.

True multitasking in resource management on 2D reconfigurable device was implemented by (Tabero, Jesus et al. 2008), in which vertex list set updater is used to track the free area boundary and the tasks allocation is based on look-ahead heuristic method. The space utilization ratio (SUR) based logic in classified stuffing method have been explained by(Marconi et al. 2008b) for online placement and the performance analysis was assessed both in quality and speed mode.

(Lu, Marconi, Gaydadjiev, Bertels, et al. 2008) presented an algorithm called Immediate fit (IF) method to handle the on-line placement problem on partially reconfigurable devices. Simulation has been carried out for mixed set of tasks to analyze the performance. Lu,C-H et al. (2010) proposed multiobjective hardware tasks placement algorithm by classifying the incoming tasks into three groups.1D reuse and partial reuse concept have been applied to reduce the reconfiguration time(Lu et al. 2009).

Marconi et al. (2009) proposedthe quad corner concept method to improve the online placement of tasks on FPGAs. Elbidweiby & Trahan (2009) proposed online placement with both maximal and vertical strips management known as the MHVS algorithm.Though the quality was much lower than the KAMER algorithm, it was found to be faster than the latter.Region based scheduling method for online placement of tasks has been discussed in a dissertation by (Elbidweighy 2009).

Xiao et al. (2009) developed an Scan line algorithm that can find empty rectangles which are not maximal. Duplicate scanning can be avoided by recording a set of scanned positions. Lee et al. (2010) introduced two procedures namely C-Look and CSAF to find the feasible candidate space for arriving tasks. Tasks placement using the proposed procedure yielded the following results by 76.4% in rejection ratio, 68.12% in execution speed and 76.32% in total waiting method. An efficient online task scheduling algorithm with an effective area partitioning model was introduced by (Lu et al. 2010) and the result showed that the scheduling approach performs better. Bassiri & Shahhoseini (2011b) have discussed the various FPGA area models and the fitting strategies used for real time hardware tasks placement. Hong et al. (2011)proposed a novel online placement algorithm called Empty Area Compaction (EAC) with first fit approach to achieve the overall task acceptance rate and the execution time was found to be 10µs.

Wassi-Leupi (2012) discussed the various scheduling algorithms for tasks placement in a dissertation. Bassiri & Shahhoseini(2011a) proposed reusing based scheduling technique for real time hardware tasks placement in targeting reconfiguration overhead minimization. In order to improve the length of contiguous free space, tabu search method based dynamic defragmentation method were presented (Fekete et al. 2012).

Marconi & Mitra (2011) have recorded the increasing demand for 3D FPGAs due to reduced wire length, delay, power, channel width and energy consumption and modelled an 3D FPGAs. A new concept known as blocking effect was introduced for real time scheduling and placement. The proposed algorithm produces 61% better solutions with a 15% longer runtime overhead.

Various issues and methods in online hardware tasks scheduling and placement have been discussed (Marconi, 2011). Lin et al. (2013) concentrated on analytical placement using multilevel timing and wire length driven by assuming novel block alignment to improve the scalability in FPGA placement. Their simulation results show better improvement in speed up.

2.1.2 Survey on Non Real time Hardware tasks Placement algorithms

The importance of CAD tools in design process and genetic algorithm based FPGA placement has been highlighted by (Baruch et al. 1999). Gudise & Venayagamoorthy (2004) analyzed the PSO algorithm based FPGA placement and routing. Swarm intelligence algorithm namely the particle swarm optimization algorithm based digital circuits implementation on FPGAs platforms has been proposed by (Venayagamoorthy & Guidise 2004).

The simulated annealing method based placement of non real time hardware tasks on FPGA for its execution has been given by (de Lima et al.2007). To facilitate the hardware tasks placement on heterogeneous dynamic reconfigurable FPGAs, genetic algorithm has been applied by (Nousias et al. 2007)and the multi-objective cost function was devised to perform the analysis. Xu et al. (2007) presented a novel meta heuristic algorithm named Ant colony optimization for tasks placement on FPGAs and compared the performance with a few optimization algorithms. Experimental results prove that the proposed algorithm achieves a better performance.

Genetic algorithm based FPGA placement and routing with different cost function have been discussed by (Yang, M et al. 2007). El-Abd et al. (2010) presented discrete co-operative particle swarm optimization based hardware tasks placement,which is slightly different from the normal PSO in FPGA placement. In order to obtain optimal FPGA area in hardware tasks placement, genetic algorithm has been applied by (del Solar et al. 2004) for analysis.

Rajabioum (2011) discussed the modified cuckoo search algorithm to solve the engineering problems. Further, the improved cuckoo search algorithm for optimization algorithms discussed by (Valian et al. 2011).Particle swarm optimization algorithm based placement and routing of hardware tasks on FPGAs have been discussed by (Benuel Sathish Raj et al. 2012) and the cost function has been calculated using the manhattan distance formulae ,considering 14x14 CLBs as FPGA area for experimentation.The performance was measured with respect to wirelength minimization. They analyzedan 4-bit ALU on Xilinx XC4000 FPGA model.

Mohanty et al. (2012) made comprehensive study on simulated annealing based placement algorithm. Farokhi & Sabbaghi-Nadooshan (2013) discussed a new ant colony algorithm based on mutation for hardware tasks placement on FPGAs placement and a performance analysis was carried out. Bali et al. (2013) discussed the PSO-SA technique for wirelength minimization in hardware tasks placement on FPGAs.

Yang, X-S & Deb (2013) have presented the better design optimization using Multi-objective cuckoo search algorithm. The importance of nature inspired algorithm for optimization to solve the real life problems was explained by (Fister Jr et al. 2013).Further,Gravitational search algorithm to optimize the NP-Complete problem have been discussed by(Eldos & Al Qasim 2013) which can be applied to solve the FPGA Placement.

The technical details of Xilinx FPGAs were presented in the programmable data sheet (Book 1996). Brown and Rose 1996 discussed the field programmable devices and their programming technologies. Rose & Hill (1997) explained that the total delay of circuit due to routing increases with each process generation. CAD flow and its algorithms for Field Programmable gate arrays based system design have been discussed by Gerez 1999.

The details of internal functional blocks of Field Programmable Gate arrays have been explicated by (Vantis Corporation 1998). Betz & Rose (1998) presented an area efficient FPGA based on cluster based logic to reduce the size of placement problem and to increase the speed of execution on FPGAs. In order to reduce the area with the penalty of speed, multiplexer based add one circuit have been proposed by (Kim & Kim 2001), which replaces the dual RC adders.Proposed adder requires 42% fewer transistors than the conventional carry select adder. He et al. (2005) proposed a modified area-efficient 16-b SQRT CSA using binary to excess-1 converter circuit for ripple carry adder in order to achieve optimal power and area.

Kuon & Rose (2006), explained the advantages of using field programmable devices in runtime reconfigurable systems which can be benefited with a higher cost of power, larger area and low speeds when compared to the ASICs. Ramkumar et al. (2010) developed an ASIC implementation of fast carry select adder using the modified method. Introducing simple gate level modification named BEC logic in normal CSA with low power and area efficient carry select adder have been proposed by (Ramkumar & Kittur 2012) and the performance analysis was also carried out.D-latch based design of Carry select adder was proposed by Nair (2013) to achieve low power and area efficient adder.

2.2 SUMMARY

This chapter summarizes the literature survey on different methods of real and non real time hardware tasks placement algorithms on reconfigurable FPGAs. This chapter gives references related to placement issues and the various solutions presented in the literature to obtain better placement. This literature survey also highlighted the importance of efficient real and non-real time hardware tasks placement algorithms.

Further, the survey also provides the knowledge about the tasks modelling, different methods of free space management, fitting strategies, scheduling methods, placement algorithms and its metrics, analysis procedures and so on, in order to execute real time hardware tasks placement.This literature survey also gives the importance of optimization algorithms to execute non real time hardware tasks, in order to obtain the better placement. The design of computing elements to achieve high speed and less area has also been discussed. With the intention of utilizing the advantages of FPGA based designs, this research work also focuses on developing different methods and approaches for the placement of real and non real time hardware tasks related to an application.